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QCA-based Implementation of Budget-friendly and Energy-Efficient Exclusive-OR/Exclusive-NOR Gates

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Abstract

Quantum-dot cellular automata (QCA) is a novel nanoscale computational approach that proposes reduced dimensions, lower power consumption, increased speed, and deliberate design as a solution to the scaling challenge associated with CMOS technique. QCA is a nascent nanotechnology that utilizes the Coulomb repulsion principle. Quantum computing has emerged as a highly effective paradigm for the creation of energy-efficient hardware at the nanoscale. This article presents implementation of a very efficient and simplified 2-bit QCA XOR gate in QCA Designer tool. The suggested design exhibits a reduced quantity of quantum cells and spatial dimensions compared to its most optimal pre-existing QCA configurations. The simulation results demonstrate that the proposed architecture exhibits superior performance compared to the most optimal existing layouts in terms of quantum cell count, area, latency, and quantum cost.

Keywords: Exclusive-OR, Exclusive-NOR, QCA, Majority Voter Gate, CMOS

INTRODUCTION

Quantum-dot Cellular Automata (QCA) is an emerging technology that offers potential as a viable alternative to address the limitations associated with complementary metal-oxide-semiconductor (CMOS) technology and its dependence. This article provides a comprehensive understanding of the energy efficient and budget-friendly designs of Ex-OR and Ex-NOR logic gates in Quantum-dot Cellular Automata (QCA) technology. The utilization of the QCA designer tool has been employed for the purpose of simulating and verifying physical outcomes (D. Tripathi et al., 2020) [1]. In addition, researchers have also endeavored to investigate the energy and power analyses of the proposed design. In addition to QCA Technology, there are other emerging technologies such as CNT (A. Bachtold et al., 2001) [2], SiNWs (Y. Zhang et al., 2017) [3]. However, QCA stands out due to its notable characteristics, including a high device density of up to 10^{12} devices/cm^2 and a high speed in the terahertz range. Consequently, QCA demonstrates greater feasibility compared to other new technologies. QCA utilizes a novel computational approach in which binary information is stored in the state of an electron, as opposed to the conventional use of current. Instead of utilizing physical wire connections, the cells transmit information within the circuit.

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CONCEPT OF QCA

QCA designs originate as a sequential arrangement of quantum cells, wherein each cell transmits data electrostatically to its adjacent cells (A. Moustafa., 2019) [4], (M. Niemier., 2004) [5]. The QCA-cell plays a crucial role in the QCA strategy, enabling the execution of computations and information flow through the cells. Each individual cell is engaged in a bonding arrangement with a pair of electrons, as seen in Figure 1.

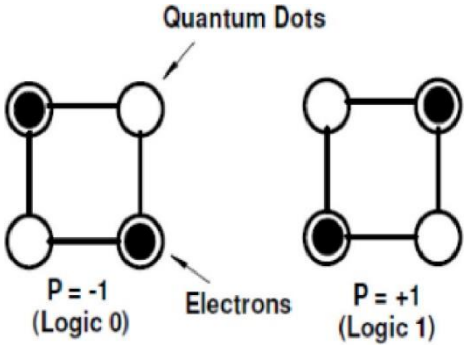

Figure 1. QCA Cells polarization Polarizations (C. Lent et al., 1997) [6].

Cell polarization refers to the establishment of an electric field within a Quantum Cellular Automata (QCA) cell, which determines whether the electrons within the cell are assigned a binary value of '1' or '0'. There are two initial states of QCA cells that are available: one consists of regular cells oriented at 90°, while the other consists of rotated cells oriented at 45°. Figure 1 depicts a 90° cell exhibiting a polarization state of p = +1, which corresponds to the *binary value 1* (A. Chabi et al., 2014) [7]. Conversely, a polarization state of p = -1 reflects the *binary value 0*. The cells that are in a relaxed condition remain in a non-polarized state, as indicated by previous studies (A. Chabi et al., 2014) [7], (S. Hashemi et al., 2013) [8].

Majority Voter Gate

The positioning of the majority gates is advertised in Figure 2. The outcome of a QCA cell wanders, managing to the computations of a QCA cell within the means of the gate. The majority gate plays a basic portion in constructing the AND/OR gates (D. Tripathi et al., 2020) [1], (A. Moustafa., 2019) [4]. In QCA all digital logic gates are made up of Majority gates. If the polarization of the majority gate is -1 then it becomes AND gate and if +1 then it becomes OR gate QCA architecture.

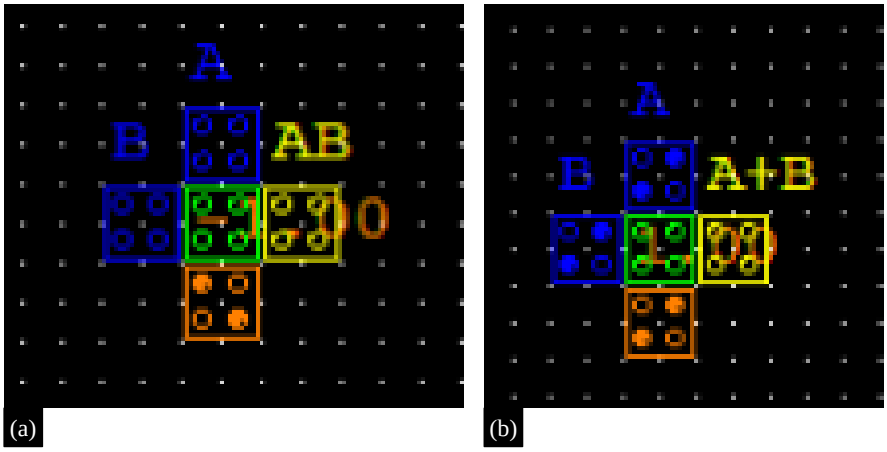

Figure 2. (a) Majority voter as AND gate (b) Majority voter as OR gate.

Clocking in QCA

QCA Clocking gives the capability to create and invalidate the meta-stable stage (M. Niemier., 2004) [5], (G. Singh et al., 2016) [9]. The QCA clocking action contains fourfold stages: Switch, Hold, Release & Relax. As shown in Figure 3, During the Switch phase, the barriers are raised, and the cells become polarised based on the state of its neighbouring cell. During the Hold phase, barriers are kept at a high value. This allows the outputs to drive the next stage inputs. The barriers are lowered during the Released phase, and the cell remains in an unpolarized neutral state. The cell remains in an unpolarized neutral state during the Relaxed phase. Cells in a QCA are linked to four clocking zones, each lagging by 90 degrees in phase.

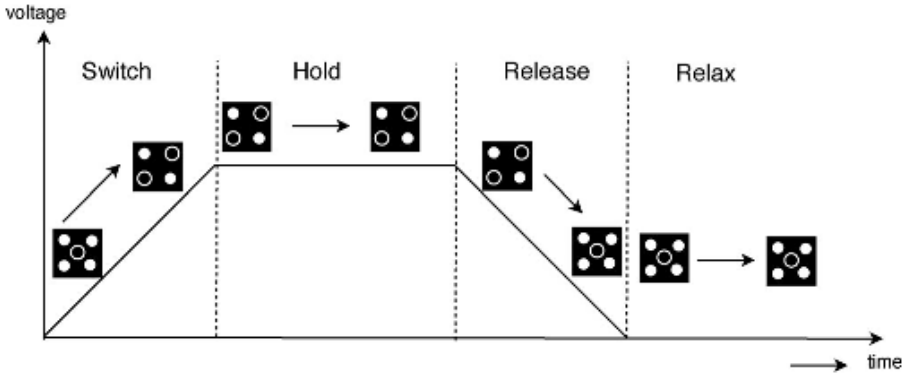

Figure 3. QCA clocking phases (C. Lent et al., 1997) [6].

IMPLEMENTED QCA Ex-OR and Ex-NOR ARCHITECTURES

QCA XOR Gate Topology

An exclusive-OR (XOR) gate is a base of every contemporary ICs and ALUs. The exclusive-OR (XOR) gate is vital to suggest designing of any compound circuits. In previous research, various QCA designers created XOR gates that are explained (S. Hashemi et al., 2013) [8], (X. Fengbin, et al., 2017) [10].

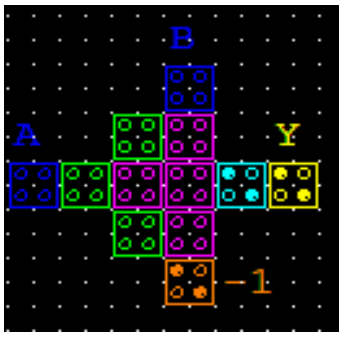

Figure 4. Implementation of 2-input Ex-OR Gate

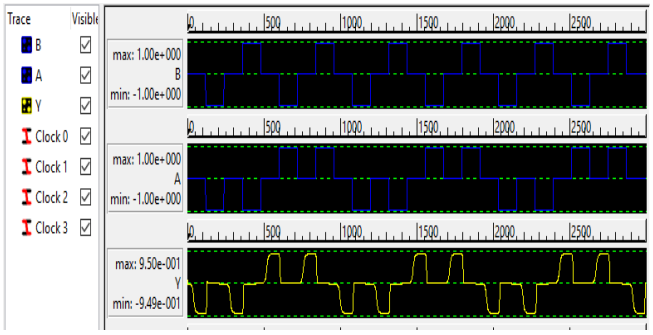

Figure 5. Simulation waveform of 2-input Ex-OR Gate.

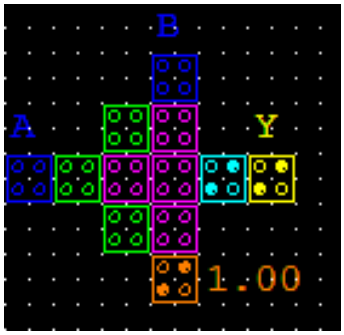

Figure 6. Implementation of 2-input Ex-NOR Gate.

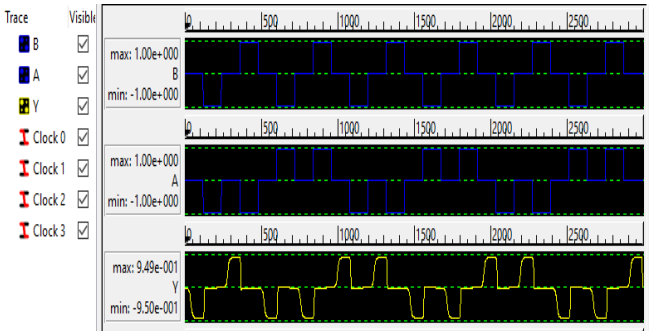

Figure 7. Simulation Waveform of Ex-NOR in QCA Designer.

The implemented both QCA 2-input XOR & 2-Input X-NOR layouts consist of *12 quantum cells and 0.01 μm^2 area* as shown in Figure 4 & Figure 6 and the simulation outcome waveform is shown in Figure 5 & Figure 7. There is *0.75 Clock latency* observed in the case of both the implemented designs [11–14]. Based on Simulation outcome waveform both the designs are functionally verified with their respective truth Tables.

Power consumption of Ex-OR & Ex-NOR is 0.035 nW & 0.032 nW respectively and *Average Energy dissipation* of Ex-OR and Ex-NOR is 0.885 meV & 0.835 meV respectively.

SIMULATION OUTCOMES AND DISCUSSION

Quantum dot cellular automata are taken for simulation of suggested QCA designs. The simulation parameter just like the quantum cost, an area utilized, latency, and quantum cost has been calculated and coordinated after optimizing the number of cells and coordinated reducing area so the latency will also be decreased (A. Bahar et al., 2017) [15], (A. Chabi et al., 2017] [16]. The proposed methodology used is optimized and realizes the QCA layout with the best competency related to the existing design. In gain, the suggested circuit simulation results are estimated with the corresponding truth table 1. QCA can be a novel methodology for enhancement of the parameter like area, shortening the quantum cell for nano scale circuitry which is applicable to the design of extremely functional digital logical circuitry. The comparison table explained that the implemented QCA architectures of QCA XOR, QCA X-NOR, have gained a less QCA cell count, area and quantum cost as related to previously existing QCA layouts. Table 1 shows the QCA XOR gate, Table 2 explains QCA XNOR gate, Table 3 shows the Various performance Parameters associated with implemented digital designs in QCA. In this article, a cost efficient and optimum QCA layout of XOR gate and X-NOR Gate is suggested. The suggested architecture has very few cells and higher solidity as related to its actual past counterpart.

Table 1. Performance comparison of QCA XOR design with existing design

QCA XOR Gate	Cell Count	Area (μm^2)	Latency (Clock Cycles)	Quantum Cost= (Area * Latency)
(S. Hashemi et al., 2013)	60	0.0115	1.5	0.016
(A. Chabi et al.,2014)	51	0.0926	2.0	0.184
(G. Singh et al., 2016)	29	0.0414	0.25	0.010
(A. Bahar et al., 2017)	28	0.0357	0.75	0.026
(A. Chabi et al.,2017)	12	0.0211	0.75	0.015
(X. Fengbin, et al., 2017	14	0.0345	0.75	0.025
Implemented XOR	*12*	*0.010*	*0.75*	*0.007*

Table 2. Performance comparison of QCA XNOR design with existing design

QCA XNOR Gate	Cell Count	Area (μm^2)	Latency (Clock Cycles)	Quantum Cost= (Area * Latency)
(L. Wang et al., 2020)	36	0.0431	0.75	0.032
Implemented X-NOR	*12*	*0.010*	*0.75*	*0.007*

Table 3. Performance parameters of QCA XOR and QCA XNOR

Circuit Design	Cell Count	Area (μm^2)	Latency (Clock Cycles)	Quantum Cost= (Area * Latency)	Average Energy Dissipation Eav (meV)	Power Dissipation (nW)
Implemented XOR	12	0.010	0.75	0.007	0.885	0.035
Implemented X-NOR	12	0.010	0.75	0.007	0.832	0.33

PERFORMANCE PARAMETERS

To assess the design effectiveness of any architecture in QCA technology, it is necessary to consider three fundamental parameters: the number of cells, the area utilized in micrometers squared (μm^2), and the latency. By quantifying these factors, it is possible to make comparisons between any given circuit and past circuits. The measurement of these characteristics is facilitated through the utilization of a simulation tool known as QCA designer 2.0.3. A summary of these performance metrics, among others, is as follows:

(1) *Cell count:* The term "cell" pertains to the collective utilization of individual components in the construction of a circuit design. For instance, 2-input AND/OR gates are fabricated utilizing 5 cells. (V. Jain et al., 2023) [17]

(2) *Area Occupied:* The term "Area occupancy" refers to the overall spatial utilization of cells within a given circuit. In the process of design, it is customary to position each individual cell at 2 nm from its neighboring cell. Additionally, it should be noted that the surface area occupied by an individual cell measure 324 nm^2. The total area is calculated by selecting all cells that have a separation gap. For instance, the 2-input AND/OR gates collectively occupy an area of 3232 nm^2 each, encompassing the space between neighboring cells. (V. Jain et al., 2023) [17]

(3) *Delay:* The calculation is determined by multiplying 0.25 with the total number of clock phases utilized in generating the desired output. For instance, the 2-input AND/OR employ two clock phases each to get the desired outcome. Therefore, the latency of the entity is calculated as 0.25 multiplied by 2, resulting in a value of 0.5. (V. Jain et al., 2023) [17]

(4) *Cost Function:* The circuit complexity in QCA technology is determined by the utilization of majority gates, inverters, and crossovers. The utilization of a cost function is a common approach in academic literature to quantify the level of complexity. The computation of a constructed circuit is performed using the formula provided in Equation 1.

$$\text{Cost Function} = [(MV)^K + INV + (CO^L] * T^P \quad \text{……. Equation-1 (V. Jain et al., 2023)}$$

In the above equation, the symbols MV represent majority gates, INV represent inverters, CO represent crossings, and T represent clock phases. In this context, the variables K and L are assigned a fixed value of 2, whereas the variable P remains constant at a value of 1.

SIMULATION PARAMETERS

Simulation parameters used to implement the designs are depicted in Table 4 given below.

Table 4. Simulation parameters

Parameters	Values
Radius of effect	65 nm
Relative permittivity	12.9
Cell size	18 nm
Cell area	324 nm^2
Separation gap	02 nm
Overall samples	12000
Convergence tolerance	0.0000100
Clock low	3.8×10^{-23} J
Clock shift	0
Clock high	9.8×10^{-22} J
Clock amplitude factor	2
Layer Separation	11.5
Maximum iteration/sample	100

CONCLUSION AND FUTURE SCOPE

Nanotechnology has been the center of current analysis about the growth of nano-electronics circuitry. As digital logic gates are rudimentary for maximum digital circuitry, requiring higher speed, less complex and least zone designs are imperative. This paper gives an optimal way to execute a 2-input XOR and XNOR in the QCA Designer simulation tool for nanotechnology applications. According to execution parameter comparison, it is overseen that the implemented QCA XOR and QCA XNOR gate designs have attained an efficient and optimum layout and achieved less parameter count like area occupied, quantum cost and latency as related to its best previous counterparts. The suggested cost efficient XOR & X-NOR gate layouts consist of only 12 regular quantum cells and latency of only 0.75 clocking cycles. This study has the potential to be applied in future research for

the advancement of QCA-based Full Adder, Full Subtractors, Binary incrementor circuits, ripple carry adders, and other circuits of varying lengths. The proposed methodology employed is optimized and effectively implements the QCA layout, showcasing superior expertise in relation to the current design.

Conflicts of Interest

The Authors declare that they have no conflicts of interest in this work.

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