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The Role of Majority Functions in Enhancing Full Subtractor Performance in High-Density Logic Circuits

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Abstract:-

In the present trend of very large-scale integration (VLSI) technology, implementing a Boolean function with the fewest number of gates (logic) has always been important. Low power design strategies now provide much more benefits than in the past. Performance, affordability, and dependability may be key issues in this area of technology design. Power dissipation is now recognized as a crucial component in the development of competitive market areas such wireless applications, laptops, and portable medical equipment. In this paper, we have compared multiple full subtractor circuits for their total transistor count and overall power consumption. We have proposed a majority function based full subtractor and compared the same with the existing one. The proposed circuit shows some substantial benefits over its existing counterpart.

Keywords:- VLSI, Majority function, Leakage Power, MTCMOS, Threshold.

Introduction:-

Two single bit numbers can be subtracted using the half subtractor. Half subtractors are not allowed to "Borrow-in" information from the prior circuit. So, full subtractors are used to get

around this problem. A full subtractor is a combinational logic circuit which is employed to perform more than two single bit number subtraction. Additionally, it considers lower substantial stage borrowing. As a result, a full subtractor is capable of subtracting three bits. Three inputs and two outputs make up a full subtractor (Difference and Borrow). In our approach, the full subtractor is designed around majority-based function. A majority function (Fig.1) is nothing but a circuitry whose output is logic 1 whenever majority of its inputs are at logic 1 and vice versa. It is designed using capacitors connected in between input and output. A generalized block diagram of the majority is shown in Fig.1. This paper exhibits the proposed of full subtractor with the use of 12 transistors and majority function and thus compared with the 20 Transistors and 14 transistor existing model of full subtractor [5].

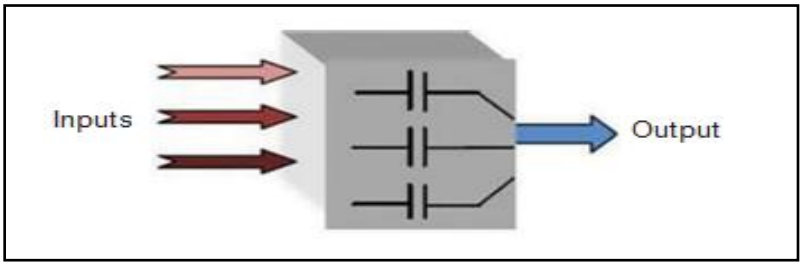

Fig 1. Majority function

Existing Methodology:-

20 TRANSISTOR MODEL:

Several techniques [1],[2],[3],[4],[10] have been proposed to reduce the number of transistors in both full adder and subtractor in order to reduce power consumption, delay and fabrication cost. Fig.2 shows the Full Subtractor transistor level circuit diagram with twenty transistors. It uses less power, has lower leakage current, and takes up less space than a static CMOS Full Subtractor since the number of transistors is lowered. Here six transistors are utilized to accomplish the difference equation and ten transistors to deduce the borrow by inverting four transistors [5]. Here the length of PMOS and NMOS is 0.25um whereas the width of PMOS is 2.175um and width of NMOS is 4.175um respectively.

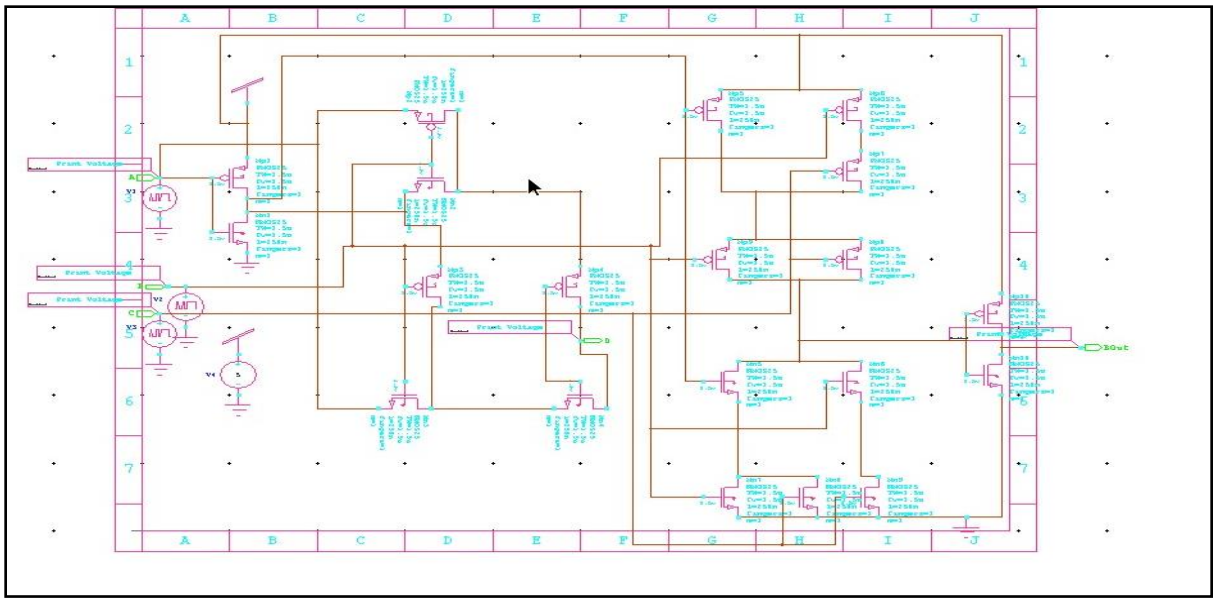

Fig:2. Full subtractor with 20 transistors

OUTPUT OF 20T MODEL OF FULL SUBTRACTOR:

After simulating the circuit of 20 transistors model at Tanner EDA tool (250nm) the output is shown at Fig.3. Where the "difference" part has a little noise/distortion. Which can be rectified by changing the input parameters or by adjusting the width of the transistors.

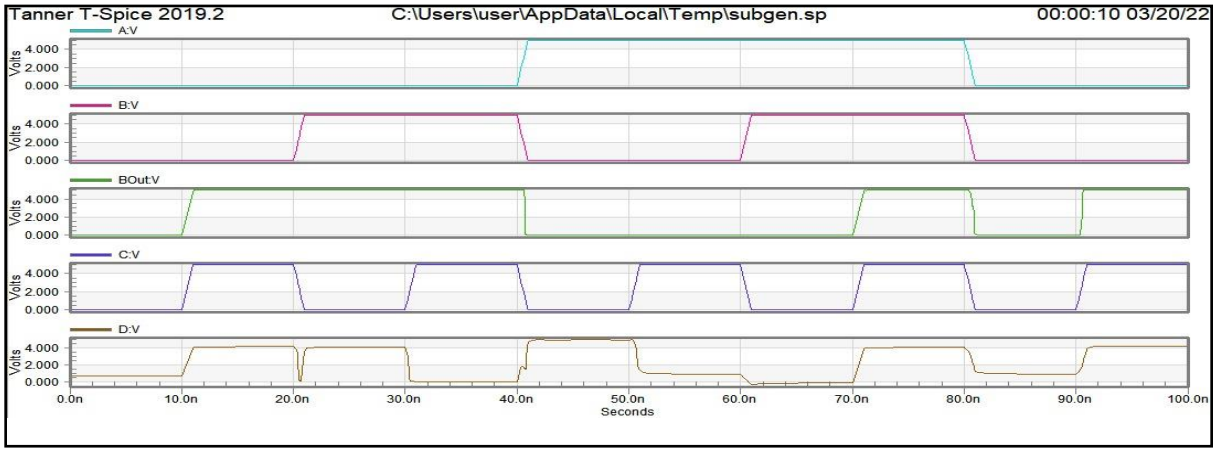

Fig.3: Output of full subtractor with 20 transistors

14 TRANSISTORS MODEL:

Fig.4 shows the 1-Bit Full Subtractor transistor level circuit schematic. The six transistor XNOR - XOR modules generate 2 intermediate signals that are fed into the MUX (2x1). The two intermediate signals produced by the above logic gates serve as inputs to the MUX (2x1), while the 3rd input serves as the multiplexer's selection line. The output of the multiplexer is used to calculate the difference among the inputs that is A, B, and C. Two AND gates and one OR gate

are used to create Borrow [6],[7],[8],[9],[11]. Here the length of PMOS and NMOS is 0.25um where as the width of PMOS is 2.175um and width of NMOS is 4.175um.

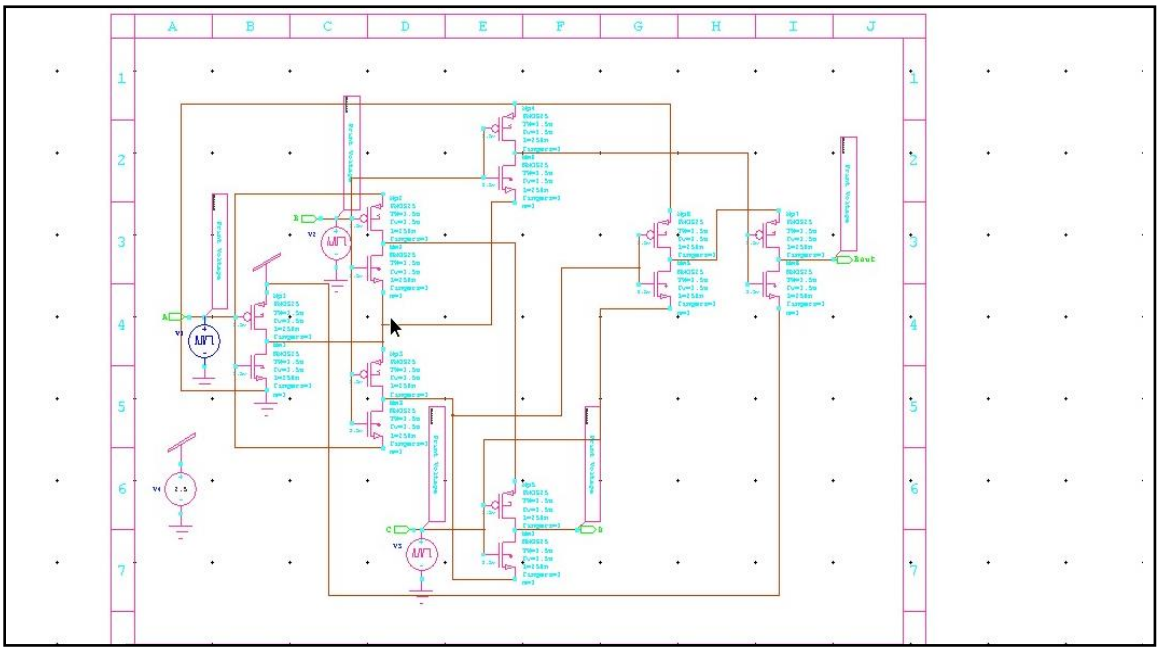

Fig.4 : Full subtractor with 14 transistors

OUTPUT OF 14T MODEL OF FULL SUBTRACTOR:

After simulating the circuit of 14 transistors model at Tanner EDA tool (250nm) the output is shown at Fig.5. Where the "difference" part and the "borrow" part has a little noise/distortion. Which can be rectified by changing the input parameters or by adjusting the width of the transistors.

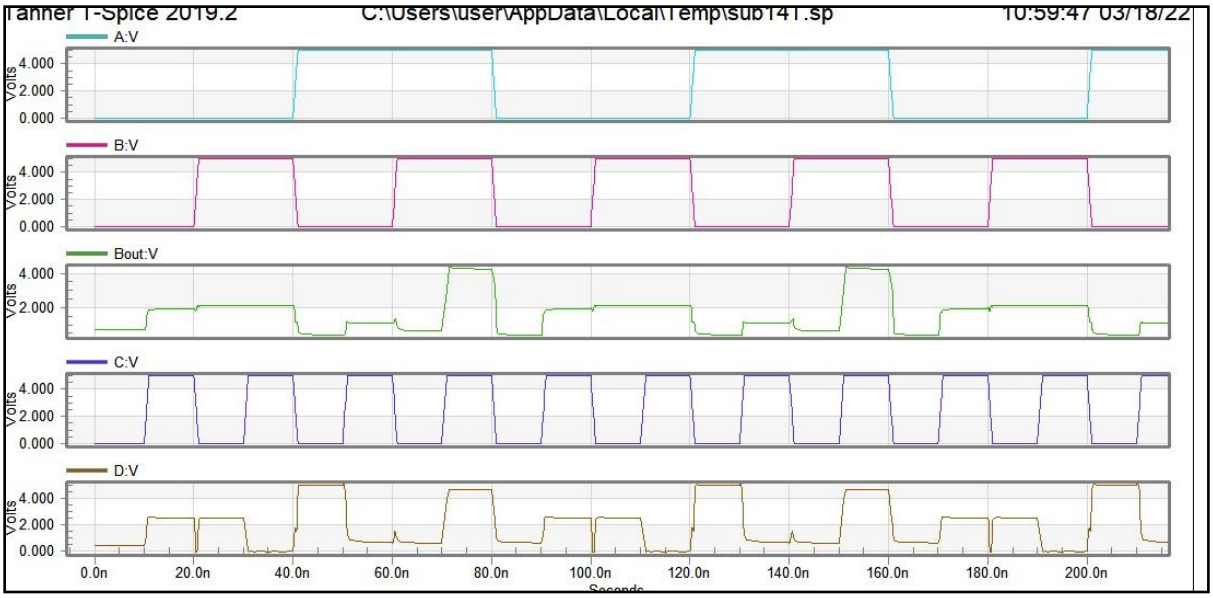

Fig.5: output of 14 transistor model of full subtractor)

PROPOSED DESIGN OF FULL SUBTRACTOR WITH 12 TRANSISTOR:

Below in Fig.6, shows the proposed design of full subtractor using 12 transistors .The circuit consists of 12 transistor (6 NMOS and 6 PMOS). No changes have been made in the (D) difference section of the full subtractor compared to its existing counterpart. But borrow has been deduced using majority function [11]. The value of all the capacitors has been taken as 5 fF.

The output of the borrow section which is built around majority function changes its state whenever its inputs are at majority ‘1’ or majority ‘0’. If more than two of the inputs are at logic ‘1’, then its output will also be at logic ‘1’ or vice versa.

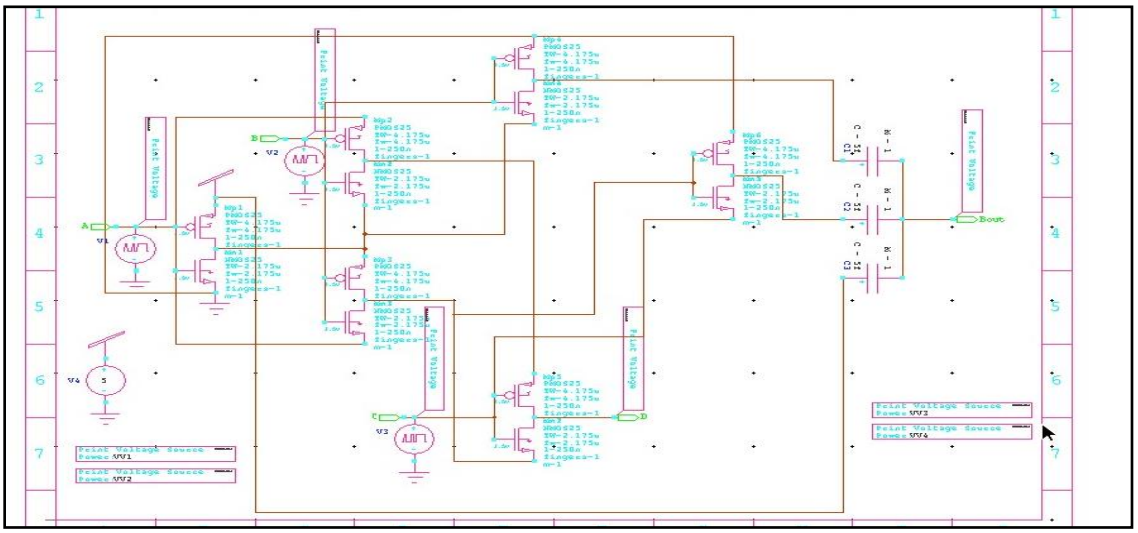

Fig.6 : proposed 12Transistor models

OUTPUT OF PROPOSED 12 TRANSISTOR DESIGN

Fig.7 shows the output of the proposed design of 12 transistors model . where A,B and C are the inputs , the D and, Bout are the output. At the Bout and D section (fig:7) there is a distortion / noise , which can be properly achieved by changing the values and parameters in the circuit.

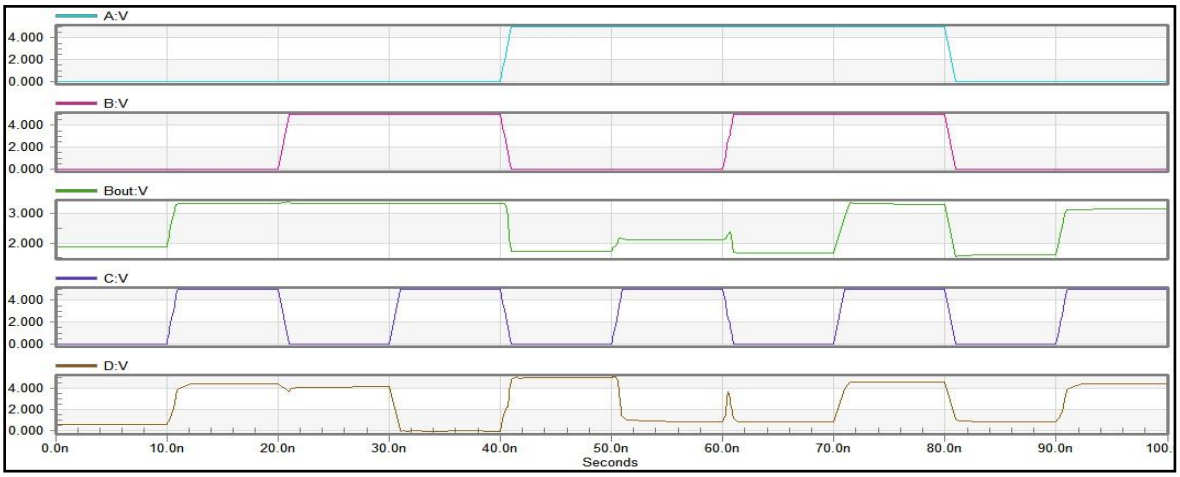

Fig.7:output of proposed 12 transistor

COMPARISON AMONG DIFFERENT CIRCUITS

Below in Table.1, comparison among 20 transistor , 14 transistors and the proposed 12 transistor design is tabulated. Here in every model the length of all the transistors is kept 0.25um. The width of PMOS and NMOS is kept at 4.175um and 2.175um respectively. The value of the capacitor is chosen to be of 5fF.

In 250 nm technology ,the average power consumed by the 20 transistor model is 227.49uw and the 14 transistor model has the average power consumption of 99.52uw. The proposed design of majority function based subtractor has the average power consumption of 98.84uw, which is slightly lesser than the 14 transistor model which can be further be lessened by changing the parameters of the transistors. Comparison of different techniques is shown in Table 2.

20T MODEL OF FULL SUBTRACTOR	14T MODEL OF FULL SUBTRACTOR	PROPOSED 12T MODEL OF FULL SUBTRACTOR
*Transistors used =20	*Transistors used = 14	* Transistors used = 12
10 NMOS and 10 PMOS has been used	7 NMOS and 7 PMOS has been used	6 NMOS and 6 PMOS has been used
Length of NMOS and PMOS = 0.25u Width of NMOS=2.175u Width of PMOS =4.175u	Length of NMOS and PMOS = 0.25u Width of NMOS=2.175u Width of PMOS =4.175u	Length of NMOS and PMOS = 0.25u Width of NMOS=2.175u Width of PMOS =4.175u Capacitor = 5fF
Average power consumed is 227.49uw	Average power consumed is 99.52uw	Average power consumed is 98.84uw

Table 1: comparison of 20T , 14T , 12T full subtractor

Comparison chart of existing and proposed techniques :

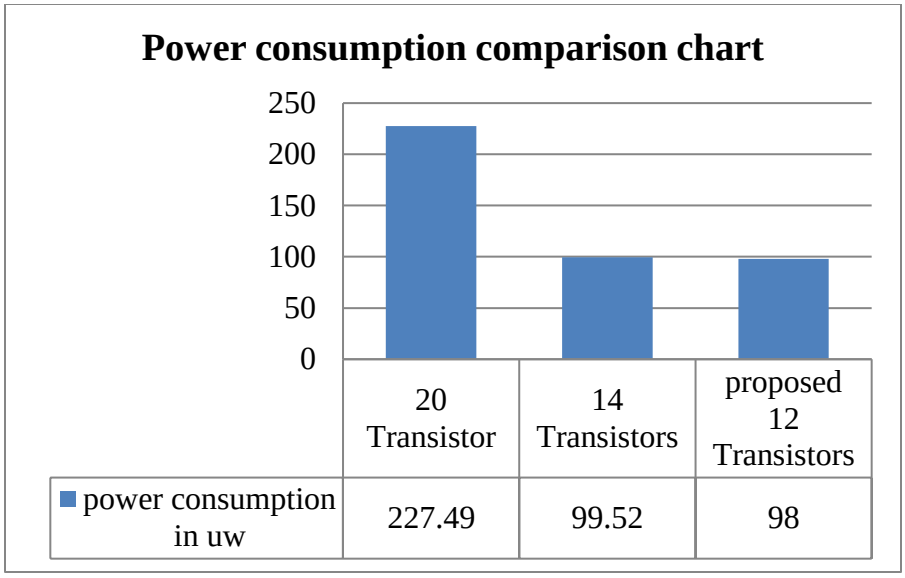

Fig 2: Comparison of different techniques.

CONCLUSION

From the output waveform and the numerical results, it is evident that a full subtractor can be implemented using 12 transistors with minimized power consumption. However there exists some noise at the output due to low voltage swing (VoL), which can be minimized by adopting proper voltage swing techniques.

FUTURE WORK

The proposed 12 T design of full subtractor has the desired output, but it suffers from low level output swing(VoL). Through further research, the noise can be reduced to zero by adopting proper output voltage swing techniques.

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