

Performance and Analysis of 6T, 8T and 10T SRAM Cell in 28 nm Technology

Anagha Kamdi^{1*}, Sanket B. Kasturiwala²

Abstract

Technology scaling into deep sub-micron regimes has significantly increased the design challenges of Static Random Access Memory (SRAM), particularly at the 28 nm technology node. As transistor dimensions shrink, SRAM cells become more vulnerable to stability degradation, leakage current, process variations, and reduced noise margins, which adversely affect the overall memory performance and reliability. The conventional 6T SRAM cell remains widely used because of its compact structure and high storage density; however, its read and write stability deteriorates considerably with advanced technology scaling. To address these limitations, alternative SRAM architectures, such as 8T and 10T cells, have been developed. These designs introduce additional transistors to separate the read and write operations, thereby improving cell robustness, enhancing noise margins, and reducing read disturbance effects. However, these benefits are achieved at the cost of increased silicon area and design complexity. This paper presents a comparative analytical study of 6T, 8T, and 10T SRAM cells implemented at the 28 nm technology node using theoretical analysis and literature reports. Key performance parameters, including stability, leakage power, read and write reliability, variability tolerance, and area overhead, were evaluated and discussed. This study highlights the operational characteristics, advantages, limitations, and trade-offs associated with each architecture, providing valuable insights for selecting suitable SRAM designs for modern low-power and high-performance CMOS applications.

Keywords: SRAM, Read/write reliability, leakage power, 28 nm technology node, technology scaling.

INTRODUCTION

Static random-access memory (SRAM) is a fundamental semiconductor memory technology widely used in modern electronic systems because of its low latency, high speed, and compatibility with CMOS processes. It plays a critical role in system-on-chip designs, processors, and caches, making it a major focus for research and development in electronics, especially as technology scales to advanced nodes [1, 2]. SRAM exists in multiple architectural forms, among which 6T, 8T, and 10T cells are commonly studied, with each variant addressing specific challenges related to stability, power, and variability issues.

While conventional 6T SRAM offers high density, 8T and 10T architectures have been developed to improve read and write reliability at scaled technologies by mitigating the limitations introduced by aggressive transistor scaling [3, 4].

The 6T SRAM cell, as shown in Figure 1, is the conventional and most widely used memory cell owing to its compact area and simple structure. It consists of two cross-coupled CMOS inverters formed by four transistors that store data and two access transistors that connect the internal storage nodes to the complementary bitlines during read and write operations. The word line controls the access transistors, enabling an interaction between the cell and bit lines [5, 6].

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The 6T SRAM operates as follows:

- *Hold operation (Static state)*: During the hold operation, the word line remains disconnected, isolating the storage nodes from the bit lines and allowing the cross-coupled inverters to retain the stored data.
- *Read operation (Fetching data)*: In a read operation, both bit lines are precharged to the supply voltage, and the word line is asserted. Depending on the stored data, one of the bit lines discharges slightly, creating a differential voltage that is sensed by the sense amplifier.
- *Write operation (Changing data)*: write operation in a 6T SRAM cell is performed by driving complementary data on the bit lines and asserting the word line. The bit-line drivers must overpower the cross-coupled inverters to flip the stored values.

8T SRAM cell

The 8T SRAM cell, as shown in Figure 2, is a memory architecture that extends the conventional SRAM structure by adding extra transistors to support a separate read mechanism. It consists of a storage core formed by cross-coupled inverters and a dedicated read path implemented using two additional transistors controlled by an independent read word line.

The 8T SRAM cell operates as:

- *Hold operation (Static state)*: During the hold operation, both the read word line and write word line remain deselected, isolating the storage nodes from all bit-lines. The cross-coupled inverters maintain the stored data through positive feedback, whereas the dedicated read path remains inactive, ensuring stable data retention.
- *Read operation (Fetching data)*: In a read operation, the read bit line is pre-charged to the supply voltage, and the read word line is asserted. Based on the stored data, the read path conditionally discharges the read bit line without directly connecting the internal storage nodes. The resulting voltage change on the read bit line is sensed by the sense amplifier to determine the stored value.
- *Write operation (Changing data)*: write operation in an 8T SRAM cell is performed by applying complementary data to the write bit-lines and asserting the write word line. The access transistors allow the bit-line drivers to update the stored data in the cross-coupled inverters, after which the write word line is deselected to restore the hold state [7, 8].

10T SRAM cell

The 10T SRAM cell, as shown in Figure 3, is an enhanced SRAM architecture designed to support robust memory operation through additional control over both the read and write processes. Its architectural approach allows the 10T SRAM cell to maintain stable operation across varying operating conditions, making it suitable for advanced low-voltage memory designs.

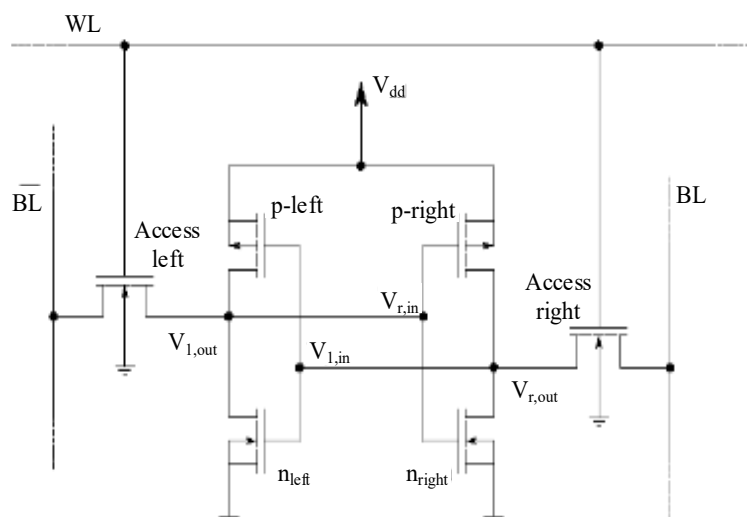


Figure 1. Architecture of 6T SRAM cell.

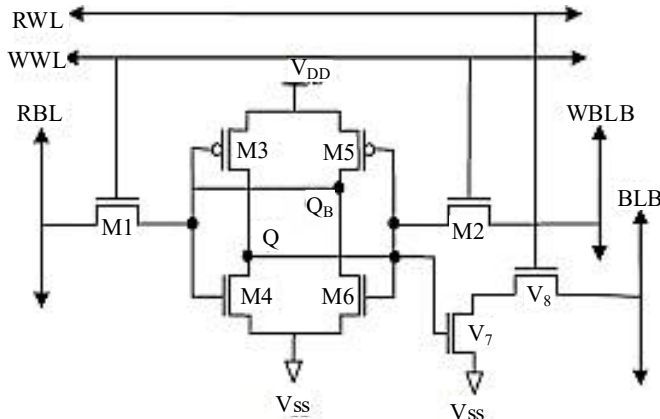


Figure 2. Architecture of 8T SRAM Cell.

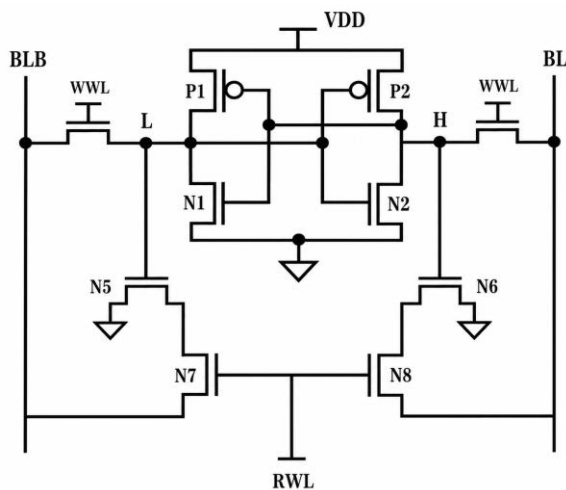


Figure 3. Architecture of 10T SRAM Cell.

His cell operates as:

- *Hold operation (Static state):* During the hold operation, all word lines and assist control signals remain deselected, preserving the feedback connection between the cross-coupled inverters. The stored data are retained securely in the storage nodes, whereas both the read and write assist paths remain inactive.
- *Read operation (Fetching data):* In the read operation, the read bit line is precharged, and the read word line is asserted. The stored data control the discharge of the read bit line through a dedicated and isolated read path, allowing the data to be sensed without disturbing the internal storage nodes. This ensures a stable read access during memory operations.
- *Write operation (Changing data):* write operation in a 10T SRAM cell is carried out by asserting the write word line and activating the write-assist circuitry. The assist transistors temporarily weaken or interrupt the feedback of the cross-coupled inverters, enabling the bit-line drivers to efficiently overwrite the stored data. Once the write operation is completed, the assist signals are dissipated to restore the normal cell operation [9, 10].

ARCHITECTURAL AND OPERATIONAL COMPARISON OF 6T, 8T, AND 10T SRAM CELLS

The 6T SRAM cell has traditionally been the standard memory architecture in CMOS technologies because of its compact layout, high storage density, and minimal transistor count. At higher technology nodes, it offers a favorable balance between power consumption, speed, and silicon cost, leading to its widespread adoption in system-on-chip designs and commercial processors. However, as technology

scales to nodes such as 28 nm, the 6T architecture faces significant challenges because of increased device variability, reduced supply voltage, and higher leakage currents. During read operations, the direct coupling between the storage nodes and precharged bit-lines leads to read disturbance effects and degradation of the read static noise margin, whereas write operations suffer from a limited voltage margin and strong inverter feedback, restricting reliable data overwriting under low-voltage conditions.

To mitigate the read stability issues associated with the 6T cell, the 8T SRAM architecture introduces a decoupled read path by incorporating a dedicated read circuit controlled by an independent read word line. This structural modification separates the storage nodes from the read bit line during read access, allowing data to be sensed without disturbing the stored value, thereby improving the read reliability at scaled technology nodes. Despite these improvements, the write operation in the 8T cell remains similar to that in the 6T architecture and continues to be influenced by the transistor strength ratios at reduced supply voltages. Additionally, the increased transistor count results in area and leakage overheads, which can limit the achievable memory density.

The 10T SRAM cell further enhances memory robustness by addressing both read and write reliability through the inclusion of decoupled read circuitry and write assist mechanisms. Auxiliary transistors temporarily modify the feedback strength of the storage inverters during write operations, enabling reliable data updates, even under aggressive voltage scaling and process variations. Although the 10T architecture provides improved tolerance to process, voltage, and temperature variations, these benefits are achieved at the cost of increased area, design complexity, and additional control signals.

Overall, the continued use of 6T, 8T, and 10T SRAM architectures reflects the inherent trade-offs in scaled memory design rather than a linear replacement trend. Each architecture serves a distinct design objective, and the selection among them is guided by system-level requirements, such as area efficiency, power budget, operating voltage, and reliability constraints at the 28 nm technology node.

QUANTITATIVE COMPARISON OF SRAM CELLS AT 28 NM CMOS (RESEARCH DATA)

Here, we present 28 nm CMOS SRAM-specific quantitative results obtained by a detailed analysis of various published and practical resources.

Static Noise Margin (SNM / Stability)

At the 28 nm technology node, the conventional 6T SRAM cell exhibits the lowest read static noise margin (RSNM) and write static noise margin (WSNM) among the commonly used SRAM architectures, as shown in Table 1. This limitation primarily arises from the use of shared-access transistors, which are responsible for both read and write operations. During a read operation, the internal storage nodes are directly connected to the precharged bit lines through access transistors. This direct coupling can introduce voltage disturbances at the storage nodes, leading to a phenomenon known as a read disturbance. As technology scales and the supply voltage is reduced, the impact of device mismatch and process variability becomes more significant, further degrading the RSNM and making the cell more vulnerable to data instability during read access.

To overcome these challenges, the 8T SRAM cell introduces a dedicated decoupled read port that separates the read path from the internal storage nodes. This architectural modification ensures that the stored data are not directly affected by the read bit-line during read operations. Consequently, the read-disturb problem is effectively eliminated, leading to a substantial improvement in the RSNM at the 28 nm technology under low supply voltage conditions. However, the write operation in the 8T SRAM cell remains largely similar to that of the conventional 6T architecture, in which the bit-line drivers must still overpower the cross-coupled inverter feedback to change the stored data. Consequently, the improvement in the WSNM is relatively limited, particularly when aggressive voltage scaling is applied.

The 10T SRAM architecture further enhances memory stability and reliability by incorporating additional assist and control transistors that provide nodes. The decoupled read mechanism also enhances

the overall read reliability of the memory cell, particularly with regard to control over both read and write operations. These assist mechanisms strengthen the isolation of the read path while temporarily weakening the feedback of the cross-coupled inverters during write operations. This approach reduces the difficulty of overwriting the stored data and significantly improves the write margin. As a result, the 10T SRAM cell demonstrates improved RSNM and WSNM compared to both the 6T and 8T architectures. These architectural enhancements enable reliable SRAM operation even under low supply voltages and high process variability conditions, which are common challenges in deeply scaled technologies such as 28 nm technology nodes. Consequently, the 10T architecture is often considered a robust solution for modern low-power, variation-tolerant memory systems.

Minimum Operating Voltage

At the 28 nm technology node, the minimum operating voltage ($V_{\min}$) of conventional 6T SRAM cells, as shown in Table 2, is limited by severe read disturbance and write failures, typically constraining reliable operation to relatively higher supply voltages. The introduction of a decoupled read path in 8T SRAM cells significantly relaxes the read stability constraints, allowing the cell to function correctly at lower supply voltages compared to 6T designs. In 10T SRAM cells, additional write-assist and control transistors further improve both the read and write margins, enabling reliable operation under aggressive voltage scaling. Consequently, many 8T and 10T SRAM designs at 28 nm have demonstrated stable operation at near-threshold or sub-threshold supply voltages in the range of approximately 0.25–0.4 V, which is not feasible for conventional 6T architectures.

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Table 1. Static noise margin of SRAM cells at 28nm.

Metric	6T (28 nm)	8T (28 nm)	10T (28 nm)	Conclusion
Read Static Noise Margin (RSNM)	Lower (baseline)	Higher than 6T	Expected highest	8T has improved noise margin due to the decoupled read port at 28 nm.
Hold / Write Static Noise Margin (WSNM)	Baseline	Not clearly reported for 28 nm	Expected higher than 6T	10T variants typically include write-assist, improving WSNM.
SNM behaviour w.r.t voltage (trend)	Poorer at low VDD	Better at low VDD	Best for wide VDD	8T decoupled read improves low-V stability; 10T adds further redundancy.

Table 2. Minimum operating voltage ($V_{\min}$) of SRAM cells at 28 nm.

Cell type	Minimum oper. voltage (V)	Conclusion
6T	~0.6–0.8 V (fails below ~0.5 V)	Standard 6T baseline at 28 nm (stability limited).
8T	Successful reads down to ~0.25 V	Ultra8T SRAM demonstrated in 28 nm with read operations at 0.25 V .
10T	Lower than 6T (often ~0.3–0.4 V in near-threshold designs)	10T literature in other nodes shows low $V_{\min}$ capability with assist techniques.

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10T	Lower than 6T (often ~0.3–0.4 V at near-threshold designs)	10T literature in other technology nodes shows low $V_{\min}$ capability with assist techniques.

Table 4. Read/write stability and speed (Qualitative at 28 nm).

Metric	6T	8T	10T	Conclusion
Read Disturb	High	Eliminated (decoupled port)	Eliminated + robust read assist	8T read port decoupling is standard.
Write Stability	Moderate	Same as 6T (shared write)	Improved via feedback cut/assist	10T designs often improve write margin.
Speed (Read/Write)	Baseline	Often faster read	Can be faster with assistance	Assist schemes in 8T/10T improve effective timing.
PVT Tolerance	Lower	Higher than 6T	Highest	More transistors and assist configurations offer better PVT tolerance.

Although the exact micron² values depend on the layout style, the SRAM literature consistently reports a ~20–30% area overhead for 8T cells compared to 6T, with 10T cells present even in higher area sequences owing to the additional transistors. At 28 nm, this increased area directly contributes to a higher total leakage power, as the subthreshold and gate leakage scale with the transistor count. However, the extra transistors in the 8T and 10T architectures enable decoupled read paths and better control techniques, which can reduce dynamic power and improve read stability. In 10T SRAMs, the area overhead is often justified by excessive leakage reduction using power gating or virtual VDD schemes, making them suitable for low-power applications despite their larger cell size.

Read/Write Stability and Speed

The 6T cell suffers from read disturbance and limited PVT tolerance owing to shared read–write paths. The 8T architecture eliminates read disturbance through port decoupling, improving read stability and speed while maintaining a write behavior similar to that of the 6T. The 10T cell further enhances reliability by incorporating assistive mechanisms that improve the write stability, speed, and PVT tolerance. Overall, higher-transistor SRAM cells trade area for significantly improved stability and variability resilience at advanced nodes, such as 28 nm. Table 4 shows the Read/Write Stability and Speed (qualitative at 28 nm).

CONCLUSION AND FUTURE SCOPE

Based on the comparative analysis of 6T, 8T, and 10T SRAM cells at the 28 nm technology node, it is evident that the SRAM design increasingly prioritizes stability and variability tolerance over the minimal transistor count. The conventional 6T cell, while area-efficient, suffers from read disturbance, limited noise margins, higher sensitivity to PVT variations, and a higher minimum operating voltage. The 8T architecture addresses major read stability issues by decoupling the read path, significantly improving the RSNM, and enabling lower-voltage operation, albeit with modest area and leakage overhead. The 10T cell further enhances both read and write robustness through additional assist and control transistors, achieving the highest RSNM, WSNM, and PVT tolerances among the three. These architectural enhancements allow reliable operation closer to near-threshold or subthreshold voltages, which is critical for low-power applications.

Although 8T and 10T cells incur area penalties and potential leakage owing to extra transistors, advanced techniques such as assist circuits and power gating effectively mitigate these drawbacks. Overall, the choice of SRAM topology at 28 nm represents a trade-off between density, power, and

reliability, with 8T and 10T designs being more suitable for low-voltage and variation-aware systems, whereas 6T remains relevant for high-density, performance-oriented memory arrays.

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