

Unified Mathematical Framework for Semiconductor Devices, Junction Dynamics, and Circuit Analysis

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Abstract

Semiconductor devices form the fundamental building blocks of modern electronic and integrated circuit systems, where their electrical behavior is governed by coupled carrier transport, electrostatic, and circuit-level phenomena. This work presents a unified mathematical framework for modeling semiconductor devices, junction dynamics, and their interaction with electronic circuits. The formulation integrates fundamental semiconductor relations, carrier concentration, drift–diffusion transport, Poisson’s equation, continuity equations, PN-junction behavior, diode characteristics, bipolar junction transistor operation, and MOSFET charge-controlled dynamics. The framework further establishes mathematical relationships between device-level parameters and circuit-level voltage, current, power, switching, and frequency responses. Nonlinear device characteristics are incorporated to represent practical operating conditions, including recombination, generation, parasitic effects, temperature dependence, and transient behavior. The proposed formulation provides a systematic basis for deriving analytical and numerical models applicable to rectifiers, amplifiers, switching circuits, CMOS structures, and integrated semiconductor systems. The resulting mathematical framework enables consistent prediction of device characteristics and circuit performance while providing a foundation for advanced semiconductor-device optimization and reliability analysis.

Keywords: Semiconductor devices; PN-junction dynamics; Carrier transport; mathematical modeling; circuit analysis; nonlinear device characteristics.

INTRODUCTION

Semiconductor devices are the fundamental elements of modern electronic systems, enabling the controlled manipulation of electrical charge, current, voltage, and energy through the engineered properties of semiconductor materials and junction structures. Mathematical modeling of these devices provides a systematic means of representing their electrical behavior, predicting their operating characteristics, and establishing relationships between microscopic carrier phenomena and macroscopic circuit responses. Semiconductor operation is primarily governed by carrier concentration, mobility, electric field, diffusion, recombination, generation, and electrostatic potential, which can be represented

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Received Date: September 09, 2026
Accepted Date: September 10, 2026
Published Date: September 12, 2026

Citation: Bibhu Prasad Ganthia. Unified Mathematical Framework for Semiconductor Devices, Junction Dynamics, and Circuit Analysis. Journal of Semiconductor Devices and Circuits. 2026; 13(2): 37–47p.

by coupled mathematical relationships involving Poisson’s equation, carrier continuity equations, and drift–diffusion transport equations. These fundamental equations provide the basis for describing the charge distribution and current flow in semiconductor regions under equilibrium and non-equilibrium conditions. PN junctions introduce nonlinear voltage–current characteristics that can be mathematically modeled through depletion-region analysis, built-in potential, carrier injection, diffusion, and junction capacitance. Similarly, bipolar junction transistors and metal–oxide–semiconductor field-effect transistors require

coupled mathematical formulations to describe charge control, current amplification, channel formation, threshold behavior, and dynamic switching. At the circuit level, semiconductor models must be integrated with Kirchhoff's voltage and current laws to establish complete mathematical representations of rectifiers, amplifiers, switching circuits, logic gates and integrated electronic systems. Practical device behavior also depends on temperature, parasitic resistance and capacitance, leakage mechanisms, mobility variation, and high-field effects, requiring extended nonlinear models for accurate representation. Therefore, a unified mathematical framework provides an important foundation for connecting semiconductor material properties, junction-level dynamics, device characteristics, and circuit-level performance within a consistent analytical structure. Such modeling facilitates parameter extraction, steady-state and transient analyses, sensitivity evaluation, numerical simulations, and device optimization. The development of unified mathematical formulations is particularly important for advanced semiconductor technologies, where increased integration, higher switching frequencies, reduced dimensions, and nonlinear operating conditions demand accurate predictions of electrical behavior. Accordingly, this study develops a systematic mathematical modeling framework for semiconductor devices, junction dynamics, and associated circuits, emphasizing the fundamental governing equations, coupled device relationships, nonlinear characteristics, and circuit-level mathematical representations.

Figure 1 presents a structured mathematical framework connecting semiconductor physics with device and circuit behavior. The framework begins with the fundamental parameters, carrier concentrations, electrostatics, drift-diffusion transport, and continuity equations. These formulations support PN-junction dynamics involving the depletion width, capacitance, carrier diffusion, and nonlinear junction current. The framework then develops mathematical models for diodes, BJTs, and MOSFETs, including parasitic and temperature effects models. Circuit-level modeling integrates KCL, KVL, small-signal, transient, frequency-domain, and nonlinear analyses. Finally, the framework supports rectifiers, amplifiers, switching circuits, integrated circuits, power electronics, validation, and optimization through iterative-model refinement.

Semiconductor device modeling has been extensively developed to describe carrier transport, junction behavior, and electrical characteristics using physics-based mathematical equations. Sze et al. presented comprehensive models of semiconductor materials, PN junctions, diodes, transistors, and charge transport mechanisms, establishing fundamental relationships for device analysis [1]. Neamen emphasized carrier concentration, drift, diffusion, and equilibrium conditions as essential components of mathematical modeling of semiconductors [2]. Pierret developed analytical formulations for semiconductor device fundamentals, including junction electrostatics and minority carrier transport [3]. Selberherr introduced numerical approaches for analyzing semiconductor devices using coupled physical equations and computational methods [4]. Schroder examined mathematical characterization techniques for extracting semiconductor material and device parameters from the measured electrical behavior [5]. Streetman and Banerjee provided device-level formulations for PN junctions, BJTs, MOS structures, and their operating characteristics [6]. Taur and Ning developed advanced mathematical models for MOS devices and scaling effects relevant to modern integrated circuits [7]. Sedra et al. established systematic circuit-level models connecting semiconductor device equations with amplifier, switching, and analog circuit behaviors [8]. Razavi further developed analytical small- and large-signal models for semiconductor circuits, emphasizing the gain, frequency response, and nonlinear operation [9]. Chattopadhyay and Rakshit presented mathematical approaches for electronic circuits and semiconductor components, supporting the systematic analysis of practical circuit configurations [10]. Collectively, these studies establish a strong theoretical foundation for unified mathematical modeling, while further integration of device physics, junction dynamics, transient behavior, and circuit-level equations can provide a more comprehensive framework for semiconductor analyses.

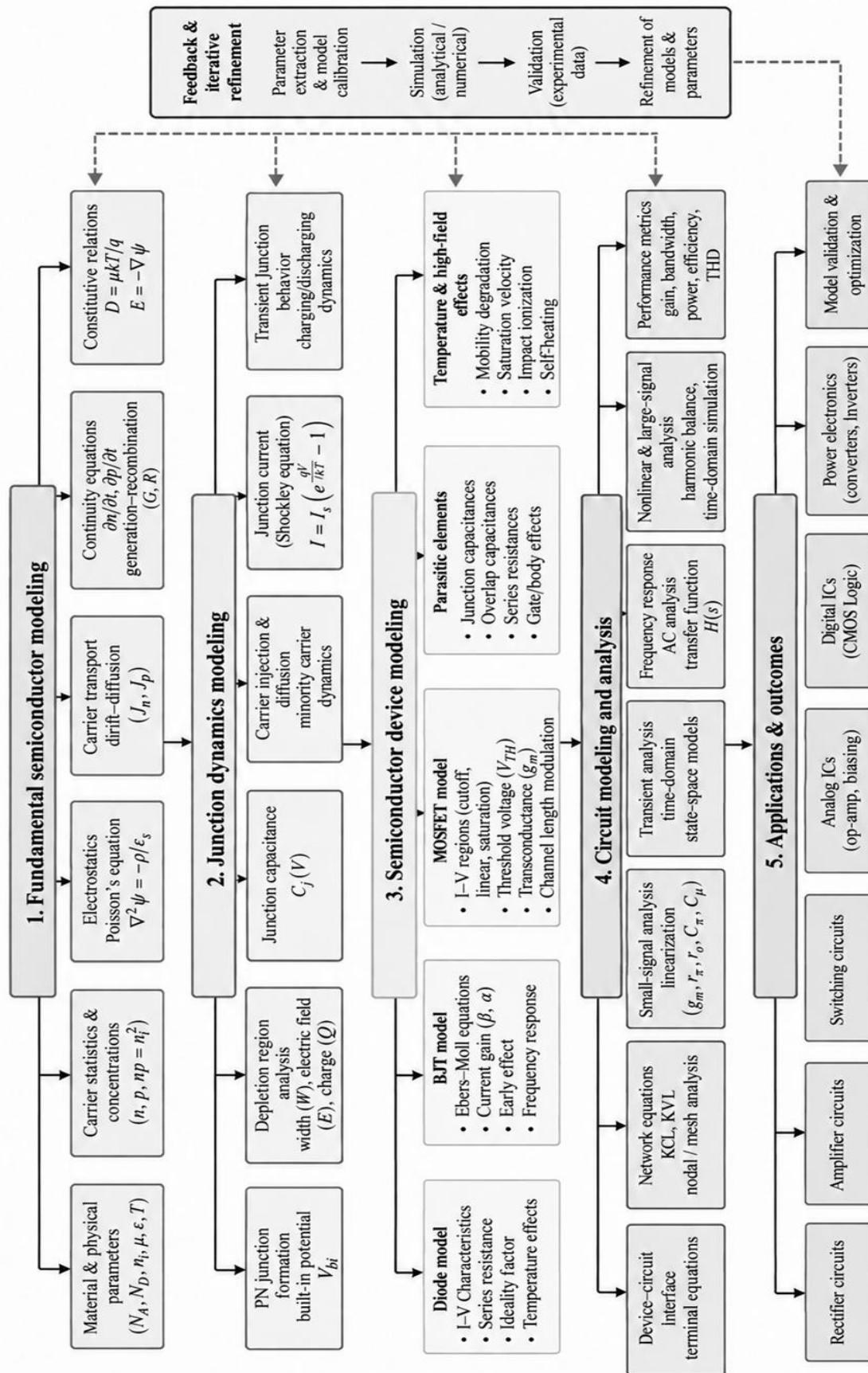


Figure 1. Unified mathematical framework for semiconductor devices, junction dynamics, and circuit analysis.

FUNDAMENTAL MATHEMATICAL MODELING OF SEMICONDUCTOR DEVICES

The fundamental mathematical modeling of semiconductor devices begins with the description of charge carriers, electrostatic potential, and carrier transport within a semiconductor material [2]. Let n and p represent the electron and hole concentrations, respectively, while N_D and N_A denote the donor and acceptor concentrations. Under thermal equilibrium, the intrinsic carrier relationship is expressed as:

$$np = n_i^2$$

where n_i is the intrinsic carrier concentration. For a doped semiconductor, charge neutrality can be expressed as

$$p + N_D = n + N_A$$

and, for a nondegenerate semiconductor,

$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

$$p = n_i \exp\left(\frac{E_i - E_F}{kT}\right)$$

where E_F is the Fermi level, E_i is the intrinsic energy level, k is Boltzmann's constant, and T is the absolute temperature.

The spatial distribution of electric potential is governed by Poisson's equation,

$$\nabla^2 \psi = -\frac{\rho}{\epsilon_s}$$

where ψ is the electrostatic potential, ϵ_s is the semiconductor permittivity, and the net charge density is

$$\rho = q(p - n + N_D^+ - N_A^-).$$

The electron and hole current densities are represented through drift and diffusion mechanisms as

$$J_n = q\mu_n nE + qD_n \nabla n$$

$$J_p = q\mu_p pE - qD_p \nabla p$$

where μ_n, μ_p are the carrier mobilities, and D_n, D_p are the diffusion coefficients. The electric field is related to the potential by

$$E = -\nabla \psi.$$

The Einstein relationships establish the connection between diffusion coefficients and carrier mobility:

$$D_n = \frac{kT}{q} \mu_n, \quad D_p = \frac{kT}{q} \mu_p.$$

Carrier conservation is described by the continuity equations,

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n + G_n - R_n$$

and

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p + G_p - R_p$$

where G and R represent the carrier generation and recombination rates, respectively. For recombination through the carrier lifetime, a simplified model is expressed as

$$R_n = \frac{n - n_0}{\tau_n}, \quad R_p = \frac{p - p_0}{\tau_p}.$$

For a one-dimensional semiconductor structure, the complete device model can therefore be expressed through a coupled Poisson–drift–diffusion system as follows:

$$\begin{cases} \frac{d^2 \psi}{dx^2} = -\frac{q}{\epsilon_s} (p - n + N_D^+ - N_A^-), \\ J_n = q\mu_n nE + qD_n \frac{dn}{dx}, \\ J_p = q\mu_p pE - qD_p \frac{dp}{dx}, \\ \frac{\partial n}{\partial t} = \frac{1}{q} \frac{dJ_n}{dx} + G_n - R_n, \\ \frac{\partial p}{\partial t} = -\frac{1}{q} \frac{dJ_p}{dx} + G_p - R_p. \end{cases}$$

This coupled formulation provides a fundamental mathematical basis for modeling PN junctions, diodes, bipolar junction transistors, MOSFETs, and semiconductor-based electronic circuits [3].

UNIFIED MATHEMATICAL MODELING OF JUNCTION DYNAMICS AND DEVICE CHARACTERISTICS

Mathematical modeling of semiconductor junction dynamics establishes a unified relationship between the electrostatic potential, carrier transport, charge distribution, and terminal electrical characteristics. For a PN junction under equilibrium, the built-in potential is determined by the carrier concentrations as follows:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

where N_A and N_D are the acceptor and donor concentrations, respectively. The depletion width under an applied junction voltage V_J is expressed as:

$$W_J = \sqrt{\frac{2\epsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_{bi} - V_J)}$$

for the reverse-bias convention $V_J < V_{bi}$. The depletion capacitance consequently becomes

$$C_J = \frac{\epsilon_s A}{W_J}$$

where A is the junction cross-sectional area. Carrier diffusion across the junction produces the fundamental diode current, which is represented by the Shockley equation as follows:

$$I_D = I_S \left[\exp \left(\frac{qV_D}{nkT} \right) - 1 \right]$$

where I_S is the reverse saturation current, and n is the ideality factor. Including the series resistance yields the implicit terminal relationship:

$$V_D = nV_T \ln \left(1 + \frac{I_D}{I_S} \right) + I_D R_S$$

where $V_T = kT/q$ is the thermal voltage.

The dynamic junction current includes capacitive effects and can be represented by

$$I_J = I_D + C_J \frac{dV_J}{dt}.$$

For transient carrier behavior, the excess minority-carrier concentration satisfies

$$\frac{\partial \Delta n}{\partial t} = D_n \frac{\partial^2 \Delta n}{\partial x^2} - \frac{\Delta n}{\tau_n}$$

with corresponding hole dynamics

$$\frac{\partial \Delta p}{\partial t} = D_p \frac{\partial^2 \Delta p}{\partial x^2} - \frac{\Delta p}{\tau_p}.$$

The associated diffusion lengths are

$$L_n = \sqrt{D_n \tau_n}, \quad L_p = \sqrt{D_p \tau_p}.$$

For a bipolar junction transistor, the collector current can be approximated by

$$I_C = \beta I_B + I_{CEO}$$

and the emitter current satisfies

$$I_E = I_C + I_B.$$

The transistor current gain is therefore

$$\beta = \frac{I_C}{I_B},$$

while the common-base gain is

$$\alpha = \frac{I_C}{I_E} = \frac{\beta}{1 + \beta}.$$

For a MOSFET operating in the saturation region, the ideal drain current is

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

where W/L is the channel aspect ratio, C_{ox} is oxide capacitance per unit area, and V_{TH} is the threshold voltage. Incorporating channel length modulation yields

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}).$$

The threshold voltage can further be modeled as

$$V_{TH} = V_{TH0} + \gamma [\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}]$$

where γ is the body-effect coefficient, and ϕ_F is the Fermi potential. Thus, the unified junction-device formulation can be summarized by the coupled state vector as follows:

$$x = [\psi, n, p, V_J, Q_J, I_D, I_B, I_C]^T$$

and its dynamic evolution as

$$\dot{x} = F(x, u, T, N_A, N_D, \mu, D, \tau)$$

where u represents the applied electrical input. This formulation links junction electrostatics and carrier dynamics directly to measurable device characteristics, providing a common mathematical foundation for diode, BJT, and MOSFET modeling under steady-state and transient operating conditions. [4].

MATHEMATICAL MODELING AND ANALYSIS OF SEMICONDUCTOR CIRCUITS

Semiconductor circuit modeling establishes a mathematical relationship between the individual device characteristics and the overall electrical behavior of electronic networks [5]. Once the voltage–current characteristics of semiconductor devices are obtained, they can be incorporated into circuit equations using Kirchhoff’s current law (KCL), Kirchhoff’s voltage law (KVL), impedance relationships and device-specific nonlinear constitutive equations. For a general semiconductor circuit containing N nodes and B branches, the node current relationship is expressed as

$$\sum_{k=1}^B a_{ik} I_k = 0, \quad i = 1, 2, \dots, N \quad (1)$$

where a_{ik} is the branch-node incidence coefficient, and I_k is the current through branch k . Similarly, the voltage relationship around an independent circuit loop is expressed as

$$\sum_{k=1}^B b_{jk} V_k = 0, \quad j = 1, 2, \dots, L \quad (2)$$

where b_{jk} represents the loop-branch relationship.

For a nonlinear semiconductor device, the terminal current can generally be represented as

$$I = f(V, x, T) \quad (3)$$

where V is the terminal voltage, x represents the internal device states, and T is the temperature. For a diode connected to a resistive load, the circuit equation is

$$\frac{V_S - V_D}{R_L} = I_S \left[\exp\left(\frac{V_D}{nV_T}\right) - 1 \right] \quad (4)$$

with

$$V_T = \frac{kT}{q}. \quad (5)$$

For small-signal analysis around an operating point (V_{D0}, I_{D0}) , the diode dynamic conductance is

$$g_d = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_{D0}} = \frac{I_{D0}}{nV_T}. \quad (6)$$

The corresponding incremental resistance is

$$r_d = \frac{1}{g_d} = \frac{nV_T}{I_{D0}}. \quad (7)$$

For an amplifier circuit, the voltage gain is defined as

$$A_v = \frac{v_o}{v_i} \quad (8)$$

and the current gain is

$$A_i = \frac{i_o}{i_i}. \quad (9)$$

The power gain is consequently

$$A_p = \frac{P_o}{P_i} = A_v A_i. \quad (10)$$

For a transistor-based circuit, the small-signal hybrid relationship can be expressed as

$$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}. \quad (11)$$

For a MOSFET operating in saturation, the drain current is modeled by

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}). \quad (12)$$

The corresponding transconductance is

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) (1 + \lambda V_{DS}). \quad (13)$$

The output resistance caused by channel-length modulation is approximately

$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \approx \frac{1}{\lambda I_D}. \quad (14)$$

For a common-source amplifier, the approximate voltage gain is

$$A_v \approx -g_m (R_D \parallel r_o \parallel R_L). \quad (15)$$

The frequency response of a semiconductor circuit can be represented using its transfer function,

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{N(s)}{D(s)}. \quad (16)$$

For a first-order RC network,

$$H(s) = \frac{1}{1 + sR_{eq}C_{eq}} \quad (17)$$

and its cutoff frequency is

$$f_c = \frac{1}{2\pi R_{eq}C_{eq}}. \quad (18)$$

The dynamic behavior of a semiconductor circuit containing capacitive and inductive elements can be formulated in the state-space form as follows:

$$\dot{x} = Ax + Bu + F(x, u) \quad (19)$$

$$y = Cx + Du. \quad (20)$$

Here, x denotes the circuit state, u represents the input signals, and y denotes the circuit output. The nonlinear term F accounts for the semiconductor device nonlinearities. The circuit power is obtained from

$$P(t) = v(t)i(t) \quad (21)$$

and the average power over one operating interval T_0 is

$$P_{avg} = \frac{1}{T_0} \int_0^{T_0} v(t)i(t) dt. \quad (22)$$

For periodic signals, the RMS voltage and current are

$$V_{rms} = \sqrt{\frac{1}{T_0} \int_0^{T_0} v^2(t) dt} \quad (23)$$

$$I_{rms} = \sqrt{\frac{1}{T_0} \int_0^{T_0} i^2(t) dt}. \quad (24)$$

Therefore, the complete mathematical model of a semiconductor circuit can be expressed compactly as

$$F(x, \dot{x}, u, y, T, \theta) = 0 \quad (25)$$

where θ contains semiconductor and circuit parameters, such as mobility, threshold voltage, junction capacitance, resistance, channel dimensions, and device gains. This unified formulation provides a mathematical foundation for the steady-state, transient, small-signal, frequency-domain, nonlinear, and power-performance analyses of semiconductor circuits [4].

Semiconductor circuit modeling establishes mathematical relationships between individual device characteristics and the overall electrical behavior of electronic networks, where the circuit containing N nodes and B branches can be governed by Kirchhoff's Current Law (KCL), $\sum_{k=1}^B a_{ik} I_k = 0$, in which a_{ik} denotes the branch-node incidence coefficient and I_k represents the current through branch k , while Kirchhoff's Voltage Law (KVL) is expressed as $\sum_{k=1}^B b_{jk} V_k = 0$, where b_{jk} is the loop-branch coefficient and V_k is the branch voltage. The nonlinear terminal behavior of a semiconductor device can be represented by $I = f(V, x, T)$, where I is the terminal current, V is the terminal voltage, x is the internal state vector, and T is the absolute temperature [7]. For a diode-resistive circuit, the current relationship is $\frac{V_S - V_D}{R_L} = I_S [\exp(V_D/nV_T) - 1]$, where V_S is the source voltage, V_D is the diode voltage, R_L is the load resistance, I_S is the saturation current, n is the ideality factor, and $V_T = kT/q$ is the thermal voltage. Around an operating point, the diode dynamic conductance is $g_d = I_{D0}/(nV_T)$, with I_{D0} denoting the operating-point current, and the incremental resistance is $r_d = 1/g_d$. For MOSFET modeling, the saturation-region drain current is $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$, where μ_n is electron mobility, C_{ox} is oxide capacitance, W/L is channel aspect ratio, V_{GS} is gate-source voltage, V_{TH} is threshold voltage, V_{DS} is drain-source voltage, and λ is channel-length modulation coefficient. The transconductance is $g_m = \partial I_D / \partial V_{GS}$, while the output resistance is approximately $r_o = 1/(\lambda I_D)$. For an amplifier, the voltage gain is $A_v = v_o/v_i$, current gain is $A_i = i_o/i_i$, and power gain is $A_p = A_v A_i$, where subscripts i and o denote input and output quantities. The circuit frequency behavior is described using $H(s) = V_o(s)/V_i(s)$, where $H(s)$ is the transfer function and s is the complex frequency. Dynamic semiconductor circuits can be represented by $\dot{x} = Ax + Bu + F(x, u)$ and $y = Cx + Du$, where x , u , and y denote the state, input, and output vectors, respectively, while A , B , C , and D are system matrices, and F represents nonlinear device effects. The circuit power is calculated as $P(t) = v(t)i(t)$, providing a direct mathematical basis for evaluating the semiconductor circuit efficiency, dynamic response, and electrical performance [9].

The developed mathematical framework demonstrates that semiconductor device and circuit behavior can be represented through a unified nonlinear formulation in which carrier transport, junction electrostatics, device constitutive relationships, circuit constraints, dynamic states, and operating conditions are mathematically coupled. A comprehensive representation of the proposed framework is as follows:

Here, ψ is the electrostatic potential, n and p are the electron and hole concentrations, respectively, q is the electronic charge, ϵ_s is the semiconductor permittivity, N_D^+ and N_A^- are the ionized donor and acceptor concentrations, respectively, J_n and J_p are the electron and hole current densities, respectively, G and

R denote the generation and recombination rates, respectively, μ represents the carrier mobility, D denotes the diffusion coefficient, E is the electric field, I_D is the device current, V_D is the diode voltage, I_S is the saturation current, V_T is the thermal voltage, C_{ox} is the oxide capacitance, W/L is the channel aspect ratio, V_{GS} and V_{DS} are the terminal voltages, V_{TH} is the threshold voltage, and λ is the channel-length modulation coefficient. The principal finding is that these physical equations can be simultaneously constrained by circuit-level KCL and KVL relationships, allowing device-level nonlinearities to propagate directly into circuit-level voltage, current, power, and dynamic responses [8]. The complete dynamic representation can be further formulated as

$$\dot{x} = Ax + Bu + F_{nl}(x, u, T, \theta), \quad y = Cx + Du \quad (27)$$

where x is the state vector, u is the input vector, y is the output vector, θ contains semiconductor and circuit parameters, and F_{nl} represents nonlinear device effects. The novelty of the framework lies in integrating semiconductor physics, junction dynamics, diode behavior, transistor characteristics, and circuit equations into a mathematically consistent formulation, rather than analyzing each layer independently. An additional performance relationship is obtained as follows:

$$\mathcal{P} = w_1 \|y - y_{ref}\|_2^2 + w_2 \int_0^{t_f} \|\dot{y}(t)\|_2^2 dt + w_3 P_{loss} + w_4 \|\theta - \theta_0\|_2^2 \quad (28)$$

where w_1, w_2, w_3, w_4 are weighting coefficients, y_{ref} is the desired response, P_{loss} is the circuit power loss, and t_f is the analysis interval. This formulation provides a mathematical basis for simultaneously evaluating the accuracy, dynamic stability, power performance, and parameter sensitivity, thereby making the framework suitable for advanced semiconductor device modeling, circuit simulation, optimization, and design [10].

CONCLUSION

The unified mathematical framework developed in this study provides a systematic representation of semiconductor devices, junction dynamics, and semiconductor circuit behavior through interrelated physical and electrical relationships. The modeling begins with fundamental semiconductor parameters, including electron and hole concentrations, doping densities, carrier mobility, diffusion coefficients, electrostatic potential, and temperature, and establishes their relationships using Poisson's equation, carrier continuity equations, and drift-diffusion transport equations. The mathematical treatment of PN junctions further incorporates built-in potential, depletion width, junction capacitance, carrier diffusion, and nonlinear diode current-voltage characteristics, enabling the representation of both steady-state and transient junction behaviors. The framework is extended to transistor-level characteristics through mathematical formulations of the BJT current gain, collector and emitter currents, MOSFET drain current, transconductance, threshold voltage, and channel length modulation. At the circuit level, semiconductor device equations are integrated with Kirchhoff's voltage and current laws to establish nonlinear network models suitable for rectifier, amplifier, switching, and integrated circuit analysis. Small-signal parameters, transfer functions, frequency response, power relationships, root mean square (RMS) quantities, and state-space representations provide additional mathematical tools for analyzing circuit performance under different operating conditions. The resulting formulation demonstrates that device-level physical parameters can be systematically connected to terminal electrical quantities and, ultimately, to circuit-level performance indicators. Therefore, the unified model provides a mathematical foundation for analytical derivation, numerical simulation, parameter estimation, transient analysis, frequency-domain analysis, and semiconductor circuit optimization. Its modular structure also allows additional physical effects, including temperature variation, parasitic elements, leakage current, recombination, and high-field phenomena, to be incorporated without changing the fundamental modeling architecture. Overall, the developed mathematical framework establishes a coherent pathway from semiconductor material physics to junction behavior, device characteristics, and circuit response, supporting the accurate and scalable analysis of contemporary semiconductor devices and electronic circuits.

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