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Design and Simulation of Full Adder-Based CMOS 4–2 Compressor Using CMOS XOR-XNOR Logic

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Abstract

This study utilizes the recent development of CMOS transistors to construct an energy-efficient Full adder-based CMOS 4–2 compressor. The CMOS Exclusive-OR-Exclusive-NOR component and multiplexer used in the transmission logic of the novel CMOS compressor include eight transistors. The XOR-XNOR logic style is the most efficient and effective due to its speed and reduced power consumption. Utilizing an operational supply voltage of 0.7 V and 90 nm CMOS technology, the Cadence Virtuoso Tool can ascertain three parameters: the Power-Delay Product (PDP) and the maximum output delay. The proposed CMOS 4–2 compressor's performance was evaluated against existing designs using a 0.7 V supply. Simulation results demonstrate significant improvements in speed, power consumption, and power-delay product. Compared to traditional 4–2 compressors, the new design offers enhanced efficiency and better overall performance. These enhancements make the proposed compressor more suitable for low-power, high-speed applications, highlighting its potential in modern digital systems. The results confirm its superiority over previous designs in key performance parameters under identical operating conditions.

Keywords: Area, CMOS, MIMO diverse full adder, leakage power, leakage current, cadence

INTRODUCTION

High-speed electrical systems are becoming more and more popular and sought-after. It has been a long-standing goal of VLSI designers to construct systems that are both fast and efficient. In high-speed systems, a processing component known as a compressor is often utilized. These high-speed compression devices are becoming more popular and sought after in a broad variety of digital system components, including DSP, DSF, microprocessors, 3-D graphics programs, motion prediction accelerators & more [1]. Partially multiplied products may be reduced by using compressors in the multiplication process [2]. Partially produced products are generated, partially reduced, and partially computed in a multiplication process [3]. This step has an impact on the multiplier's energy consumption & speed. As a way to increase the performance of the multiplier, this step uses high-speed and low-power compressors [4, 5]. Compressors in the 3–2, 4–2, 4–3, 5–2, 5–3, 6–3, 7–2, 7–3, and other configurations have been devised by VLSI engineers [6–8]. The 4–2 compressor's straightforward design and regular connectivity make it a good choice for high-speed digital circuits. An energy-efficient and less-power-consuming 4–2 compressor is given in this study. In an infield of VLSI Designing, the compactness of a chip is necessary to decrease power consumption, area for improving the performance of multimedia devices. Now a day's, battery life is the most concern field in the digital life environment, portability of devices makes our work easier and saves time and money. In such a case it is the major task for the designer to give the expected outcome to the user and make the

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device user-friendly. In an infield of an arithmetic circuit, the multiplexer and adders are the most used component in chip designing. Historically, the multiplier has been used to simplify arithmetic circuits by performing 3 functions: partial product reduction, partial product creation, & addition. As the use of multimedia devices grows, so does the need to properly organize the power and voltage sources. As far as chip design is concerned, multipliers, and adders are the most common power guzzlers. It is common for lower-order compressors like 3–2 and 4–2 compressors to be utilized as standard components in many digital signal processing (DSP) applications. 4:2 compressors have been developed in this work employing a variety of logic types in conjunction with the CMOS logic that is already there. In this proposed 4:2 compressor architecture we can design by using a smaller number of transistors for implementation. We perform the compressor design by using conventional logic styles, which are discussed using these low-power Adders architectures. To decrease the amount of electricity dissipated, we may lower the supply voltage. By lowering the number of transistors, we may minimize and simplify the complexity of circuits in both arithmetic and digital systems by using this strategy. Compressors are employed in multiplier circuits to minimize power consumption and delay because of their ability to simplify complicated calculations. Today, 4–2 and 5–2 compressors are frequently used for high speed and performance multipliers because of the decreased reaction time of the partial product accumulation step. In terms of the structure of regular construction of a Wallace tree with less complexity, the 4–2compressori is the only one. It has been suggested that different 4–2 compressor circuits may be used to reduce power consumption and maximize space efficiency. As CMOS architecture needs a large number of transistors to work at low supply voltage levels, some of them can function at low voltages but require a huge amount, while others are less efficient and can't drive the next level of the systems.

LITERATURE REVIEW

We take reviews from several research papers and various journal and conference papers. We studied the work and the development of the structure with a different technique. In digital system processing the speed of the system is necessary to enhance the performance and get the desired outcome. As we know different types of adders and multiplier are used to construct the 4:2 compressor. In previous many papers use the MUX and the XOR gate for the construction of the Adder circuit to develop FA based 4:2 CMOS Compressor.

Lower-order compressors serve as the primary cell in a variety of arithmetic operations, with partial product summation in multipliers being one of the most common. Veeramachaneni et al. [9], Design of unique 3–2, 4–2, and 5–2-speed compressors with the capacity to operate at low voltages is shown in this study. A comparison of the new compressor to an old one is made in terms of power consumption, total delay, & efficient area, among other things. Design implementations employing XOR and multiplexer are compared in the proposed study to see which is the most efficient. Both output & its inverse are available, however, present compressor designs do not quickly use these outputs. To maximize the efficiency of compressors, outputs are grouped logically in the paper architecture Because of their low power consumption, reduced transistor count, as well as improved delay time, new compressors may be used as a viable design choice.

The hybrid-CMOS logic style uses full adder (FA) by separating it into three modules, Agarwal et al. [10], A variety of levels may be used to create the most effective designs. To begin, this design uses XOR-XNOR circuits, which have a higher driving potential and can provide both full-swing XOR and XNOR outputs at the same time. In addition, it uses less power and has superior delay performance to other alternatives. An XOR-circuit-based second module utilizes the first module's Carry and Sum outputs as inputs, respectively, to produce a Sum result. The first stage's output & other inputs are used to produce a carry output in the third module. We have designed a new FA circuit to address power consumption and overall delay between carrying out to carry in & PDP in the suggested FA design.

In this paper, they use the compressor circuit designed using an arithmetic cell-like full adder. Most VLSI circuit compressors are designed using adders to implement arithmetic circuits, most of the

arithmetic circuits use multipliers & adders. ARSTRAN is a basic tool with the help of this we generate the electrical and physical performance of the proposed architecture. In this paper, Tonfat et al. [11], use the multiplexer cell in place of the gates like XOR and XNOR, And the automated physical layout generated by using the proposed tool. The circuit area power consumption and total delay have been reduced thanks to this tool.

Adders, muxes, and other high-performance arithmetic circuitry are common in DSP systems. When it comes to high-performance circuits, multipliers are a crucial part of the overall circuit design. Power and speed are a problem while using this device. When used in multiplier circuits, compressors play an important role in controlling the total multiplier speed. There are two new high-performance low-logic compressor topologies proposed by Menon et al. [12]. Carry propagation is limited to a single stage in their designs to reduce total transmission time. There are fewer delays in these models as compared to those reported in the literature. Radhakrishnan et al. [13] proposed work paper 4:2 compressor circuit designed by using pass transistor logic for a better result in the performance of the system. In this, the design uses the XOR-XNOR gates and avoid the use of inverter cell. The complete circuit is designed using 28T. Tish work represents many low powers and high-performance cells, to overcome the use of complex circuit architectures. The total voltage is reduced by minimizing the output voltage swings at the nodes in the overall circuits. The performances of most DSP applications depend on the selection of the cells. These papers reduce the most important field in the VLSI system and give the expected results.

Compressor

It is a device for combining many partial items into a single complete one. Figure 1(a) and (b) depicts the 4–2 compressor's block diagram. Cin and M1 are the only two required inputs, whereas Sum, Carry, and Cout are the only three required outputs. There are two compressors, one in the previous lower significant stage, and one in the next higher significant stage, each with different input and output. It is worth noting that the weighting of M1 through M4 is identical to that of M1 through M4 except for carrying, which is weighted one binary bit order higher. The compressor has an advantage over a complete adder since Cout is not reliant on Cin. Figure 1 shows 4–2 compressors having 2 serially linked FAs (Full adders). Four XOR gates provide a critical route delay in this implementation. Equation: A 4–2 compressor must adhere to the following rule:

Many various implementations of the 4–2 compressor have been documented in the literature [6] through [14]. Figure 2 (a–b) depicts two popular topologies for implementing 4-to-2 compressors [6], [9]. XOR gates and multiplexers make up the first (MUX). Three XOR gates make up the critical route delay. XOR-XNOR modules and MUXs are used in the later version, which is based on the earlier version's redesigned architecture. XOR-XNOR and two MUXes are involved in the crucial route delay. The following equations are used to implement these architectures:

$$M_1 + M_2 + M_3 + M_4 + C_{in} = Sum + 2 * (Carry + C_{out})$$

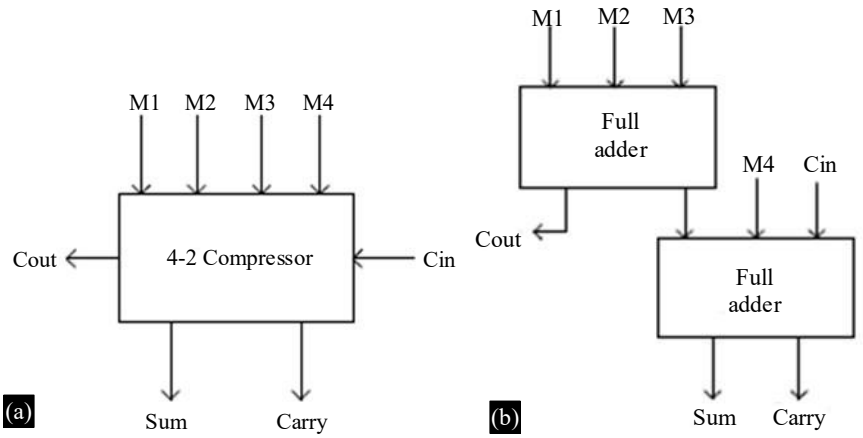

Figure 1. (a) Block diagram, (b) Compressor 4–2 has an FA-based setup.

$$\text{Sum} = M_1 \oplus M_2 \oplus M_3 \oplus M_4 \oplus C_{IN}$$

$$C_{out} = (M_1 \oplus M_2) * M_3 + \overline{M_1 \oplus M_2} * M_1$$

$$Carry = (M_1 \oplus M_2 \oplus M_3 \oplus M_4) * C_{IN} + \overline{M_1 \oplus M_2 \oplus M_3 \oplus M_4} * M_4$$

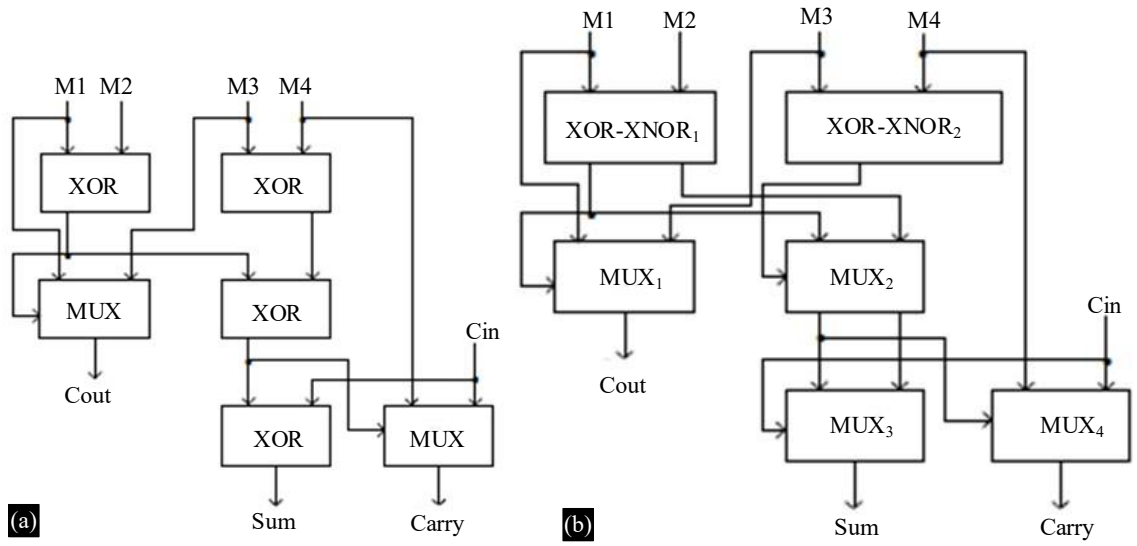

Figure 2. (a) Block diagram using XOR logic style, (b) Block diagram using XOR-XNOR logic style.

A four-to-two compressor in the CMOS logic type is shown in Figure 3. When more transistors are employed, the system uses more power, covers a larger surface, and provides a longer delay. Chang et al. (2007) [7] present 4–2 compressors built entirely on DPL (Double Pass-Transistor Logic). The original architecture was used to construct this high-speed compressor. Before DPL XOR-XNOR modules, XOR gates were utilized instead. These modules create XOR as well as XNOR signals concurrently. Each of the XOR and XNOR select inputs on the multiplexer is linked to an appropriate XOR or XNOR signal for processing. Using an inverter on some of the multiplexer inputs is no longer necessary because of this. Because DPL XOR-XNOR modules need input inverters, which boost switching activity, the compressor consumes more power. The design in Figure 2(b) uses CMOS logic for XOR-XNOR1, 2 modules, and MUX1,3,4 in Veeramachaneni et al. (2007) [9] to construct another 4–2 compressor. The compressor speed is increased by using a transmission gate logic type for MUX2. There is also less power usage since MUXs do not need an additional converter for certain inputs.

The transmission version of MUX and the 10T XOR-XNOR module are used in [11]. Inverters at the MUX are a factor in the increased power usage. This step does not make good use of XNOR & XOR signals, even though they are there. In Kumar and Kumar (2014) [14], a novel 8T XOR-XNOR module is presented, & 4–2 compressor is constructed utilizing the same. Because fewer transistors are utilized, the compressor takes up less space.

Proposed Novel CMOS 4-2 Compessor

This section describes a novel 4–2 compressor architecture using transmission gate logic and 2–8T XOR-XNOR modules & 4 MUXs. According to Tonfat and Reis (2012) [11], an entirely new XNOR gate is suggested. In addition to providing fast speed and complete voltage swing at the output, this XNOR gate also uses less energy. At the XNOR gate's output, an inverter is required for XOR functioning. As a result, the XOR-XNOR module in Figure 4 utilizes a total of eight transistors (a).

The complement of input Y is generated by the inverter of this XOR-XNOR module, which is composed of MP1 & MN1 transistors. The second inverter is controlled by the output of this inverter,

which includes transistors MP2 and MN2. Nearly all of the XNOR function is generated by this second inverter, although it suffers from voltage deterioration when X=0,1 and X=Y=1 are combined [10]. The MP3 and MN3 pass transistors are utilized to prevent the issue from arising. transistors MP1 and MP2 in this module provide a logic high level at the output when X=Y=0 is applied to their respective inputs (XNOR). MP2 and MN1 are switched on, and MN2 and MN3 have a logic low, therefore the output node gets logic low as well when X and Y are both 1 Switching on transistors MN2 and MP1 causes an output node logic low when X=1 and Y=0 is present. All transistors MP3, MN1, MN2, MN3, and the output logic high level are switched on when inputs X=Y=1. Figure 4(b) shows a MUX constructed using transmission gate logic. To create a signal that is opposite of its select input, MUX3 utilizes an inverter. For the Cout generator, a pair of XOR-XNOR modules' outputs are sent into MUX1 and MUX2, respectively. The Carry generator is also connected to MUX2's output and its complement form (MUX4). As a result, the compressor's critical path time and transistor count are reduced by eliminating inverters. Increasing compressor speed while reducing power consumption is accomplished by using correctly sized inverter transistors and appropriately sized transmission gate logic type MUX transistors, respectively [15]. The transistors' widths are provided in brackets in Figure 4. Figure 5 illustrates the circuit design for the proposed 4–2 compressor.

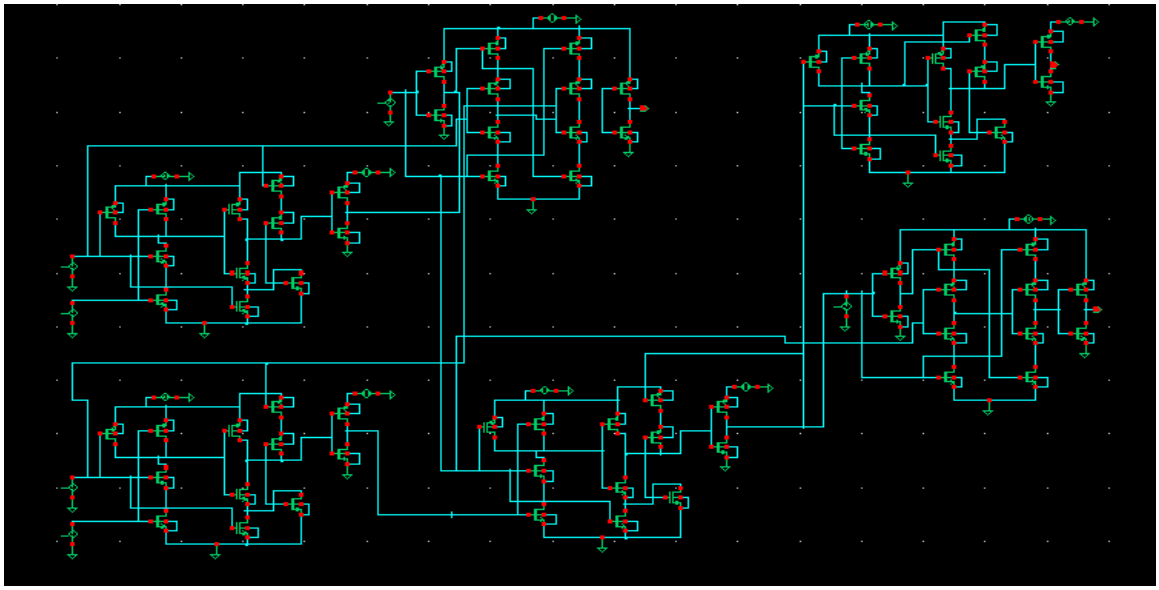

Figure 3. Schematic of a CMOS 4–2 compressor.

Simulation Result and Performance Analysis of Proposed Novel CMOS 4-2 Compressor

Cadence Virtuoso Tool is utilized to do simulations in 90nm CMOS technology. Table 1 lists the proposed compressor's performance characteristics for supply voltages between 0.7 V and 1.2 V. Maximum delay, average consumption, as well as output-delay product are all measured, as shown by the results. Figure 6 illustrates the transient compressor response.

Table 1. Performance parameter comparison between CMOS and proposed CMOS 4–2 compressor.

Performance parameter	CMOS 4–2 compressor	Proposed novel CMOS 4–2 compressor
Technology Used	90 nm	90 nm
Supply Voltage	0.7 V	0.7 V
Low Power	20.4 nW	18.4 nW
Output Delay	80.8 ns	66.9 ns
Power Delay Product (PDP)	1648.32 ns	1230.96 ns
Transistor Count	72	36
Area Used	Large	Small

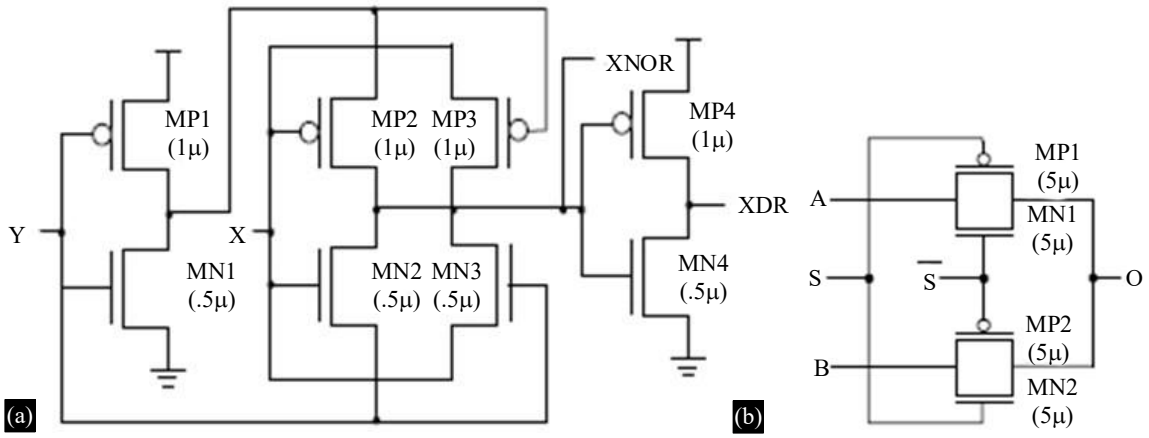

Figure 4. (a) 8Transistor-based XOR-XNOR logic style, (b) Transmission gate logic style based MUX.

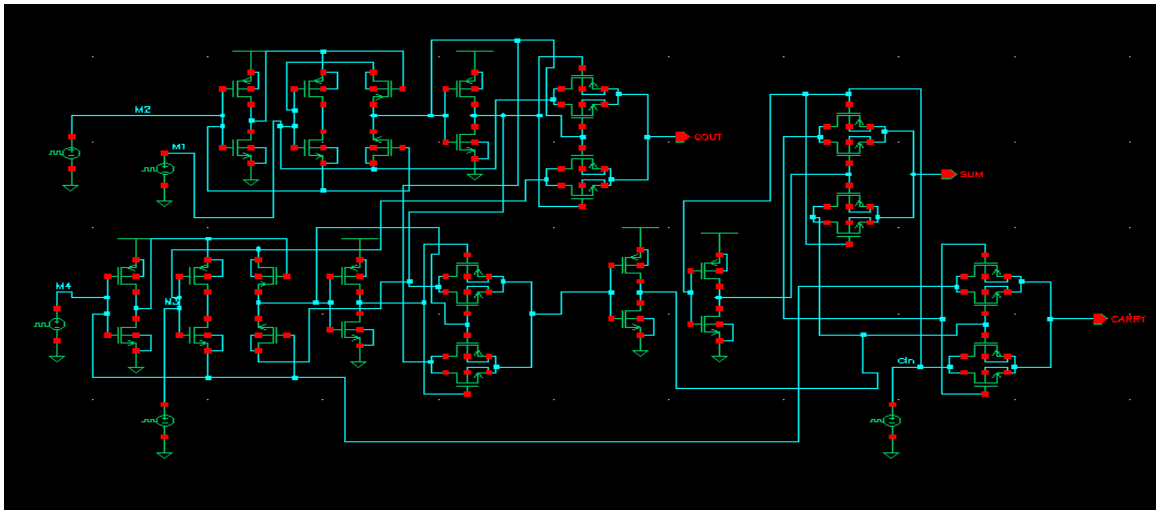

Figure 5. Schematic of proposed novel CMOS 4–2 compressor.

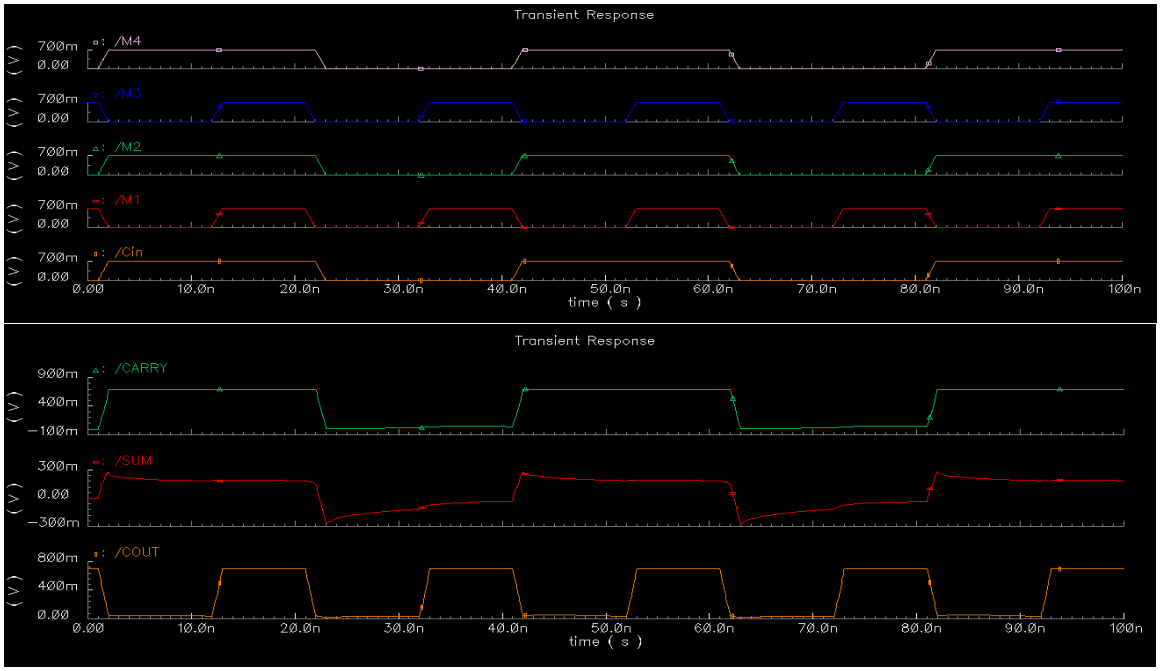

Figure 6. The suggested CMOS 4–2 compressor's transient response.

To simulate the proposed CMOS 4–2 compressor circuit, researchers used a cadence tool and 90 nm method by a notional supply voltage of Vdd = 0.7 V. To reduce power consumption while preserving CMOS 4–2 compressor Circuit performance, several strategies have been utilized to reduce gate leakage at 27°C room temperature. A comparison of CMOS 4–2 compressor Circuit parameters such as delay and low power is presented in Table 1.

Leakage Power Analysis

Leakage power gives a device standby power when we lower the channel length or provide scaling. Sub-threshold voltage and substrate injection effects may both cause leakage current. leakage power is wasted energy, and Compressors have a specific leakage power:

$$P_{LEAK} = I_{LEAK} V_{dd}$$

where P_{LEAK} is leakage power of Full Adder, I_{LEAK} abbreviate for leakage current, Vdd is power supply.

Propagation Delay

Instead of a buffer, a Full Adder is employed, which results in a reduction in both latency and power usage. When it comes Full Adder Compressor, its adjustable threshold voltage is one of its most favorable features. The threshold voltage is adjustable, and it can be set to be either above or below the normal operating voltage of a buffer, making it easier to handle. Since the low-voltage threshold of a Full Adder based Compressor may be adjusted to work with more noise and voltage glitches than a buffer, it is possible to reduce latency by using a Full Adder based Compressor. Full Adder logic gates propagation delay is the time it takes for an input to change before output changes.

The simulation results show that 90 nm technology at 0.7 V supply voltage has a lower latency. Time is taken to get a message through during signal changes.

$$\text{Delay} = 0.69 R_{eq} \times C_L$$

where in the equation the R_{eq} resistance that is implemented using the feed through the cell and C_L is the load capacitance.

CONCLUSION

This study presents a CMOS 4–2 compressor with a complete adder that exhibits reduced power consumption. The analysis and performance of compressor circuits are entirely contingent upon the primary components of the circuits. To reduce power consumption and latency, the circuit uses the XNOR-XOR logic style and transmission-based logic style. Utilizing the Cadence Virtuoso tool in 90nm CMOS technology, three parameters may be computed with an operational supply voltage of 0.7 V: PDP and the maximum output delay. The performance parameters of the proposed compressor are compared with other existing 4–2 compressors using a 0.7 V supply. The simulation results indicate that the proposed CMOS 4–2 compressor achieved improvements in speed, power, and power-delay product (PDP). Other full adder modules exhibit diving capability difficulties; however, this particular module operates at just 0.7 V. The transistor count and power consumption of the proposed CMOS 4–2 compressor are reduced, and its performance surpasses that of existing circuits, as shown by the CMOS 4–2 compressor analysis.

REFERENCES

1. Kaul H, Anders MA, Mathew SK, Hsu SK, Agarwal A, Krishnamurthy RK, Borkar S. et al. A 320 mV 56 μW 411 GOPS/watt ultra-low voltage motion estimation accelerator in 65 nm CMOS. IEEE Journal of Solid-State Circuits. 2008 Dec 30;44(1):107–14.
2. Mokrian P, Howard GM, Jullien G, Ahmadi M. On the use of 4: 2 compressors for partial product reduction. InCCECE 2003-Canadian Conference on Electrical and Computer Engineering. Toward a Caring and Humane Technology (Cat. No. 03CH37436) 2003 May 4 (Vol. 1, pp. 121–124). IEEE.

3. Law CF, Rofail SS, Yeo KS. Low-power circuit implementation for partial-product addition using pass-transistor logic. IEE Proceedings-Circuits, Devices and Systems. 1999 Jun 8;146(3):124–9.
4. Mori J, Nagamatsu M, Hirano M, Tanaka S, Noda M, Toyoshima Y, Hashimoto K, Hayashida H, Maeguchi K. A 10 ns 54* 54 b parallel structured full array multiplier with 0.5 mu m CMOS technology. IEEE Journal of Solid-State Circuits. 1991 Apr 30;26(4):600–6.
5. Dorojevets M, Kasperek AK, Yoshikawa N, Fujimaki A. 20-GHz 8 x 8-bit parallel carry-save pipelined RSFQ multiplier. IEEE transactions on applied superconductivity. 2012 Nov 15;23(3):1300104.
6. Prasad K, Parhi KK. Low-power 4–2 and 5–2 compressors. InConference record of thirty-fifth Asilomar conference on signals, systems and computers (cat. no. 01ch37256) 2001 Nov 4 (Vol. 1, pp. 129–133). IEEE.
7. Chang CH, Gu J, Zhang M. Ultra low-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits. IEEE Transactions on Circuits and Systems I: Regular Papers. 2004 Oct 31;51(10):1985–97.
8. Nirlakalla R, Subba RT, Jayachandra-Prasad T. Performance evaluation of high speed compressors for high speed multipliers. Serbian Journal of Electrical Engineering. 2011;8(3):293–306.
9. Veeramachaneni S, Krishna KM, Avinash L, Puppala SR, Srinivas MB. Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors. In20th International Conference on VLSI Design held jointly with 6th International Conference on Embedded Systems (VLSID'07) 2007 Jan 6 (pp. 324–329). IEEE.
10. Agarwal M, Agrawal N, Alam MA (2014) A new design of low power high speed hybrid CMOS full adder. In: 2014 International Conference on Signal Processing and Integrated Networks, SPIN 2014
11. Tonfat J, Reis R (2012) Low power 3-2 and 4-2 adder compressors implemented using ASTRAN. In: 2012 IEEE 3rd Latin American Symposium on Circuits and Systems, LASCAS 2012-Conference Proceedings
12. Menon R, Radhakrishnan D. High performance 5:2 compressor architectures. IEE Proc Circ Devices Syst. 2006. doi:10.1049/ip-cds:20050152
13. Radhakrishnan D, Preethy AP. Low power CMOS pass logic 4-2 compressor for high-speed multiplication. In: Midwest Symp on Circuits and Systems; 2000. doi:10.1109/MWSCAS.2000.95145
14. Kumar S, Kumar M. 4-2 compressor design with new XOR-XNOR module. In: Int Conf on Advanced Computing and Communication Technologies (ACCT); 2014.
15. Bhattacharyya P, Kundu B, Ghosh S, et al. Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. IEEE Trans Very Large Scale Integr (VLSI) Syst. 2015. doi:10.1109/TVLSI.2014.2357057

