STM JOURNALS

Journal of
Semiconductor Devices and Circuits

ISSN: 2455-3379
Volume 11, Issue 3, 2024
September–December
DOI (Journal): 10.37591/JoSDC

https://journals.stmjournals.com/josdc

Review JoSDC

A Comprehensive Review of FinFET Technology: Advantages, Challenges and Applications

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Abstract

This has been complemented by improvements on the new layers that have surpassed the manufacturer's planar transistor with the new FinFET (Fin Field-Effect Transistor), which enhances modern demands on high performance, small size, and low power consumption. This review is for timely information on the latest developments in FinFET technology, such as curbing leakage currents by 50% and enhancing its speed by 30% proving that FinFETs are indispensable for integrated circuits at 7 nm and below. The review also reviews how FinFETs can lower the dynamic power consumption by about 40% using lower supply voltages, so as to cater to both performance and low-power portable applications. Furthermore, it discusses the effects of the fabrication materials such as high-k dielectric and silicon-germanium (SiGe) on the device characteristics and stability. The review ends with FinFET's use in processors and the Internet of Things, the future consideration of extreme ultraviolet (EUV) lithography, and advanced engineering. Further improvements in semiconductor design are another key aspect of 3D FinFET technology. GAA transistors are integrated into modern designs as they provide superior electrostatic control and further reductions in leakage currents at sub-5 nm nodes. III–V compounds and two-dimensional materials have expanded the application sphere of FinFETs and contributed to new segments such as artificial intelligence, quantum computing, and autonomous systems. Furthermore, significant progress has been made in thermal management and modularity, enabling applications in high-performance computing and energy-constrained consumer devices. As manufacturing processes aim to meet sustainability goals, FinFET technology defines strategies to optimize power and performance. From the discussions in this paper, it is evident that FinFET is strategically positioned to drive nanoelectronics technology forward and unlock new possibilities across a variety of applications, addressing challenges in miniaturization and material integration.

Keywords: FinFET, power consumption, semiconductor materials, integrated circuits, transistor scaling, fabrication technology

INTRODUCTION

Background of FinFET Technology

Current planar transistors are essentially at the material and physical limits as the sizes of devices approach the molecular level. At these small dimensions, other effects, such as short-channel effects, bulk inversion at optimal, and higher leakage of power dissipation, become critical. To address such problems, the semiconductor industry introduced the Fin Field-Effect Transistor (FinFET), which eliminates the planar gate structure with that of a fin-like silicon structure. This three-dimensional architectural enhancement helps to establish better electrostatic control over the channel, making it more efficient, less leaky, and far more scalable. Therefore, FinFETs are vital in furthering the continued scaling of silicon through the node 7 nm and beyond, effectively maintaining the vision of Moore's Law [1–4].

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Received Date: October 04, 2024
Accepted Date: October 10, 2024
Published Date: October 20, 2024

Citation: Joel Joseph, Shiv Prajapati, Parul Panchal. A Comprehensive Review of FinFET Technology: Advantages, Challenges and Applications. Journal of Semiconductor Devices and Circuits. 2024; 11(3): 1–12p.

Importance of FinFET Technology

The present study highlights the significance of FinFET technology in the controllability of short channels, power dissipation, subthreshold leakage current, and variability measures. Knowing that FinFETs are core to the enabling of high-performance, low-power electronic technology, it is imperative for companies operating in fields such as mobile computing, artificial intelligence (AI), and the Internet of Things (IoT) [6]. With an estimated compound annual growth rate (CAGR) of over 22% in 2022–2030, FinFET technology is becoming more critical for generating the next generation of semiconductor devices. Compared with traditional FinFETs, IG FinFETs provide lower power consumption and a higher drive current, making them suitable for high-performance and energy-saving applications. Furthermore, they handle issues related to power consumption in devices and data centers, which are becoming increasingly essential with the ever-rising global energy consumption [5].

Motivation for the Review

In this review, an attempt will be made to present an overview of how FinFET technology is evolving as power efficiency increases, with a special emphasis on the fabrication material. Previous work tends to concentrate on the individual features of FinFETs and lacks a wider perspective; therefore, this review contributes to the integration of enhanced power reduction techniques and material developments. The goal is to distinguish weak points that influence the dependability of circuits made of FinFETs and open new potential scientific and technical discussions in FinFET operation and development as the industry transfers to sub-5 nm nodes [7].

TECHNOLOGICAL EVOLUTION OF FINFET TECHNOLOGY

Historical Context

Therefore, it can be said that the FinFET transistor is an evolution in semiconductor technology that sorts out issues with planar MOSFETs mainly below the 32 nm node. Short-channel effects (SCE), leakage currents, and power inefficiency are the main drawbacks of planar transistors, which become even more serious as the devices shrink. FinFETs using the new design with a FinFET 3-D structure led to the minimization of SCEs and leakage currents [9]. This led to a further increase in the process scaling down to smaller nodes while enhancing both the performance and power factors that pave the way to developing future generations of advanced process nodes, including 7 nm and below [10].

Key Milestones in FinFET Development

1. *Early concepts (1990s):* In 2004, multi-gate transistors were synthesized at the University of California, Berkeley, which presented better gating of the channel and lower leakage currents. These early prototypes set the stage for the future development of FinFETs.
2. *Introduction of FinFET (2000):* Chenming Hu was the first to develop a FinFET architecture in which a gate entirely encases a thin strip of silicon, thereby allowing the effective Channel Length to be considerably shorter than in planar structures. The most significant flaw of the original planar MOSFET structure was solved through improved electrostatic control and scalability.
3. *Commercial adoption (2011):* FinFETs or Tri-Gate transistors were introduced in the 22 nm process by Intel, who reported up to 37% fewer instructions per cycle and 20 – 50% better performance at lower voltages compared to the planar transistor technology. This was a major industry turning point and allowed FinFETs to replace planar MOSFET [8].
4. *Advancements in design (2010s-Present):* Further development strategies, including strained silicon, high-k dielectrics, metal gates, and advanced lithography, make it possible for the FinFET to go below 7 nm. They have increased power consumption by approximately 25% and advanced drive current for optimal general device performance.
5. *Current trends and future directions:* However, as we approach the 5 nm and the 3 nm nodes, FinFETs are also integrating new materials such as germanium and III–V compounds to enhance channel mobility. Furthermore, the emergence of Gate-all-around (GAA) transistors as the next step of progression from the current FinFET structure, which provides better electrostatic control to the channels than the present form of FinFETs, is anticipated. A comparative overview of FinFET generation is presented in Table 1.

Table 1. Comparative overview of FinFET generations.

Generation	Node size	Key innovations	Performance improvements
Early Prototypes (1990s)	N/A	Multi-gate structure, improved channel control	Reduced leakage, concept validation
First Commercial (2011)	22 nm	Tri-Gate design, enhanced electrostatic control	37% performance gain at lower voltage vs planar transistors
Advanced FinFET (2014-18)	14 nm, 10 nm	Strained silicon, High-K/Metal Gate (HKMG) stack	~25% power reduction, improved drive current
Latest FinFETs (2020-Present)	7 nm, 5 nm	Improved channel mobility, advanced lithography	40% lower power consumption, high performance
Future Directions	5 nm and beyond	Gate-all-around (GAA) structure, III–V, and germanium channels	Further scaling, better short-channel control

Recent Developments and Innovations

Recent advancements in FinFET technology have focused on further enhancing power efficiency, performance, and scalability.

- *Gate-all-around technology:* GAA transistors, including nanosheet and nanowire FETs, enable better electrostatic control owing to their encircling channels. However, what GAA is supposed to allow for even more aggressive scaling and power reduction at 5 nm nodes and below?
- *Material innovations:* To counter the continual scaling issue, carrier mobility is increasing, and elements such as III–V compounds and germanium are being written into the chip. These materials enhance the drive current and power density and increase the efficiency, particularly in high-performance applications, including AI and data processing.
- *Extreme ultraviolet (EUV) lithography:* Double patterning is now required in EUV lithography at sub 7 nm nodes for FinFET manufacturing, which minimizes variability and maximizes yield. The advanced micropatterning technology, EUV, is the main contributing factor at 3 nm and the following node.
- *Thermal management:* Transistor density has been another challenge with a high rate of packaging, which has triggered significant interest in thermal management. Innovations in cooling and thermal compounds are being sought to sustain the efficiency and durability of compact, thermally demanding parts [11].

APPLICATIONS OF FINFET TECHNOLOGY

Since its introduction, FinFET technology has been one of the most efficient solutions for modern semiconductor issues, namely, high-speed, and low-power devices, and their scalability. Below are the key applications and examples of FinFET implementations along with their respective limitations.

High-performance Computing (HPC)

FinFETs act as a revolutionary tool for boosting the speed-to-power advantage in CPUs, GPUs, and data centers to support AI, Machine learning, and large data management. For instance, Intel, the Xeon processors utilized in data centers, utilize FinFET technology to offer increased speeds and decreased power use.

Limitation

High-density designs in HPC systems produce a lot of heat, especially with densely packed components, and the cooling mechanisms needed to cater to the thermal density increase the complexity and costs.

Mobile Devices

There are some advantages of using FinFETs; these benefits include the battery life and energy efficiency of smartphones and wearable technology devices. For instance, the A14 Bionic chip in Apple is built with a 5 nm FinFET process; the power of this chip is 40% more efficient than other previous

generations and provides longer battery backing at the same time supporting the gaming application and AR.

Limitation

Leakage currents and voltage dissipation remain challenging at smaller nodes, causing power loss in microprocessors and making further scaling difficult without introducing leakage issues.

Internet of Things

FinFET technology allows for small power consumption and chip sizes that are necessary for IoT devices, such as sensors and wearable devices. Samsung is one of several companies that use Exynos chips for many IoT devices that require FinFETs for efficient processing and prolonged battery life.

Limitation

There are additional IoT use cases that also demand somewhat less power than what the actual FinFET designs enable, which include devices that depend on energy scavenging or minute batteries to power them for an extended length of time.

5G and Telecommunications

FinFETs are ideal for the high data rates and signal processing required by 5G mobile networks. As for the Snapdragon processor base in Qualcomm, FinFET technology has been adopted to enhance the radio frequency (RF) results, which indicates the data transfer rate and power advancement of 5G smartphones.

Limitation

Normally, FinFETs reduce I/O costs, but they are not efficient at the frequencies used in mmWave 5G; therefore, it is necessary to turn to other structures such as GAA transistors for the enhanced RF characteristic.

Automotive Electronics

By providing reliability and stability, FinFETs meet the high-level automotive requirements in Advanced Driver Assistance Systems (ADAS) and infotainment systems. For instance, self-driving infotainment chips currently deployed in Tesla electric car electric vehicles (EVs) have been developed using FinFETs.

Limitation

Strong mechanical and thermal environments in automobiles harm the reliability of FinFET-based devices and cause greater susceptibility to failure, thus necessitating more robust packaging and encasing materials.

Consumer Electronics

FinFETs are particularly utilized in optimizing the performance and power management of consumer electronic devices, such as laptops, game consoles, and smart TVs. New-generation game consoles such as Xbox Series X and PlayStation 5 have chosen FinFET-based Advanced Micro Devices (AMD) processors that guarantee high-performance gaming with better power efficiency.

Limitation

The high cost of FinFET fabrication remains a concern because their structures are more advanced than those of typical flat transistors.

Healthcare and Wearables

FinFETs drive low-voltage applications that include wearable health monitors, such as smartwatches, CGM, and diagnostic tools. These devices use FinFETs for health monitoring in real-time with minimal power consumption; thus, they can operate continuously and do not require frequent charging Design of (a) FinFET and (b) SOI FinFET is shown in Figure 1.

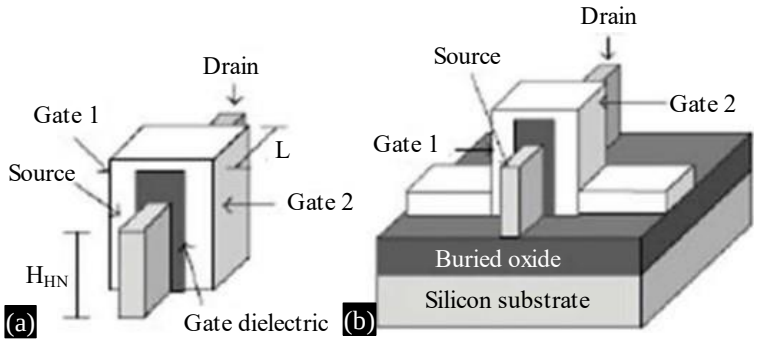

Figure 1. Design of (a) FinFET and (b) SOI FinFET.

Limitation

Ultra-low standby power to increase operating cycles in healthcare applications where some relief is desired, particularly in the case of medical equipment that may be in use for long periods and requires no attention from service personnel such as remote patient monitoring systems.

DESIGN AND PERFORMANCE ANALYSIS OF FINFET TECHNOLOGY

Introduction to FinFET Design

Planar MOSFETs are largely outdated, while FinFETs are a step forward owing to their 3D structure, which is designed to provide strong electrostatic control, reduce the leakage current, and have better scalability at smaller nodes of manufacturing. These features make FinFETs suitable for use in devices that require high operating performance, low power consumption, and both present and future integration capabilities in operation within modern semiconductors [12]. The design of the (a) FinFET, and (b) silicon-on-insulator (SOI) FinFETs is shown in Figure 1.

Key Design Features of FinFETs

- *3D Fin Structure:* The gate is positioned around the fin on three edges; this results in better electrostatic control, minimizes SCE and leakage currents, and enhances performance and power consumption.
- *Gate-all-around:* To provide even greater electrostatic control by encircling the channel, they are expected to further decrease leakage at sub-5 nm nodes.
- *High-K/Metal Gate (HKMG):* Hafnium oxide and metal gates also minimize leakage and improve the effectiveness of the gate, thus enabling future shrinking.
- *Strained Silicon:* Though SiGe and III–V compounds boost the carrier mobility in the devices, they are suitable for high-speed applications such as high-performance processors and communication devices.

Performance Metrics of FinFETs

- *Subthreshold Slope (SS):* FinFETs have a lower subthreshold slope (~60 mV/decade) than planar MOSFETs, which provides better switching. It has been established that GAA transistors are expected to perform even better.
- *On-Current (I_ON) and Off-Current (I_OFF):* Moreover, FinFETs provide 30% better endpoint current, I_ON as well as 50% less leakage current, I_OFF improving energy consumption. GAA transistors offer even further leakage reduction, making them perfect for the sub-5 nm node.
- *Drive Current and Delay:* The suitably high drive current and compounding switching speed make FinFETs adept for use in processors and GPUs. By enhancing the execution strategies, we anticipate that GAA FETs will increase these indices.
- *Power Efficiency:* FinFETs enable up to 40% reduction in dynamic power, thus making themselves ready to be implemented in mobile and IoT devices. GAA transistors provide slightly more power efficiency than FDSOI at nanoscale nodes.

- *Thermal Stability:* Owing to the low leakage currents, FinFETs enable better thermal characteristics for high-power applications such as automotive electronics and data centers. It is believed that GAA transistors should deliver similar or improved stability compared with FinFET transistors [13].

Comparative Performance of FinFETs and Emerging Technologies

- *Nanowire FETs (GAA):* These types of transistors are better in terms of electrostatic control and size than FinFETs, which have improved I_ON by 50% and reduced I_OFF, making them suitable for sub-5 nm.
- *Tunnel FETs (TFETs):* Quantization of power occurs through quantum tunneling in TFETs, but the problem with these devices is that they entail a low drive current and are hence not suitable for better performance in computing applications.
- *Carbon Nanotube FETs (CNTFETs):* CNTFETs provide high mobility and low power, but integration issues make them less suitable as near-future replacements for FinFET and GAA transistors.

POWER CONSUMPTION IN FINFET TECHNOLOGY

Of these, FinFET technology plays an important role in power dissipation as devices scale down to deeper nodes because of its marked leakage/dynamic power performance advantage over its planar MOSFET counterpart.

1. *Reduced leakage current:* Owing to the special 3D gate structure of FinFETs, the electrostatic administrative control is higher and the off-state current is less than the plane MOSFET by 50%. Transistors working with GAA at sub 5 nm nodes will bring about an additional level of leakage control owing to the complete encircling of the channel.
2. *Lower threshold voltage variability:* As a result, using FinFETs results in an improved Vt control that reduces variability without sacrificing the benefits attained at lower voltages. The inclusion of materials such as SiGe and III–V compounds will add to the extent of Vt control, which is critical for mobility and HPC use.
3. *Dynamic power efficiency:* FinFETs reduce the supply voltages, and the capacitance, and minimize dynamic power by 40%; appropriate for mobile, AI, and HPC. Hence, many future designs based on multi-threshold voltage configurations will enhance power management.
4. *Scalability and power efficiency:* FinFETs can be scaled down to 7 nm and below. GAA transistors will take over FinFETs at sub-five nanometers for better command and power management.
5. *Thermal management:* The lower power loss of FinFETs enhances the thermal characteristics of the devices, prolonging the working cycle, AI, and data centers. Future applications of FinFETs will improve the thermal characteristics of packaging 3D. A comparison of the FinFET, Planar MOSFET, and GAA FET is presented in Table 2.

Table 2. Comparison of FinFET, Planar MOSFET, and GAA FET.

Metric	FinFET	Planar MOSFET	GAA FET
Leakage current	Up to 50% reduction	Higher leakage	Further reductions expected
Dynamic power efficiency	~40% reduction	Higher due to capacitance	Similar or superior to FinFET
Threshold voltage control	Consistent threshold voltage control, minimal leakage	Greater variability	Improved control
Scalability	Effective at 7 nm and beyond	Limited beyond 14 nm	Superior at sub-5 nm
Thermal management	Lower dissipation, better heat control	Higher dissipation	Similar or better than FinFET

Future Trends: GAA Transistors

The wrap-around style gate of the GAA transistors reduces the leakage current and achieves better electrostatic control of the device, resulting in enhanced power performance. FinFETs will be superseded by GAA at sub-5 nm and will be optimized for scaling, putting them at vantage for the next generation of mobile, IoT, and AI use cases.

FABRICATION AND MATERIALS IN FINFET TECHNOLOGY

The conversion from two-dimensional planar structures to FinFETs represents one of the most important changes in semiconductor manufacturing technology because of the technological demands for performance, power consumption, and scalability. The Static random access memory (SRAM) technology of FinFETs implies a connection with high-density and low-power devices, which offers certain difficulties and, therefore, requires modern technologies and materials. Some of the latest material and process developments have become key enablers in moving FinFET technology down to 7 nm, 5 nm, and beyond.

FinFET Fabrication Process

1. *Lithography and patterning:* EUV lithography is used for fin generation below the 7 nm node, which is described under this category. The high resolution and fidelity of EUV make it well suited to the patterning needed for FinFETs' small dimensions; however, EUV has its own cost and defects to lay, which needs further improvements.
2. *Fin formation:* The etching irregularity of the fins arises from the anisotropic etching process that forms fins from the silicon substrate. The first developments related to the control of fin dimensions, because fin height and fin width must be reconciled to achieve the desired balance between performance and power.
3. *Gate dielectric deposition:* There are new high-dielectric-constant materials, such as HfO_2, to reduce gate leakage while having the ability to go to the next level. Atomic Layer Deposition (ALD) offers the possibility of obtaining a dielectric thickness with high reliability and performance.
4. *Gate electrode formation:* High-metal gates such as Titanium Nitride (TiN) and tungsten (W) decrease the channel resistance to enhance the drive current and power supply. The current research aims to find better materials for gates that can perform better in devices that are at the sub-5 nm level.
5. *Source/drain engineering:* Strain management using SiGe or SiC increases the carrier mobility and, in turn, increases the drive current. The incorporation of these materials is essential for enhancing the performance of miniature devices.
6. *Spacer formation and silicidation:* Dielectric materials such as silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) separate the gate and source/drain areas; nickel silicide (NiSi) reduces the contact resistance-enhancing current through the circuit path.
7. *Contact formation and metallization:* Copper and aluminum are the materials most commonly used in interconnections, but cobalt and ruthenium are used because of their low resistance and backup against electromigration in interconnects owing to scaling in advanced nodes.

Materials Used in FinFET Fabrication

- *Silicon and silicon-germanium (SiGe):* The fin structure is made of Silicon and, SiGe is used to improve mobility in a p-type channel transistor, which is essential in technology with sizes below 10 nm.
- *High-k dielectrics:* HfO_2, for example, increases the capacitance and decreases the gate leakage, which is crucial for scaling to finer features.
- *Metal Gates:* Comparison of both W and TiN lower gate resistance and increased switching speed. Current research is directed towards searching for improved higher levels of performance at smaller nodes.
- *Spacers and isolation:* Si_3N_4 and SiO_2 eliminate parasitic capacitance and help to isolate gates that could otherwise interfere with tightly grouped parts.

- *Silicides and interconnects:* True rectangular dual-fin field dielectric isolation with nickel silicide (NiSi) results in low contact resistance, and copper is still a major interconnect metal. Nevertheless, both cobalt and ruthenium materials are under discussion for enhancing the current reliability and avoiding electromigration at advanced nodes.

Challenges in FinFET Fabrication

1. *Patterning and lithography:* High numeric humanities orders remain a key for small node sizes in modern FinFETs, with EUV lithography being a crucial technique, albeit costly and accompanied by difficulty in managing defects. Pricing, and in particular, achieving stable yields even at smaller nodes remains a challenge.
   - *Potential solution:* Explorations in the directed self-assembly technique, in which molecules automatically arrange themselves in the required manner, could be used to reduce EUV use while retaining the same level of accuracy.
2. *Strain engineering and material integration:* Strain engineering and the use of new materials, including III–V materials, for example, indium gallium arsenide (InGaAs), increases the device efficiencies but has barrier-like lattice mismatch and defect formation. These problems occur when dissimilar material systems are joined, and the atomic arrangement deforms at the interfaces, affecting the reliability of the devices.
   - *Potential solution:* More complex procedures such as Heterojunction Integration (the use of materials with dissimilar characteristics such as thermal expansion) and Epitaxial Growth (successive layering of materials free from any structural imperfections) are in an experimental stage to minimize imperfections and maximize the compatibility between the materials being used.
3. *Thermal management:* This is especially the case as transistor density increases, and hence, power densities are also enhanced, caused by heat dissipation problems. Lack of thermal control can cause equipment failure or reduced functionality when used in high-power conditions such as AI and data centers.
   - *Potential solution:* Further work is still being conducted in the areas of superior cooling techniques, such as liquid cooling, phase change materials, and 3D packaging. Furthermore, TIMs that enhance the thermal conductivity for cooling each device are in the works for circuits that are increasingly more compact.

TYPES OF FINFETS

FinFETs (Fin Field-Effect Transistors) apply a three-dimensional design, which provides better control over SCE. Different FinFET structures are possible, and each is designed to achieve the best performance in terms of power.

SG FinFET (Single-Gate FinFET)

- *Structure:* The gate is formed only on one of the sidewalls of the fin at the top, whereas the other surfaces are open or have a dielectric layer.
- *Operation:* Provides less electrostatic control, leading to a low drive current, and is best suited for designs requiring simplicity and low power consumption.
- *Applications:* Employed in low-power digital applications, where power consumption is of paramount importance compared to frequency. The 3D structure of the SG FinFET is illustrated in Figure 2.

IG FinFET (Independent-Gate FinFET)

- *Structure:* There are separate gates on each side of the fin, which enables the fin to be operated independently.
- *Operation:* Provides flexibility in the amount of threshold voltage that can be set to allow it to switch between low-power mode and high performance.
- *Applications:* Recommended for adaptive power control and other applications that may necessitate power efficiency and the ability to perform complex operations seamlessly. The three-dimensional (3D) structure of the IG FinFET is shown in Figure 3.

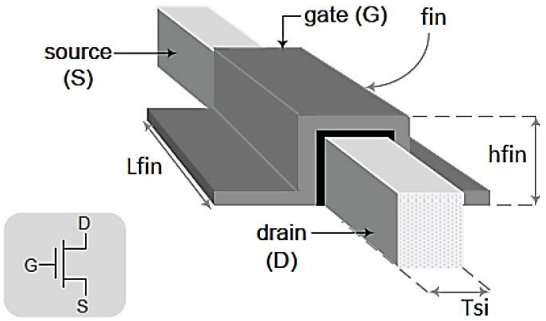

Figure 2. 3D structure of SG FinFET.

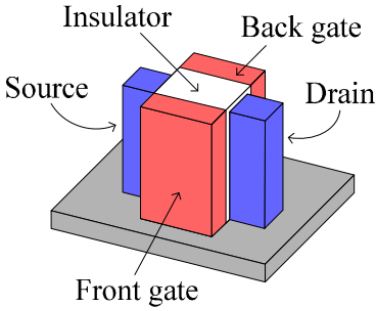

Figure 3. 3D structure of IG FinFET.

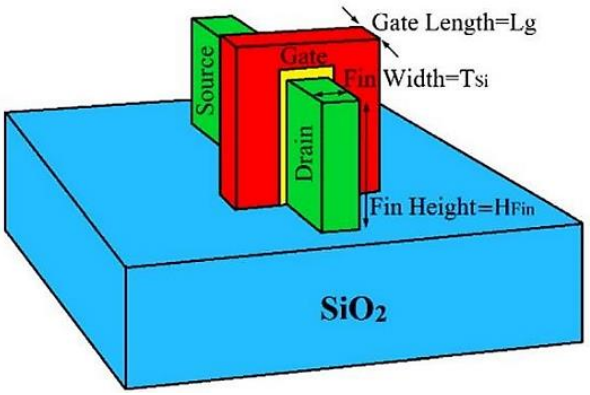

Figure 4. 3D structure of TG FinFET.

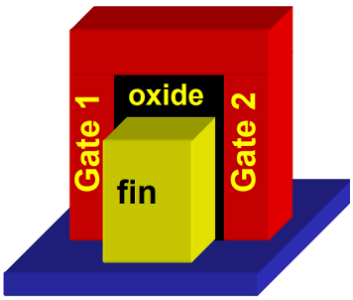

Figure 5. 3D structure of DG FinFET.

TG FinFET (Triple-Gate FinFET)

- *Structure:* This gate extends up to three sides of the fin: the top and both sidewalls, thus offering excellent electrostatic control.
- *Operation:* Strengthens the gate channel connection, minimizes leakage currents, and optimizes its performance for a smaller technology node.
- *Applications:* Characteristics of high-end computing and low-power designs, where good gate control and high drive currents are required. The three-dimensional (3D) structure of the TG FinFET is shown in Figure 4.

DG FinFET (Dual-Gate FinFET)

- *Structure:* This gate encircles the two vertical sidewalls of the fin, and the top may be either exposed or covered by a dielectric material.
- *Operation:* This allows for good electrostatic control and minimization of SCE. They can be configured to function in tandem or separately depending on their efficiency.
- *Applications:* Popular in digital logic and analog systems, and can be applied effectively in both high-speed and low-power applications. The 3D structure of the DG FinFET is illustrated in Figure 5.

Challenges in FinFET Technology

Although FinFET technology provides an improvement in performance and energy, there are difficulties as long as the number of nodes decreases below 7 nm. These are issues related to fabrication difficulty, SCE, power dissipation, use of materials, and thermal considerations.

1. *Fabrication complexity:* Compared to planar transistors, FinFET structures have three-dimensional and complex structures that require special processes, such as EUV lithography, which are costly and pose significant challenges to manufacturing companies to attain high yields.
    - *Example:* Intel struggled with a 10 nm process with fin patterning being one of the main challenges. At the 7 nm node, EUV lithography was adopted to enhance patterning

accuracy because of its ability to produce finer patterns that were difficult to produce using previous techniques.
- *Future outlook:* Current research is directed at refining EUV tools and searching for another solution in the form of directed self-assembly (DSA) to drive prices down and refine the resolution.

2. *Short-channel effects:* As nodes continue to be reduced below 7 nm, SCEs including drain induced barrier lowering (DIBL) and threshold voltage increase and decrease circuit performance.
   - *Example:* Taiwan Semiconductor Manufacturing Company (TSMC) uses HKMG stacks as well as precise gate control for the 5 nm node to reduce SCEs and enhance performance.
   - *Future outlook:* It was also warned that GAA transistors such as nanosheet and nanowire FETs are expected to provide even better control over SCEs and may serve as a solution for sub-5 nm nodes.
3. *Power consumption and leakage:* As devices shrink, their power consumption and leakage currents are magnified, especially at low voltages. More often, it becomes exceedingly complicated to balance leakage with the performance of the firm.
   - *Example:* Apple 5 nm A14 Bionic chip employs a 5 nm FinFET with the latest solution for a high-k dielectric and a method called power gating for power consumption savings.
   - *Future outlook:* Future work will investigate III–V semiconductors and a two-dimensional material, MoS_2, to eliminate leakage currents and enhance productive power in successive generations.
4. *Material integration:* The use of high-k dielectrics and metal gates for devices presents a problem of defects and stability as the node sizes further decrease.
   - *Example:* Samsung's 7 nm FinFET process conducts SiGe in the channel to enrich carrier movement. However, deformations such as lattice mismatch could be a problem; these are defects when it comes to the reliability of devices.
   - *Future outlook:* Current research efforts have focused on refining the interfaces of the materials to eliminate as many defects as possible and experimenting with new applications of materials such as GaN and InGaAs.
5. *Thermal management:* The primary disadvantage of transistor density is that it generates heat–thermal hotspots that reduce reliability and shorten device lifespans. Thermal management has a significant impact on product performance in high-power applications.
   - *Example:* NVidia's 7 nm GPUs contain state-of-the-art thermal solutions to control the heat output while overloaded with computational workloads.
   - *Future outlook:* Current research on liquid cooling, thermal sensors, and 3D packaging is being conducted to address the problems of heat dissipation in high-power designs, including AI processing and data centers.
6. *Cost and scalability:* Owing to the complex geometry of FinFETs and the application of EUV lithographic techniques, FinFET manufacturing is expensive. The high costs can be a problem when considering the scale of FinFETs for volume manufacturing, or if the foundry is small or application-sensitive.
   - *Example:* The 5 nm node in the Taiwan Semiconductor Manufacturing Company (TSMC) is used by most companies, even though its costs are high because of the manufacturing benefits it offers, including performance and power consumption.
   - *Future outlook:* Methods such as DSA and three-dimensional integration are currently being studied to make FinFET technology more cost-effective and effective for sub-5 nm nodes.

CONCLUSION

FinFETs (or tri-gate transistors) have become the new heart of semiconductors, applying alternatively to planar transistors as the entrance of 7 nm nodes and beneath. The gate structure of FinFETs is 3D, which enhances electrostatic control, improves power dissipation, and is less susceptible to SCE; thus, it is appropriate for high-speed and low-power applications. Improvements and innovations, including high-k dielectrics and metal gates, have also been incorporated into FinFET structures. However, the

following challenges persist: fabrication complexity, material variability, and leakage current. With technology scaling, low gate voltages and signal control have become further challenges.

Current explorations, including GAA transistors and materials such as silicon-germanium (SiGe) and III–V compounds, are Design of Experiments (DOE) to meet such challenges.

Future trends and research directions: Why FinFETs reside in such a situation and what are the limitations of FinFETs when the forthcoming semiconductor technology is concerned are important to understand which GAA nanosheet and nanowire FETs are expected to emerge to overcome the current situation for new applications such as quantum computing and neuromorphic computing, which require high accuracy and low power.

Key Research Areas Include

- *Material integration:* III–V compounds (InGaAs, etc.) and 2D semiconductors (graphene, MoS_2, etc.) have been investigated to activate other carriers to achieve higher mobility and lower energy consumption. Nevertheless, issues such as defects, lattice mismatch, and heat dissipation remain among the burning problems. Solutions to these problems are still being researched using techniques such as heterogeneous integration and epitaxial growth.
- *Advanced lithography:* With EUV lithography being critical to sub-7 nm nodes, the development of short-wavelength EUV and DSA is anticipated to enhance the pattern quality and lower the cost. It was concluded that further studies on mask defects and resist material optimization remain indispensable for sub-5 nm scaling.
- *Thermal management:* It is also noted that with higher transistor density, thermal issues may arise as critical problems in 3D designs. Investigations on liquid cooling, PCM, and 3D packaging have mainly focused on heat removal. Furthermore, some aspects of thermal sensing and dynamic cooling solutions to guarantee dependability for high-performance consumers are under consideration.

FinFETs, with future 3D architectures, will remain a key contribution in defining next-generation computing paradigms for delivering suitable performance enhancement with controlled energy and at scaled Technology Nodes for advanced applications.

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