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Thevenin Impedance Networks for Spice Simulation Using Analog Behavioral Modeling

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Abstract

PSPICE/OrCAD software analog behavioral modeling (FREQ) option is used to obtain equivalent circuits for Thevenin equivalent resistance to be used for three types of applications for different circuits (other different networks with these Thevenin models at DC), and Spice files are described to simulation circuits with AC analyses. Three different applications are useful in linear integrated circuits using DC Thevenin resistance of two networks are considered. Firstly, the DC Thevenin resistance is converted to AC Thevenin impedance with a complex multiplication factor using analog behavioral modeling of PSpice. This impedance is connected across the required terminals of an electronic circuit and analyzed. An impedance with a value equal to complex AC voltage equivalent to AC Thevenin equivalent is connected across the required terminals (with equivalent impedance=AC voltage/AC) and verified. The current through this impedance is converted to the desired AC voltage with a complex number and a third circuit is analyzed with these modifications. Two SPICE files which are self-explainable are given with examples. The FREQ option, which was not previously available in SPICE 2G versions, is used to obtain Thevenin modifications for impedance and AC voltages. This Analog behavioral option can be used in polar or rectangular formation of complex numbers. The frequency-dependent (independent) immittances can be simulated using this option. These two facilities are (could be) used in the examples described.

Keywords: Analog passive network theory, non-linear circuits, complex variables, circuit analysis and modeling, solid state circuits, microwave circuits, VLSI technology

INTRODUCTION

A circuit with resistors and independent voltage and current sources can be substituted with a *Thevenin equivalent* circuit. Substitution can be helpful in circuit analysis and simulations [1–12].

Thevenin Theorem and Application

The Thevenin equivalent circuit is an ideal independent voltage source connected in series with a resistor. In this work, a few networks employing the Thevenin equivalent parameter (resistance) in voltage and impedance form used in different networks are simulated by the SPICE software program with analog behavioral modeling of PSpice.

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CIRCUITS AND SIMULATION PROCEDURE

Spice/PSpice is used to obtain the inverse transmission parameters for the linear two-port circuits. The inverse transmission parameter determination for a circuit with an analog behavioral modeling option using SPICE2/PSpice can be performed with the FREQ option. The frequency description FREQ of the analog behavioral modeling options of PSpice could also be used for the following applications with Thevenin DC resistance.

The following procedure is used to obtain equivalents for complex Thevenin impedances and equivalent current/voltages.

1. An electronic network is analyzed with an impedance connected between nodes (N1, N2) which is in the form R_T (1+j), where R_T is the DC Thevenin resistance of another electronic circuit.
2. The same circuit is again analyzed with another equivalent impedance R_T (1+j)/I (N1, N2) between the same nodes N1 and N2 with the previous impedance R_T (1+j) replaced. I (N1, N2) current between nodes (N1 and N2).
3. With the help of the above two representations, a different electronic circuit with an AC voltage equivalent to a known complex number multiple of I(N1, N2) is excited using PSpice-compatible networks.

The FREQ extension of PSpice allows transfer functions (voltage-controlled current, voltage-controlled voltage, current-controlled voltage, and current-controlled current-dependent sources with complex (AC) constants) as follows:

**E/G <name> N+ N- FREQ {voltage/current} = (frequency value, 20*log (modulus of complex number), phase of complex number in degrees) **

If the frequency falls between the two defined frequencies, the magnitude and phase of the output are obtained by interpolation. A network with pure resistance excited by DC sources is considered. Figure 1(a) and (b) show a network and its equivalent for computing the Thevenin resistance between the R and S terminals.

Figure 2(a) and (b) show another network with resistances and independent energy sources, and its equivalent circuit to obtain the Thevenin/Norton resistance between terminals R and S. The circuit (Figure 3) shows the Thevenin/Norton impedance (Figures 1(b) and 2(b)) (RT), Value =RT(1+j)/I (N1, N2), implemented as shown in Figure 3. I (N1, N2) is the current flowing through it.

In Tables 1 and 2, the SPICE/PSpice simulation files used to obtain results for two different circuits with the modified DC Thevenin resistance shown in Figures 1(b) and 2(b) (RT(1+j)/I(N1, N2)) are described. Three different applications to obtain the Thevenin impedance are described for two different AC circuits with analog behavioral modeling of PSpice. All results were verified using conventional methods.

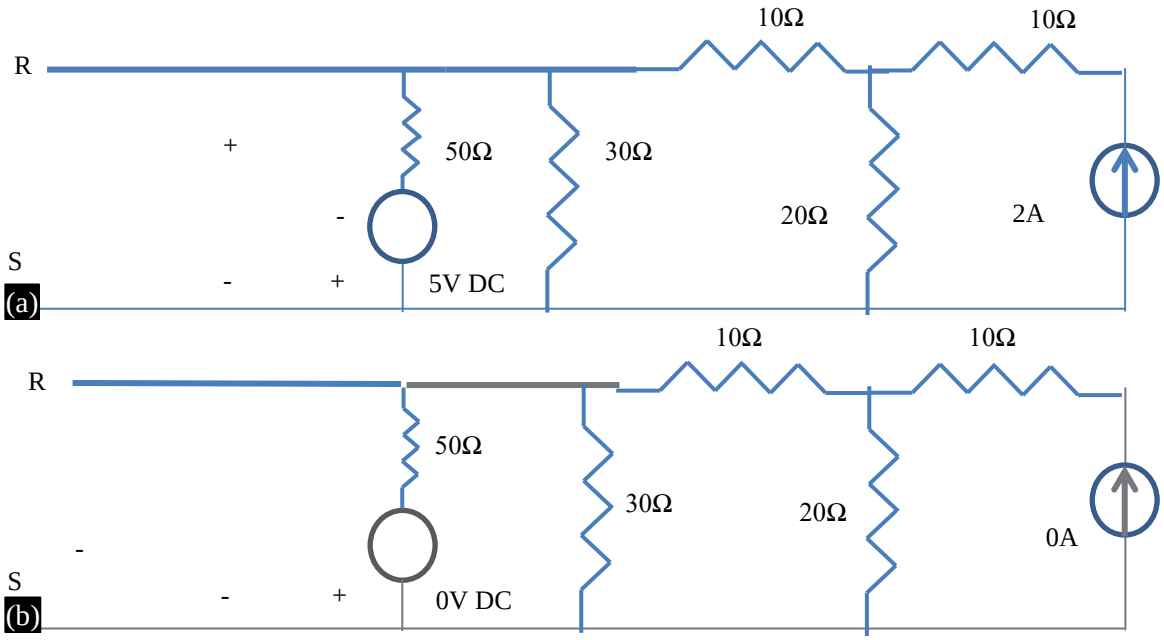

Figure 1. (a) A DC linear circuit whose Thevenin equivalent is across R-S terminals, (b) Equivalent Circuit for Thevenin Resistance across R-S terminals.

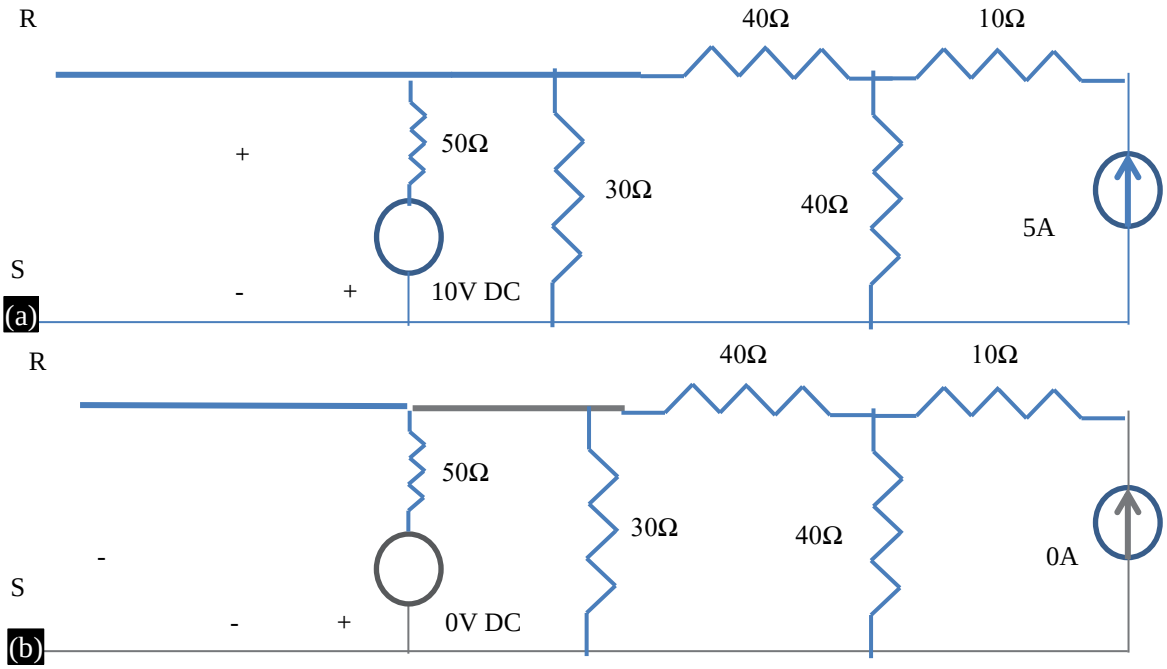

Figure 2. (a) Linear DC network whose Thevenin Parameters are across R_S terminals, (b) Equivalent Circuit (second example) for Thevenin Resistance across R-S terminals.

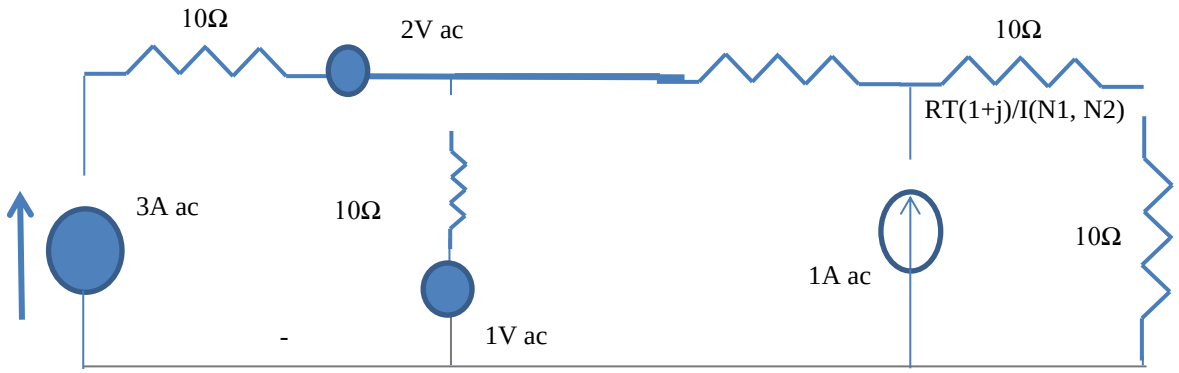

Figure 3. A network implementing polynomial Thevenin equivalent parameters.

Simulation Results

The following is a description of the SPICE/PSpice files. Circuit representations for the DC Thevenin resistance rt are listed in Tables 1 and 2.

Case 1

**** 10/20/24 18:11:31 ***** PSpice Lite (October 2012) ****** ID# 10813 ***

Three applications as described in the section "*Circuits and Simulation Procedure".*

Case 2

**** 10/20/24 18:11:31 ***** PSpice Lite (October 2012) ****** ID# 10813 ****

Three applications are described in Table 3 (see the section *"Circuits and Simulation Procedure"*).

Small Signal Bias Solution Temperature = 27.000°C

Table 1. DC Thevenin resistance (RT) circuit.

Parameters		***IMPLEMENTATION OF THEVENIN impedance RT(1+j)**
R12 1 2 50	R50 5 0 50	I08 0 8 AC 3
V20 2 0 DC 5	R550 5 0 30	R89 8 9 10

Parameters		***IMPLEMENTATION OF THEVENIN impedance RT(1+j)**
R10 1 0 30	R56 5 6 10	V109 10 9 AC 2
R13 1 3 10	R60 6 0 20	R1011 10 11 10
R30 3 0 20	R67 6 7 10	V110 11 0 AC 1
R34 3 4 10	R70 7 0 1E20	R1012 10 15 10
I04 0 4 DC 2	IFI05 0 5 AC 1	I012 0 15 AC 1
		R130 13 0 10
		GT 0 21 FREQ {V(5)} = (1E06,3.0102,45)
		R210 21 0 1

Table 2. A circuit with AC voltage which is a complex multiple of I(n1, n2)

EFVX22 22 0 30 0 1
V2223 22 23 AC 2
R2327 23 27 100
E270 27 0 FREQ {V(21)} = (1E06,0.,0.)
GFFI 0 25 FREQ {I(V1512)} = (1E06, 20.,90)
V2530 25 30
ETFI 30 31 FREQ {I(V1512)} = (1E06,6.02059991328,30.)
V3125 31 0
R250 30 0 1E20
*Realization of resistance between nodes (15) and (13)
*Impedance = RT(1+j)/I(N1, N2)
V1512 15 12
E1213 12 13 21 0 1
.AC LIN 1 1MEG 1MEG
.PRINT AC VM(22) VP(22)
.PRINT AC VM(30) VP(30) IM(V2530) IP(V2530)
.OP
.end

Table 3. Node voltage values.

Node	**Voltage**	**Node**	**Voltage**
1	16.5380	12	0.0000
2	5.0000	13	0.0000
3	24.3590	15	0.0000
4	44.3590	21	0.0000
5	0.0000	22	0.0000
6	0.0000	23	0.0000
7	0.0000	25	0.0000
8	0.0000	27	0.0000
9	0.0000	30	0.0000
10	0.0000	31	0.0000
11	0.0000		

Table 4. Voltage source currents.

Name	**Current**
V20	2.308E-01
V109	0.000E+00
V110	0.000E+00
V2223	0.000E+00
V2530	0.000E+00
V3125	0.000E+00
V1512	0.000E+00

Total Power Dissipation -1.15e+00 Watts (as calculated from Tables 3 and 4)

Case 3

**** 10/20/24 18:11:31 ***** PSpice Lite (October 2012)****** ID# 10813 ****

Three applications, as described in the section "*Circuits and Simulation Procedure"* (Tables 5 and 6 and the output presented in Table 7)

Operating point information temperature = 27.000°C

AC Analysis Temperature = 27.000°C

Table 5. Voltage-controlled current sources.

Name	GT	GFFI
I-source	0.000E+00	0.000E+00

Table 6. Voltage-controlled voltage sources (**** PSpice Lite (October 2012) ****** ID# 10813 ****).

Name	EFVX22	E270	ETFI	E1213
V-source	0.000E+00	0.000E+00	0.000E+00	0.000E+00
I-source	0.000E+00	0.000E+00	0.000E+00	0.000E+00

Table 7. Output table.

FREQ	VM (22)	VP (22)	VM (30)	VM (30)	IM(V2530)	IP(V2530)
1.000E+06	2.741E+00	1.370E+01	2.741E+00	1.370E+01	1.370E+01	7.370E+01

Table 8. Circuit description for case 3.

****
****
*Thevenin Impedance = RT (1+j)
*dc Thevenin resistance (RT) circuit
R12 1 2 50
V20 2 0 DC 10
R10 1 0 30
R13 1 3 40
R30 3 0 40
R34 3 4 10
I04 0 4 DC 5
*Above circuit representation for DC Thevenin resistance RT
R50 5 0 50
R550 5 0 30
R56 5 6 40
R60 6 0 40
R67 6 7 10
R70 7 0 1E20
IFI05 0 5 AC 1
*Implementation of Thevenin impedance RT(1+j)
I08 0 8 AC 3
R89 8 9 10
V109 10 9 AC 2
R1011 10 11 10
V110 11 0 AC 1

R1012 10 15 10
I012 0 15 AC 1
R130 13 0 10
GT 0 21 FREQ {V(5)} = (1E06,3.0102,45)
R210 21 0 1
*A circuit with AC voltage which is a complex multiple of I(N1, N2)
EFVX22 22 0 30 0 1
V2223 22 23 AC 2
R2327 23 27 100
E270 27 0 FREQ {V(21)} = (1E06,0.,0.)
GFFI 0 25 FREQ {I(V1512)} = (1E06, 0.,0.)
V2530 25 30
ETFI 30 31 FREQ {I(V1512)} = (1E06,6.02059991328,30.)
V3125 31 0
R250 30 0 1E20
*Realization of resistance between nodes (15) and (13)
*Impedance = RT(1+j)/I(N1, N2)
V1512 15 12
E1213 12 13 21 0 1
.AC LIN 1 1MEG 1MEG
.PRINT AC VM(22) VP(22)
.PRINT AC VM(30) VP(30) IM(V2530) IP(V2530)
.OP
.end
**** 10/20/24 18:24:00 ****** PSpice Lite (October 2012) ****** ID# 10813 ****
Three applications as described in the section "*Circuits and Simulation Procedure*"
**** Small signal bias solution Temperature = 27.000°C
****
Node Voltage Node Voltage Node Voltage Node Voltage
(1) 41.0130 (2) 10.0000 (3) 120.5100 (4) 170.5100
(5) 0.0000 (6) 0.0000 (7) 0.0000 (8) 0.0000
(9) 0.0000 (10) 0.0000 (11) 0.0000 (12) 0.0000
(13) 0.0000 (15) 0.0000 (21) 0.0000 (22) 0.0000
(23) 0.0000 (25) 0.0000 (27) 0.0000 (30) 0.0000
(31) 0.0000
Voltage source currents
Name Current
V20 6.203E-01
V109 0.000E+00
V110 0.000E+00
V2223 0.000E+00
V2530 0.000E+00
V3125 0.000E+00
V1512 0.000E+00
Total power dissipation -6.20E+00 WATTS
**** 10/20/24 18:24:00 ****** PSpice Lite (October 2012) ****** ID# 10813 ****

Three applications as described in the section "*Circuits and Simulation Procedure*"
**** Operating point information Temperature = 27.000°C
****
**** Voltage-controlled current sources
NAME GT GFFI
I-SOURCE 0.000E+00 0.000E+00
**** Voltage-controlled voltage sources
Name EFVX22 E270 ETFI E1213
V-source 0.000E+00 0.000E+00 0.000E+00 0.000E+00
I-source 0.000E+00 0.000E+00 0.000E+00 0.000E+00
**** 10/20/24 18:24:00 ****** PSpice Lite (October 2012) ****** ID# 10813 ****
Three applications as described in the section "*Circuits and Simulation Procedure*"
**** AC analysis temperature = 27.000°C
****
FREQ VM(22) VP(22)
1.000E+06 2.593E+00 7.015E+00
**** 10/20/24 18:24:00 ****** PSpice Lite (October 2012) ****** ID# 10813 ****
Three applications as described in the section "*Circuits and Simulation Procedure*"
**** AC analysis Temperature = 27.000°C
****
FREQ VM(30) VP(30) IM(V2530) IP(V2530)
1.000E+06 2.593E+00 7.015E+00 1.297E+00 -2.299E+01
Job concluded

DC linear electronic circuits with independent sources and circuit elements(resistors) were broken into two separate portions for the Thevenin equivalent circuit parameters [13–17] and were evaluated.

CONCLUSIONS

The Thevenin equivalent circuit parameters thus obtained are used in a representation by Spice-compatible analog behavioral modeling techniques, with the FREQ option of analog behavioral modeling in applications, as described in "*Circuits and Simulation Procedure"*. Examples are given as spin-software-compatible circuits, and the AC equivalent impedance between nodes is verified with conventional techniques. Different networks with temperature-dependent resistors could also be analyzed, and the DC Thevenin resistance could be converted and used as described in this article. By knowing the DC Thevenin resistance from other sources, we can also use the same technique. A non-linear network with suitable bias conditions can be analyzed for Thevenin resistance using conventional methods.

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