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Current Controlled Oscillator Using FinFET

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Abstract

A current-controlled oscillator using 18 nm FinFET technology is proposed in this study which consists of a Current Controlled Differential Difference Current Conveyor (CCDDCC) block to control the current. FinFET technology has better scalability and lower leakage current compared to traditional CMOS, which allows it to surpass the obstacles faced by CMOS-based oscillators. The suggested oscillator is suitable for electronic applications such as Phase-Locked Loop (PLL) systems, radio frequency (RF) communication systems, and many more, due to its linear current-to-frequency output with the help of the CCDDCC block. Detailed circuit simulations were performed with an 18 FinFET technology node, and the design was assessed based on the established increase in frequency range along with decreased power consumption. Analysis proved that there is lower power usage and better frequency stability compared to conventional CMOS based devices. The implementation of FinFET with sophisticated current control methods to develop scalable oscillators reveals new possibilities for the enhancement of low powered and high-performance devices.

Keywords: FinFET technology, current-controlled oscillator, current-controlled differential difference current conveyor, low power design, high-frequency oscillator, scalable circuit design, RF communication systems, nanometer technology nodes, oscillator circuit optimization

INTRODUCTION

Involutions in nanoscale technologies, especially in FinFET processes, have greatly improved the functionality of voltage-controlled oscillators (VCOs) in terms of frequency, power consumption, and phase noise characteristics [1–4]. From 3 to 45 nm FinFET nodes, researchers have implemented VCOs in varying ranges with each providing unique trade-offs with respect to complexity in design, range of tuning, and performance of noise [5–10]. Both Ring oscillators and LC-VCOs are popular choices while the performance was also significantly improved by newer topologies such as injection locked [11], phase interpolated [7], and quadrature [12].

SerDes, high speed I/Os, and secure hardware systems are just a few examples of underlining use case that drives the demand for advanced oscillators which are low-phase-noise, energy-efficient, dynamic in bandwidth, and convenient on the energy scale [2, 6, 13–16]. As the technology continues to enhance, the scaling of FinFETS leads to compact integration and reduction of these clutter as seen in PLLs [17], clock generators [11], and RC oscillators [16]. Multi-core [18] and current-controlled designs [19, 20] have shown the most likely candidates to increase tuning frequencies and linearity which enhance the application in modern communication and security systems.

Based on that, we propose in this study, a current controlled third order FinFET based oscillator using CCDDCC technique for high frequency stability, with added goal of ensuring process scalability.

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LITERATURE REVIEW

Modern electronics that need low power consumption and accurate frequency control depend on current-controlled oscillators. Cutting-edge technologies like FinFETs overcome the shortcomings of conventional CMOS designs, which have increased scalability, less leakage, and higher power efficiency. These developments make it possible to create oscillators with excellent performance and low energy consumption. The ensuing subsections review key ideas, current developments, and the research gaps this study fills.

Evolution of FinFET Technology

Because they produce steady clock signals, oscillators are essential for wireless communications, frequency synthesizers, and phase-locked loops [6]. Usually, they use a ring of inverting stages or an LC tank to measure frequency. Current-controlled or voltage-controlled techniques are used to control frequency. CCOs employ a control current to provide more linear tuning and reduced phase noise, which makes them perfect for high-precision applications. VCOs use a control voltage to change frequency.

Increased leakage, short-channel effects, and reliability problems have resulted from the shrinking of planar CMOS devices. With its multi-gate, three-dimensional structure, FinFET technology overcomes these obstacles by providing improved on-current and transconductance, less leakage, and superior electrostatic control [10]. Because of these benefits, FinFETs are already a major enabler for high-performance, energy-efficient circuits of the future.

CCDDCC Block in Oscillator Design

For accurate frequency tuning in current-controlled oscillators, the CCDDCC block is crucial because it transforms the incoming control current into a proportional delay. In order to guarantee a linear relationship between the control current and delay, it usually consists of a voltage-to-current stage, a delay element (such as an RC circuit or current-starved inverter), and a current-to-voltage stage [20]. According to recent research, adding FinFET technology to CCDDCC designs decreases leakage, increases transconductance, and improves electrostatic control, which results in improved linearity, a wider tuning range, and less power consumption [10].

Gaps in Existing Research

In the paper [20] there is implementation of similar current controlled third order oscillator, even though they have achieved the functional performance of the oscillator but the power consumption and frequency range can be improved further, so for addressing the high power consumption and low frequency range we have used 18 nm FinFET technology instead of 180 nm, which has given us improvements in both power consumptions and frequency range.

Table 1 tabulates the key performance differences between 180 nm CMOS and 18 nm FinFET technology.

THEORETICAL BACKGROUND

Current-controlled oscillators (CCOs) produce signals with frequencies that correspond to an input control current. They implement a delay cell, consisting of a current-to-voltage amplifier, a delay block, and a voltage-to-current amplifier, in feedback configuration [8]. The delay element, which is commonly referred to as a current controlled delay-discrimination-and-conversion block, adds a time interval proportional to the input control current. This part describes the principles of CCOs, advantages of FinFET technology, and the contribution of the CDDDCC block to accurate current control.

Table 1. Key performances differences of different technologies.

Performance Metrics	180 nm CMOS	18 nm FinFET
Power Consumption	0.42 mW	9.7 nW
Frequency	2.8 MHz	4.16 MHz

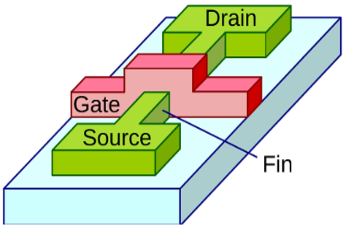

Figure 1. Structure of FinFET.

FinFET Technology

With outstanding performance and low power consumption, it exhibits advanced scalability that makes FinFET a likely candidate to replace traditional CMOS technology. Its unique 3D structure offers remarkable electrostatic control which further improves the on/off current ratios and reduces the impact of short-channel effects (Figure 1). In addition, the vertical structure facilitates high frequency operation by increasing carrier mobility and lowering parasitic capacitance which allows further miniaturization of electronic devices [5].

The poly-silicon gate FinFET transistors with a vertical fin channel have better control for short channel effect self-electrostatic biasing due to enhanced carrier mobility, lowered parasitic capacitance, reduced off current, and raised on current, all of which enable effortless operation at sustained high frequency. In addition, they are easier to scale, which is particularly useful in miniaturizing applications such as precise instrumentation, advanced timing circuitry, and wireless communications.

Compared to the traditional CMOS technology, FinFET offers considerable benefits:

a. Its wraparound gate with an actualized 3D fin structure increases on/off current efficacy and ameliorates short-channel challenges through better electrostatic control [4].
b. The vertical architecture allows greater carrier mobility while reducing parasitic capacitance which increases energy efficiency and high-frequency performance for more sensitive instruments and wireless communication [5].

These are only a few factors that stimulate the preference of utilizing FinFET over CMOS to build an oscillator.

CCDDCC Block

The CCDDCC block, located at the center of a current-controlled oscillator, converts the control current into a proportional time delay to achieve correct frequency tuning. It is made up of a feedback loop with a voltage to current converter, a delay element, and a current to voltage converter (Figure 2). A particular amount of delay that gets shorter with increasing current and longer with decreasing current is added by the delay element, after which the current is converted into voltage. Finally, the voltage is converted back to current. This method allows for fine control of the oscillator's output frequency.

Current Controlled Oscillators

Precision instrumentation, clock generation, and wireless communications especially for frequency synthesis depend on current controlled oscillators (CCOs). They operate by altering the modulating control current, which in turn adjusts the oscillation frequency. The resulting tuning is accurate as per requirement. Performance is boosted alongside power efficiency and lowered phase noise due to the enhanced carrier mobility, lowered parasitic capacitance, and greater electrostatic control in FinFET integrated CCOs. Additionally, these factors contribute to raising frequency stability and improving noise margins.

MATHEMATICAL MODELLING

The mathematical modelling and analysis of FinFET-based current-controlled oscillators can be approached using well-established circuit analysis. We need to analyse the circuit in Figure 3 to get the frequency of oscillations (FO). The main goal behind this mathematical modelling of the oscillator is to find a relation between the reactive elements and the frequency, this in turn helps in controlling the frequency with the help of input current as CCDDCC helps in controlling the values of the reactive elements with the help of input current and hence the delay from those reactive elements helps in calculating the frequency of oscillations.

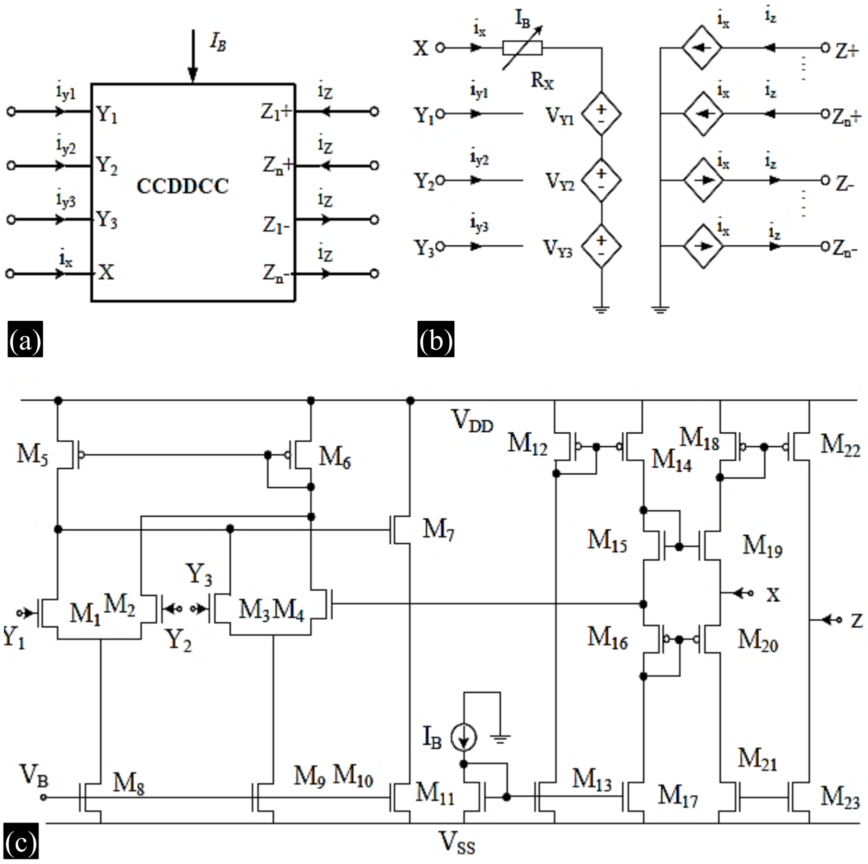

Figure 2. CCDDCC (a) Circuit symbol (b) equivalent electrical circuit (c) CMOS implementation.

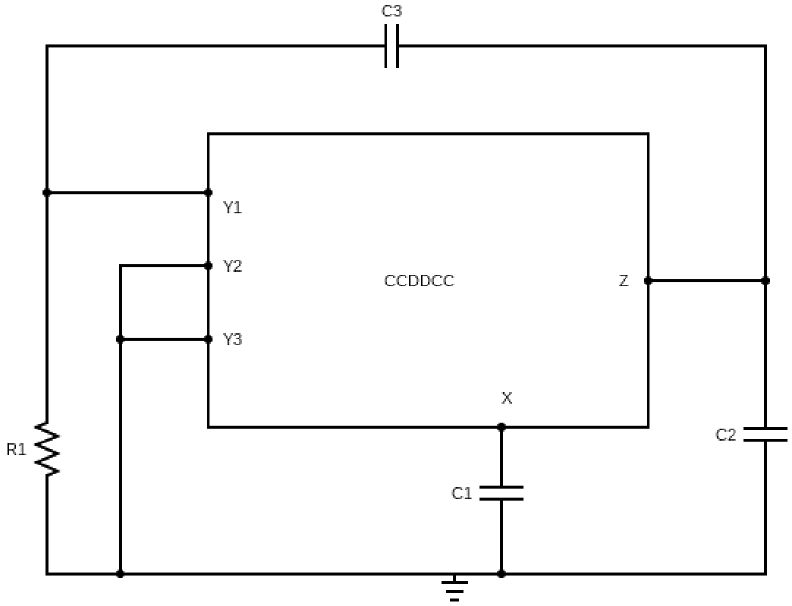

Figure 3. Circuit diagram of proposed oscillator.

Applying KCL (Kirchhoff Current Law) at node 1 of the circuit in Figure 3:

$$I_1 + I_2 + I_3 = 0 \tag{1}$$

As $I_1 = 0$ in the circuit, so Eq. (1) will be:

$$I_2 = -I_3 \tag{2}$$

Using Ohm's law in Eq. (2) we will get:

$$\frac{V_{Y1}-V_Z}{\frac{1}{SC_3}} = -V_1/R_1 \tag{3}$$

On solving Eq. (3):

$$V_{Y1} = V_Z SC_3R_1/(1 + SC_3R_1) \tag{4}$$

At node Z, using Ohm's law we will get:

$$I_Z = SC_2V_Z \tag{5}$$

Applying Ohm's law at node X we will get:

$$I_X = SC_1V_X \tag{6}$$

We have $I_X = \pm I_Z$ from [20] so from Eqs. (5) and (6) we will have:

$$SC_1V_X = SC_2V_Z \tag{7}$$

On solving the Eq. (7) we will get:

$$\frac{V_Z}{V_X} = \pm C_1/C_2 \tag{8}$$

We have $V_X = I_XR_X - V_{Y1} - V_{Y2}$ from [20], so putting the values from Eqs. (6) and (4) and $V_{Y2} = 0$ we will get:

$$V_X = SC_1V_XR_X - V_ZSC_3R_1/(1 + SC_3R_1) \tag{9}$$

Solving Eq. (9) we will get:

$$\frac{V_Z}{V_X} = (SC_1^2R_X + S^2C_1C_3R_1R_X)/(C_2 + SC_2C_3R_1 + SC_1C_3R_1) \tag{10}$$

Solving Eqs. (8) and (10) together we will get:

$$S^2C_1C_3R_1R_X + SC_1C_2(C_1R_X - C_1C_3R_1 - C_3R_1) - C_1C_2 = 0 \tag{11}$$

Putting $S = jw$ where w is the angular frequency, in Eq. (11) we will get:

$$-\left(1 + \frac{w^2C_3R_1R_X}{C_2}\right) + jw\left(C_1R_X - \frac{C_1C_3R_1}{C_2} - C_3R_1\right) = 0 \tag{12}$$

The real part of the Eq. (12) is:

$$\left(1 + \frac{w^2C_3R_1R_X}{C_2}\right) = 0 \tag{13}$$

The imaginary part of Eq. (12) is:

$$w = \frac{1}{\left(C_1R_X - \frac{C_1C_3R_1}{C_2} - C_3R_1\right)} \tag{14}$$

On solving Eqs. (13) and (14) together, we will get:

$$w = C_2/(C_1C_2R_X - C_1C_3R_1 - C_3R_1) \tag{15}$$

Now we will get the frequency of oscillations (FO) from this angular frequency in Eq. (15)

$$FO = C_1/2\pi(C_1C_2R_X - C_1C_3R_1 - C_3R_1) \tag{16}$$

Hence, we have derived the equation for calculating the frequency of oscillations of current controlled third order oscillator using FinFET. This expression will help us to calculate the frequency of the oscillator also this expression tells us how the values of resistances and capacitances affect the oscillator frequency, hence the frequency is controlled by the values of reactive elements and hence by the input current to the circuit.

PROPOSED DESIGN AND METHODOLOGY

The proposed current-controlled oscillator using 18 nm FinFET technology can be divided into the following key components:

Design of the CCO Circuit

The oscillator is designed as a third order with three capacitors and a resistor that are external to the CCDDCC block. This block turns an input control current into a time delay that is proportional to some modulating signal and bass-modulates the oscillator. Thus, the emission frequency can be finely adjusted. In the amplifier stage, the use of FinFET transistors also improves electrostatic control, mobility of the carriers, and overall stability of the frequency, while the phase noise is reduced. This approach, along with the baffling integration of the CCDDCC block maximally provides current control, creates a highly efficient and tunable oscillator for wireless communication, clock generation, and precision instrumentation.

Implementation Using FinFET

A current-controlled oscillator is achieved with high performance targeted using a 18 nm FinFET process in the technology. Because FinFETs are built with 3D double-gate structure, they have greater static control and transport of carriers, so unlike planar MOSFETs, they are more stable at higher frequencies, have less phase noise, and consume less power [2, 4]. The number of fins, fin height, and gate length are some of the various device level parameters that determine a certain region for the output frequency range, power, and filter the noise efficiently. The oscillator core has FinFET based on the issued Control Blocks. The active delay line amplifiers having a CCDDCC configuration whose primary function is to transform the input control current into a corresponding time delay for accurate phase tuning. This approach is integrated in nature and, as verified by survival analysis within Cadence Virtuoso, settles on low-area and high-performance oscillator requirements.

Performance Metrics

While estimating the effectiveness of the proposed current-controlled oscillator topology, one is able to take into account a set of important metric targets.

Power Consumption

One of the static measures of power efficiency includes minimizing the static energy for cyclic operations without producing any active work within the system. This, coupled with system level optimizations, significantly increases the energy efficiency and lifetime of the battery. The combination of advanced biasing techniques, appropriate circuit topology, and optimization of various FinFET parameters such as quantity of fins, fin height, and gate length leads to considerable static power savings in the oscillator circuitry.

Frequency Range and Tuning Capability

The oscillator's broad frequency range and accurate tuning are important performance indicators. In order to provide wide frequency coverage and dynamic adjustment through the control current, the design optimizes the oscillator core and the delay modulation block, guaranteeing precise frequency modulation and control. The frequency range should significantly increase with the use of FinFET.

METHODOLOGY

When designing a current-controlled oscillator using FinFET technology, the methodology can be broadly divided into the following steps:

Defining Design Goals

The primary design goal is to develop a current-controlled third-order oscillator using 18 nm FinFET technology. To achieve stable performance, we start with a baseline model in 180 nm CMOS, then scale to a 45 nm node adjusting R, C, bias current, and input voltage accordingly. Once the 45 nm design yields satisfactory results, we transition to 18 nm technology and further optimize these parameters for the final oscillator implementation.

Schematic Design

The next step is to create a schematic for the current controlled third order oscillator, here we are using CCDDCC block for implementing the current controlling and we are using around 22 transistors for implementing the whole oscillator, the basic schematic is same for all the technology nodes; the only difference is in the values of different components like the resistance and the capacitances and the values of bias current and the input voltage supply which we are carefully adjusting to get a stable and sustainable output. Figure 4 shows the schematic of the proposed third order oscillator implemented using the 18 nm FinFET technology.

Baseline Design at 180 nm

First we have implemented this schematic design for 180 nm CMOS technology node, we have tuned the values of R, C1, C2, C3 and the values of the Bias current and the Input voltage from the circuit diagram in Figure 4 for achieving a stable and sustained output oscillations from the oscillator, we have not made any changes to the CCDDCC block as it is just controlling the oscillating frequency via current. Table 2 shows the most appropriate values of these parameters for this third order oscillator to work.

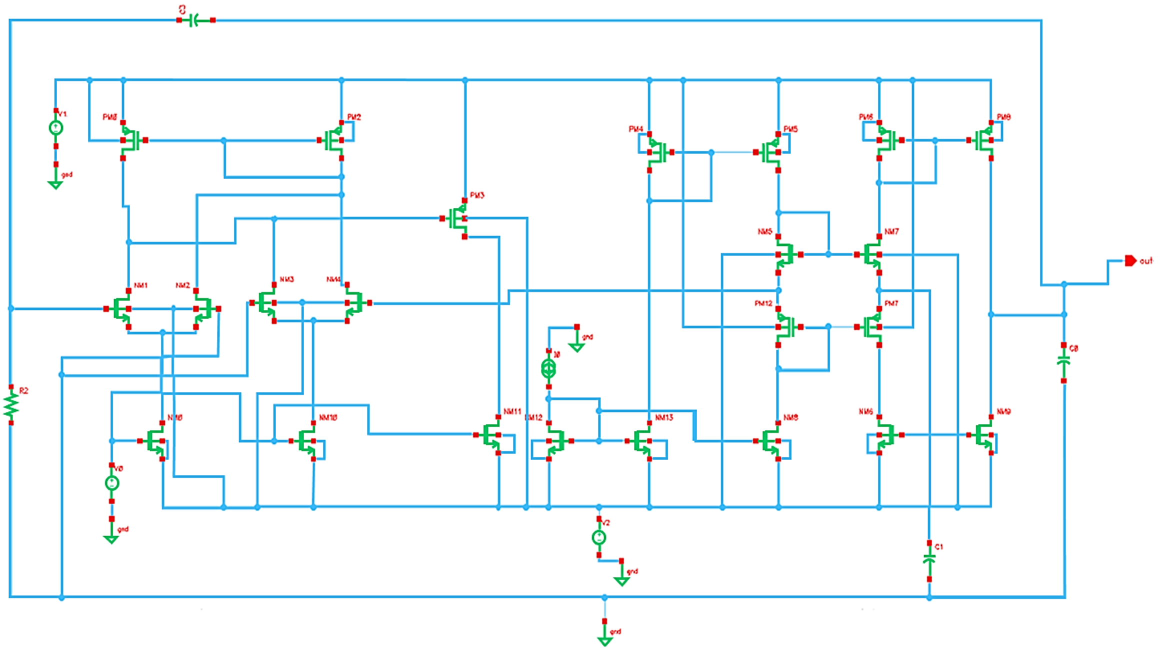

Figure 4. Schematic diagram of proposed oscillator using 18 nm FinFET Technology.

Table 2. Parameters for 180 nm design.

Parameter	Values
Resistance (R)	2 kΩ
Capacitance (C1)	100 pF
Capacitance (C2)	10 pF
Capacitance (C3)	10 pF
Bias Current (Ib)	5 µA
Input Voltage (Vdd)	1.25 V

R, C, Bias Current and Voltage Supply Optimization and Scaling Strategy

The next step after the successful implementation of the 180 nm oscillator is to scale down the technology node to 45 nm and then to 18 nm; but for that we also need to tune the parameters of the circuit accordingly. There are some strategies for tuning the values of parameters from 180 to 45 nm and then to 18 nm, and following are some ways you can scale down the values of the parameters of the 180 nm oscillator to get a sustained and stable output from the scaled down technology nodes.

Step 1: Optimization for 45 nm

Tuning the values of parameters for getting the performance from 45 nm technology node is crucial as it is the second step in order to achieve the 18 nm. For implementation of the basic starting point for getting the values for parameters like R, C1, C2, and C3 we need to divide these values by the ratio of the size of technology nodes, like in this case, we can divide by 180:45 which is 4 and then check for the output, if the output is not convincing then you can tweak the values in either direction to get a convincing output, this tweak should also be performed in the values of bias current and the voltage supply for setting the perfect values for those parameters too. After a lot of experimentation with different values for these parameters we have reached the final values for parameters shown in Table 3.

Step 2: Optimization for 18 nm

Here we are tuning the parameters for getting the descent output for the implementation of current controlled third order oscillator using 18 nm FinFET technology. Here we start by dividing the values of the capacitances with square of the ratio of the technology node sizes, in this case it is 180:18 squared, which is 100, hence we will divide the values of capacitances from 180 nm by 100 and then tune them further to get the best values for the capacitances. We also decrease the values of the resistance to get the perfect value for the resistance for which we get the convincing output, then finally we will set the values for the bias current and voltage supply; here the values of the input voltage should be pretty low as we are using FinFET which operates at low input, hence after all these tunings we get the best values for all the parameters to get the our final output for the third order oscillator implemented using 18 nm technology. The values for the parameters are shown in the Table 4.

Performance Metrics and Comparative Analysis

The main performance metrics for the oscillators have already been discussed above and we need to calculate these performance metrics for all three technology nodes.

Table 3. Parameters for 45 nm design.

Parameter	**Values**
Resistance (R)	2 kΩ
Capacitance (C1)	20 pF
Capacitance (C2)	1 pF
Capacitance (C3)	150 pF
Bias Current (Ib)	200 µA
Input Voltage (Vdd)	0.9 V

Table 4. Parameters for 18 nm design.

Parameter	**Values**
Resistance (R)	1.5 kΩ
Capacitance (C1)	300 fF
Capacitance (C2)	60 fF
Capacitance (C3)	60 fF
Bias Current	210 µA
Input Voltage (Vdd)	0.4 V

Power Consumption Calculation

The first metric is the power consumption of the circuit; here we are calculating the static power of the circuit and the way we are calculating the power is as follows:

- *Step 1:* First, we perform the DC analysis on our circuit for each technology node; this will give us the leakage current present in the circuit which is the combination of gate current and other form of leakage current.
- *Step 2:* Now as we have the leakage current, we can calculate the static power consumption of the oscillator by simply multiplying the leakage current with the input voltage for that particular technology node.

Frequency Range

Frequency range is an important parameter for the evaluation of the oscillator and we can calculate the frequency range of the oscillator using the output of mathematical modelling section which is the formula for frequency of oscillations (FO) and hence compare the frequency range of the 18 nm oscillator with the frequency of higher technology nodes from [20].

RESULTS AND DISCUSSION

The following section will discuss the results of the study; the main focus would be the oscillations generated by the oscillator, as we have discussed in the previous section that how we are scaling down the technology node gradually from 180 nm to reach the 18 nm technology node and we have made the oscillator work for each node and had achieved a descent output oscillation for each technology node including for the final 18 nm technology node. Later in this section we will see the comparison of different performance metrics of different technological nodes; and we have achieved improvements in multiple performance metrics.

Output Oscillation Waveform

This section will show the different output waveforms for the oscillators implemented in different technology nodes. Here are the output oscillations for different technology nodes. The two waveforms in Figures 5 and 6 show the output of the current-controlled third-order oscillator using 180 and 18 nm technology node, respectively. Here we can see that we get a perfect sustained oscillation in case of 180 nm and that works as the motivation or the aim to be achieved using 18 nm technology node. Hence for achieving these types of sustained and stable output waveforms we had tuned the values of the parameters for the 18 nm implementation of technology node. After a lot of experimentation, we achieved the waveform in Figure 6 which shows how we have achieved sustained and stable oscillations from the oscillator implemented using FinFET.

Table 5 shows the different performance metrics for different oscillators implemented using different technology nodes. The power consumption decreases significantly as we move towards smaller technology nodes; this is due to the fact that the leakage current is significantly decreased in case of FinFET and hence the power consumption also decreases significantly; this means the oscillator implemented using the 18 nm FinFET technology is much power efficient than the other technology nodes; this acts as one of the most important advantages of the 18 nm technology node over the traditional technologies. We can also see a significant increase in the frequency range as we go from higher technology nodes towards the lower technology nodes; this is due to reduced time delay in case of FinFET's implementation of oscillator. This also acts as an advantage of the FinFET implementation as we can use a smaller chip and still can achieve a greater frequency range which is crucial in case of RF communication.

APPLICATIONS

Software-Defined Radios (SDR)

Without requiring hardware changes, its broad frequency tuning range allows for smooth integration with a variety of wireless protocols, including 5G, Wi-Fi, and Bluetooth, guaranteeing agile switching and maximum spectrum efficiency. It is perfect for radio frequency (RF) transmission due to its wide frequency.

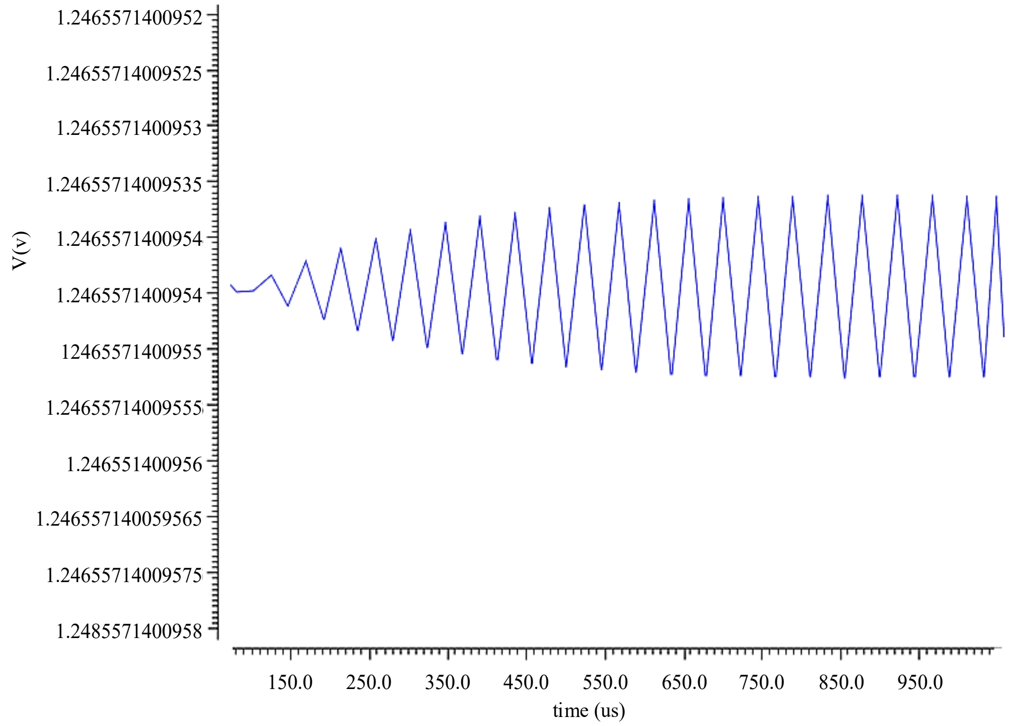

Figure 5. Output waveform for 180 nm.

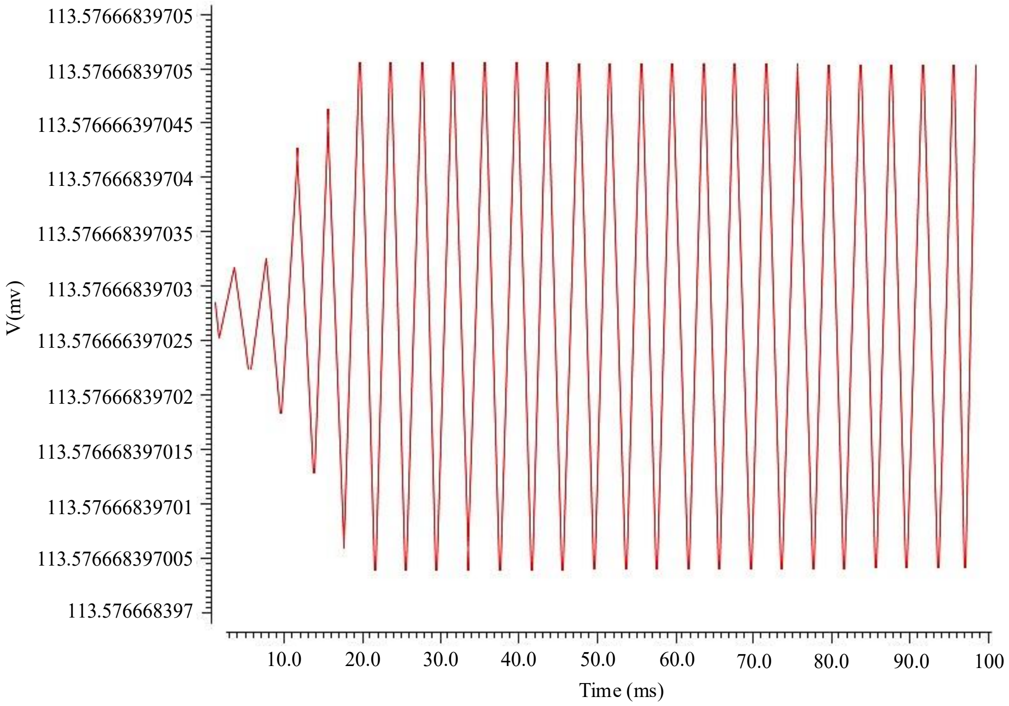

Figure 6. Output waveform for 18 nm FinFET.

Table 5. Performance metric comparison table.

Technology Nodes	Power Consumption	Frequency Range
180 nm	0.402 mW	2.8 MHz
45 nm	0.126 mW	4.2 MHz
18 nm	0.0097 mW	4.168 MHz

IoT Devices

The low power consumption of the oscillator implemented using FinFET makes it ideal for IoT applications. IoT devices are generally low power devices but they also need to communicate, so an oscillator with this small power usage can be vital. Also, the IoT devices demand a high power efficiency as they are often used all day along and hence a oscillator which is highly power efficient is an important deal for IoT devices.

Clock Generation

Clock generation is one of the main applications of any type of oscillator, and on top of that if the oscillator is small in size, it gives one more advantage for implementing clock generation in size constrained environment. Also, a great noise performance of our oscillator can be an important factor for choosing this over the traditional oscillators for the clock generation. A low phase noise and a high frequency range makes this third order oscillator implemented using makes it a perfect choice for clock generation.

CONCLUSION

The proposed 18 nm FinFET-based current-controlled oscillator achieves significant improvements over traditional implementations. Compared to 180 and 45 nm designs, it demonstrates reduced power consumption, operating at just 0.009 mW, making it highly efficient for power-constrained applications. Additionally, the oscillator offers an expanded frequency range of up to 4.1 MHz surpassing conventional implementations of the oscillators using the 180 and 45 nm technology nodes, and enabling seamless multi-standard wireless communication. A carefully optimized design ensures sustained oscillations with stable phase noise performance, making it a reliable choice for advanced RF and digital systems. These advancements highlight the potential of FinFET technology for high-performance, energy-efficient oscillator design.

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