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Delay Analysis of HS-14T 45 nm CMOS SRAM with Different SRAM Techniques for Improvement in Speed

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Abstract

This study presents a novel HS-14T design aimed at significantly improving read and write delays compared to conventional 6T and other memory cells RHRD-12T, SEUH-12T, and NHRC-14T. As technology scales, the demand for faster and more stable memory cells becomes increasingly critical. Our proposed HS-14T incorporates additional transistors to enhance stability and reduce access times, resulting in notable performance gains. Comprehensive simulations reveal that the HS-14T SRAM cell substantially reduces read and write delays, outperforming traditional 6T, RHRD-12T, SEUH-12T, and NHRC-14T SRAM cells. Specifically, the HS-14T demonstrates an impressive 80% reduction in read delay compared to NHRC-14T, an 88% reduction compared to RHRD-12T, and an 89% reduction compared to SEUH-14. In terms of write delay, the HS-14T shows a 66% reduction compared to NHRC-14T, a 98.75% reduction compared to RHRD-12T, and a 25% reduction compared to SEUH-14. Additionally, the HS-14T exhibits an 18% decrease in leakage current compared to RHRD-12T and a 1.63% decrease compared to SUEH-12T, though it shows a 55% increase compared to NHRC-14T. The software used for simulations is Symica DE, and the technology node is 45 nm. This study highlights the HS-14T SRAM's potential for significantly enhanced performance and productivity in various computing systems, making it a compelling choice for applications where rapid data access and energy efficiency are paramount.

Keywords: SRAM cell, read delay, write delay leakage current, Symica DE, minicomputers, cache memory

INTRODUCTION

SRAM is increasingly essential due to the growing demand for small, portable electronics such as cell phones and minicomputers. These devices are equipped with fast microprocessors that rely on cache memory for quicker data access. To enhance performance and functionality, Static Random Access Memory must function effectively as cache memory [1–3].

SRAM is also well-suited for battery-powered devices like wireless sensors and biomedical equipment, where battery life and power efficiency are critical considerations. Many smart gadgets, owing to their multifunctionality, have lower power consumption [4–8].

Thousands of transistors are configured in a very large scale integration (VLSI) on a single chip with a minimal surface area [9]. A key factor is the low power consumption of portable devices [10]. Multiple SRAM cells are used to form an array

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capable of storing large amounts of data. Memory occupies a significant portion of the chip system. The increase in transistor size necessitates new technologies. While this leads to higher leakage current, it helps reduce the cell area, thereby shrinking the SRAM size and improving integration density [11–16]. Leakage is a concern in all cells, and multiple-cell SRAM arrays can significantly contribute to leakage current. Voltage scaling and smaller device dimensions in upcoming technology generations create data stability challenges in SRAM cells [17–19].

The evolution of SRAM (Static Random Access Memory) technology is driven by the increasing demands for higher speed, lower power consumption, and greater stability in modern electronic devices. As technology nodes shrink, particularly down to 45 nm and beyond, the challenges associated with leakage current, read and write delays, and overall cell stability become more pronounced. The HS-14T design emerges as a promising solution to these challenges, incorporating advanced techniques to mitigate leakage and optimize performance. In recent years, various SRAM architectures, including the traditional 6T, as well as more complex designs, have been explored to enhance read/write stability and speed. These designs, while effective to varying degrees, often involve trade-offs between power consumption, area overhead, and performance. The introduction of HS-14T aims to address these trade-offs by providing a more robust framework for high-speed and low-power applications. Previous studies have highlighted the importance of optimizing read and write delays to achieve better speed and stability in SRAM cells. For instance, research on subthreshold SRAM operation emphasizes the need for careful management of delay parameters to ensure reliable performance under low voltage conditions. Another study focusing on leakage current reduction in CMOS SRAM cells demonstrates the critical role of minimizing static power dissipation to enhance overall cell efficiency.

This study presents a comprehensive delay analysis of an HS-14T CMOS SRAM cell designed using 45 nm technology, comparing it with other SRAM cells RHRD-12T, SEUH-12T and NRHC-14T to highlight improvements in speed and stability. By leveraging advanced circuit design methodologies, the HS-14T aims to achieve superior performance metrics, making it a viable candidate for next-generation memory applications.

The importance of read delay and write delay in SRAM cells is crucial for optimizing both speed and stability. Read delay, or read access time, is the duration required to read data from the SRAM, impacting overall speed. Write delay is the time needed to write data, influencing both speed and stability of the SRAM operation.

Reducing read and write delays improves the performance of SRAM cells by enabling faster data access and write operations, which is vital for high-speed applications. Moreover, optimizing these delays enhances the stability of SRAM cells by minimizing errors during read and write cycles, thereby increasing reliability.

The read delay of an SRAM cell refers to the time it takes for the cell to output valid data after a read operation is initiated. It is crucial because it determines the speed at which data can be accessed from the memory. Similarly, the write delay of an SRAM cell is the time it takes for the data to be successfully written into the cell and stabilized. This parameter is important as it affects the speed at which data can be written into the memory.

In the proposed HS-14T SRAM cell with a read delay of 1 ps and a write delay of 5 ps, these values indicate extremely fast operation as shown in Figure 1. A read delay of 1 ps means that after initiating a read operation, the data becomes available in just 1 ps, and a write delay of 5 ps implies that data can be written and stabilized within 5 ps. Such fast read and write delays are highly desirable in applications where rapid data access and processing are essential, such as high-speed computing, real-time signal processing, and advanced communication systems.

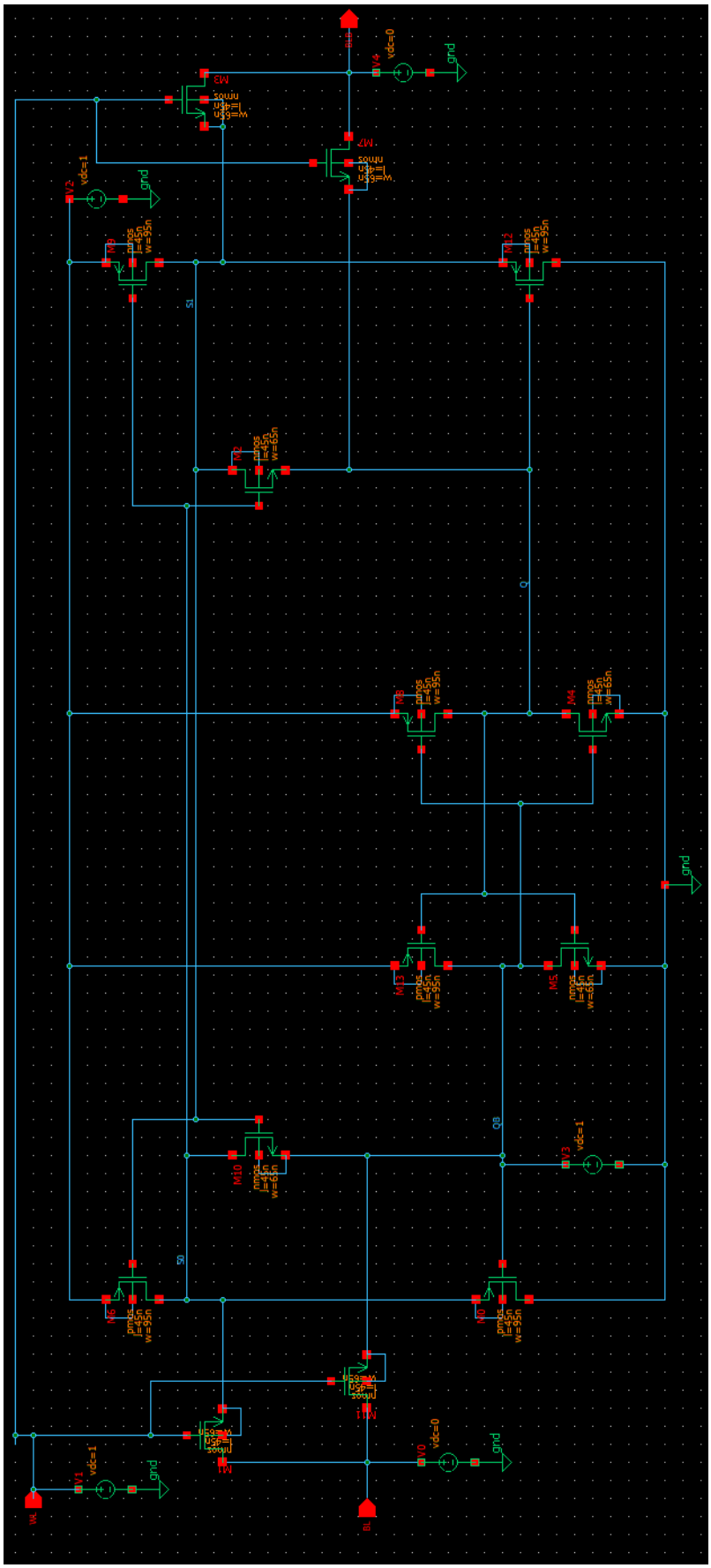

Figure 1. Proposed 14 T SRAM cell.

Leakage current in an SRAM (Static Random Access Memory) cell refers to the small electric current that flows through the transistors within the cell, even when the cell is not actively performing read or write operations. This current occurs due to various physical phenomena, such as subthreshold leakage, gate leakage, and junction leakage, which result from imperfections in the semiconductor materials and fabrication processes. Leakage current is a significant concern in SRAM cells because it contributes to standby power consumption, which can drain battery life in portable devices and increase power usage in larger systems. High leakage currents can also lead to data instability, as they may cause unintended changes in the stored data over time. Therefore, minimizing leakage current is essential to optimize power efficiency, ensure data integrity, and enhance the overall performance and reliability of SRAM-based memory systems. Leakage current in SRAM cells, including the proposed HS-14T with a measured leakage current of 48.24 μA.

PROPOSED HS-14T SRAM CELL AND ITS TRANSIENT ANALYSIS

Proposed HS-14T SRAM Cell

The HS-14T SRAM cell includes four storage nodes: Q, QB, S0, and S1. These nodes respectively hold the values '0', '1', '0', and '1', with Q and QB being complementary, as well as S0 and S1. S0 and S1 are also known as restoring nodes.

Hold Mode

In hold mode, the wordline (WL) is set to a low logic level (0), which turns off the access transistors M1, M11, M3, and M7. During this time, the bitline (BL) and bitline bar (BLB) are pre-charged to Vdd. The circuit maintains the values at Q, QB, S0, and S1. Transistors M13, M5, M8, and M4, along with M6, M9, M10, and M2, are in latch mode, ensuring the data remains stable.

Read Mode

In read mode, the wordline (WL) is set to a high logic level (1), activating access transistors M1, M11, M3, and M7. The bitline (BL) and bitline bar (BLB) are pre-charged, with BL set to 1 and BLB to 0. BLB connects to ground and discharges through M7 and M12, allowing the sense amplifier to read the value as '0' without altering the stored data.

Write Mode

During write mode, the wordline (WL) is activated, enabling data writing to the memory cell. If the cell holds a logic 1 and needs to be changed to a logic 0, BL and BLB are connected to ground and Vdd, respectively. This action turns on the pull-up transistors and turns off the pull-down transistors, effectively writing the new value into the cell.

HS-14T Memory Cell Performance Parameters Evaluations and Comparison

Read Delay

The term read access time or read delay (τr) denotes the time needed to attain a minimum potential difference of 50 mV across the bit-lines, relative to half the increase in word-line voltage time [20]. This read access time is primarily influenced by the bit-line capacitance and the read current of the memory cell [21]. The proposed HS-14T SRAM presents a significant breakthrough in-memory technology, particularly in terms of read delay reduction when compared to several established SRAM types. Specifically, compared to the NHRC-14T SRAM, the HS-14T demonstrates an impressive 80% decrease in read delay, indicating substantially faster read operations. Furthermore, when contrasted with the RHRD-12T SRAM, the HS-14T showcases an outstanding 88% decrease in read delay, significantly enhancing data retrieval speed. Additionally, compared to the SEUH-14 SRAM, the HS-14T exhibits an impressive 89% decrease in read delay, further highlighting its superior performance in terms of access time [22, 23]. Read delay or access time, is a critical parameter in memory design, representing the time taken to retrieve data from the memory cell. Minimizing read delay is essential for improving overall system performance, enabling faster data access and response times. By evaluating the read delay of the HS-14T SRAM relative to other SRAM types, we gain valuable insights into its speed and efficiency, making it a compelling choice for applications where rapid data access is

paramount. This comparison helps to elucidate the advantages of the HS-14T SRAM and its potential impact on future semiconductor designs, paving the way for enhanced performance and productivity in various computing systems.

Write Delay

Write access time (τw) is another key performance metric for memory cells. It refers to the duration needed for half of the word-line voltage rise to reach the junction of the two storage nodes [20]. This write access time is determined by the drive capability, feedback channel length, and the capacitance of the storage node. The proposed HS-14T SRAM marks a significant advancement in memory technology, particularly in terms of reduced write delay when compared to several existing SRAM types. Compared to the NRHC-14T SRAM, the HS-14T demonstrates an impressive 66% decrease in write delay, indicating substantially faster write operations. Furthermore, when contrasted with the RHRD-12T SRAM, the HS-14T showcases an outstanding 98.75% decrease in write delay, significantly enhancing data writing speed. Additionally, compared to the SEUH-14 SRAM, the HS-14T exhibits a notable 25% decrease in write delay, further underscoring its superior performance in terms of write speed. Write delay, or write access time, is a critical parameter in memory design, representing the time taken to write data into the memory cell. Minimizing write delay is essential for improving overall system performance, enabling faster data storage and processing. By evaluating the write delay of the HS-14T SRAM relative to other SRAM types, we gain valuable insights into its efficiency and speed, making it a compelling choice for applications where rapid data writing is essential. This comparison highlights as shown in Figure 2 the advantages of the HS-14T SRAM and its potential impact on future semiconductor designs, paving the way for enhanced performance and productivity in various computing systems.

Calculation of read delay, write delay and leakage current of proposed HS-14T SRAM cell with other SRAM cells (NRHC-14T, RHRD-12T and SEUH-12T) is shown in Table 1 and graphically shown in Figure 3.

PREVIOUS SRAM CELLS

Reff 01: NRHC 14-T simulation preseneted in Figure 4.
Reff 02: RHRD T2 12-T as dicussed in Table 1 can be easily understood by the Figure 5.
Reff 03: SEUH 12-T characteristics discussed in Table 1 and shown in Figure 6.

Leakage Current

Leakage current in an SRAM (Static Random-Access Memory) cell is the small, unintended current that flows through the transistors even when they are in an off state. This current results from various leakage mechanisms such as sub-threshold conduction, gate oxide tunneling, and reverse-biased junction leakage. Leakage current is an important factor in the overall power consumption and reliability of SRAM cells, as it can lead to increased energy usage and potential data retention issues. The proposed HS-14T SRAM introduces a significant advancement in memory technology, offering improvements in leakage current compared to several existing SRAM types. Specifically, when compared to the NRHC-14T SRAM, the HS-14T exhibits a substantial 55% increase in leakage current as shown in Figure 7, indicating a higher level of current flow in standby mode. However, in comparison to the RHRD-12T SRAM, the HS-14T demonstrates an 18% decrease in leakage current, showcasing enhanced efficiency and reduced power consumption. Furthermore, when contrasted with the SUEH-12T SRAM, the HS-14T showcases a 1.63% decrease in leakage current, further enhancing its energy-saving capabilities. Leakage current is a crucial factor in semiconductor device design, as it represents the current that flows through a transistor even when it is in the off state. Minimizing leakage current is essential for improving power efficiency and prolonging battery life in portable devices. By evaluating the leakage current of the HS-14T SRAM relative to other SRAM types as presented in Table 2, we gain insights into its energy efficiency and suitability for various applications. This comparison enables us to identify the strengths and weaknesses of the HS-14T SRAM in terms of power consumption, ultimately guiding its deployment in future semiconductor designs.

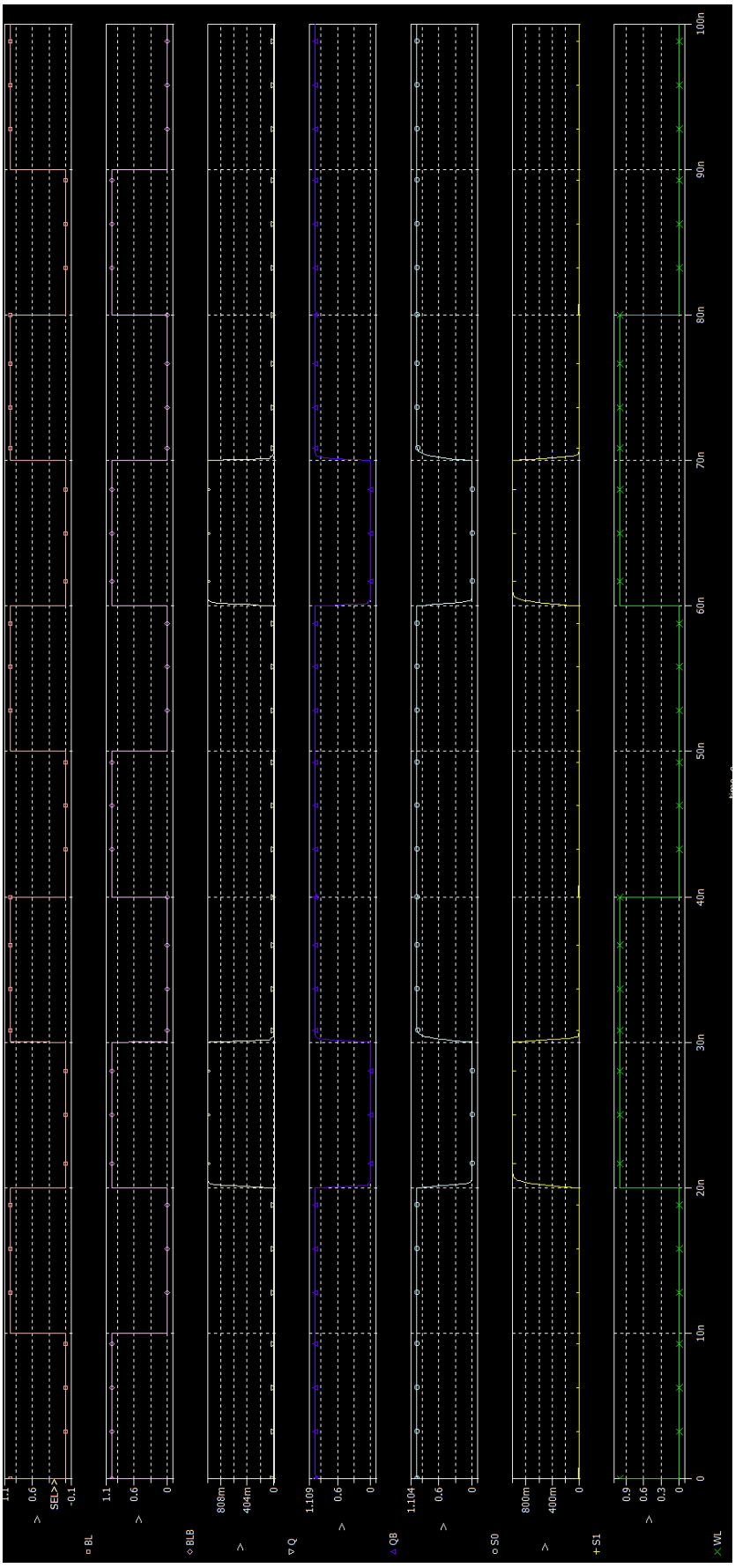

Figure 2. Transient analysis of proposed HS-14T.

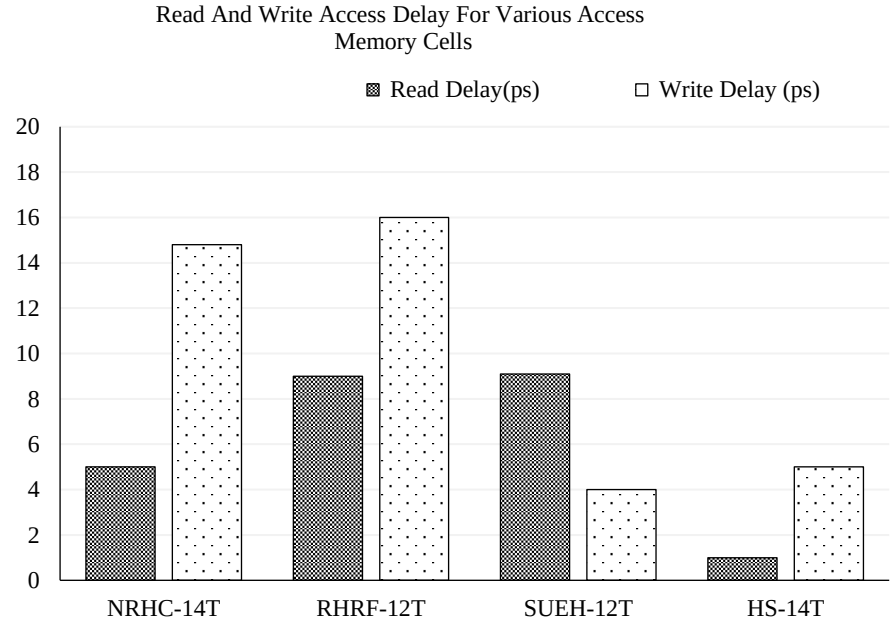

Figure 3. Read delay and write delay comparison of SRAM.

Table 1. Parameters of HS-14 Proposed SRAM cell.

Parameters	**HS-I4 T Proposed SRAM cell**
Read Delay (ps)	WL=20.03 ns Q=20.029 ns Read Delay (Total): Q-WL=20.029–20.03=1 ps
Write Delay (ps)	WL=20.030 ns Q=20.0135 ns Write Delay (Total): Q–WL=20.0135–20.030=5 ps
LC (μA)	46.24
Reff 01. NRHC-14T SRAM Cell	
Read Delay (ps)	WL=20.029 ns Q=20.024 ns Read delay (Total) Q–WL=20.029–20.24=5 ps
Write Delay (ps)	WL=20.029 ns Q=20.015 ns Write Delay=WL–Q=20.029–20.015=14.8 ps
LC (μA)	31 μA
Reff 02. RHRD-12T SRAM Cell	
Read Delay (ps)	WL=20.030 ns Q=20.021 ns WL-Q=20.030–20.021=9 ps
Write Delay (ps)	WL=20.030 ns Q=20.014 ns WL-Q=20.030–20.014=16 ps
L.C. (μA)	59 μA
Reff 03. SEUH-12T SRAM Cell	
Read Delay (ps)	WL=20.030 ns Q=20.02 ns WL-Q=9 ps
Write Delay (ps)	WL=20.030 ns Q=20.026 WL-Q=20.030–20.026=4 ps
LC (μA)	49 μA

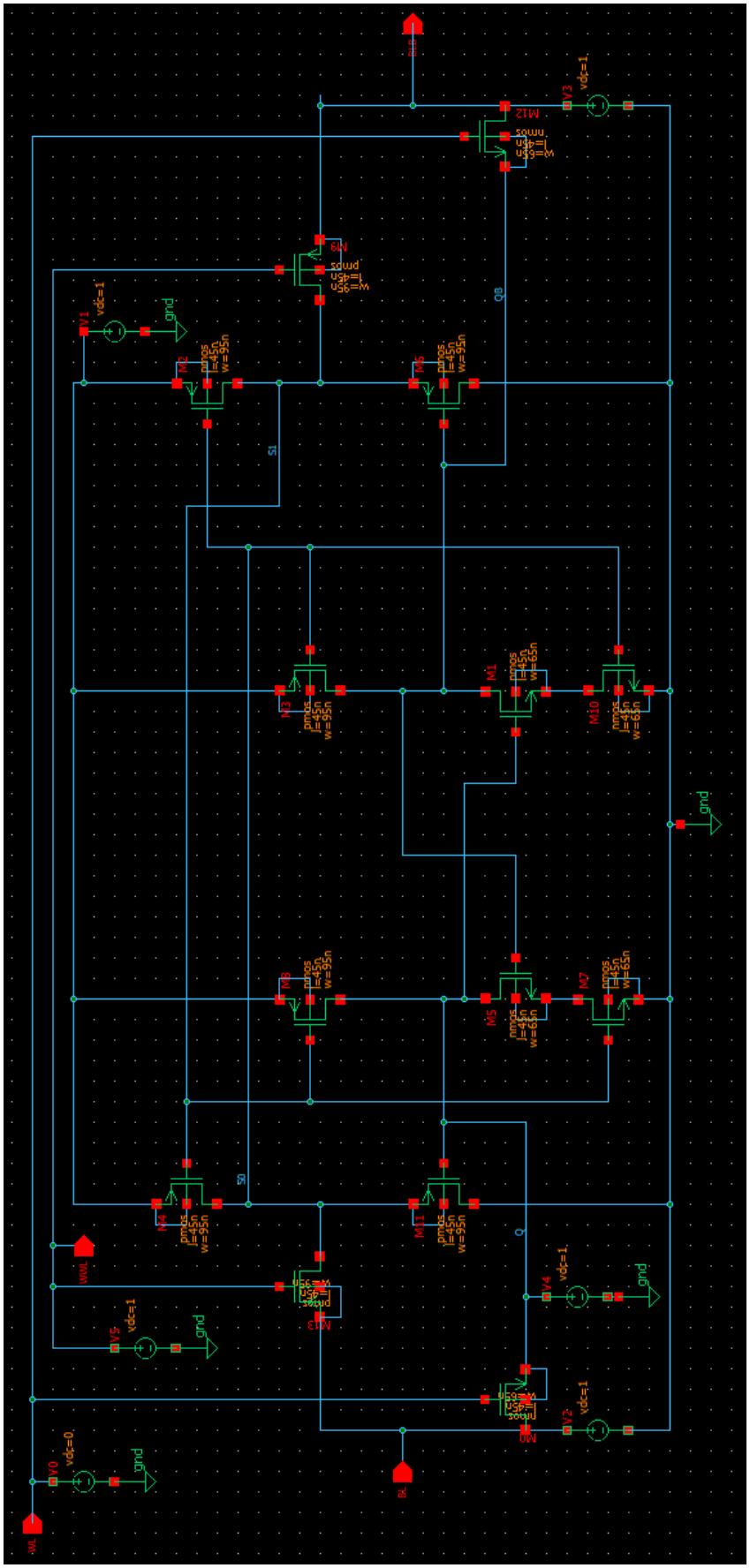

Figure 4. Reff 01. NRHC 14-T.

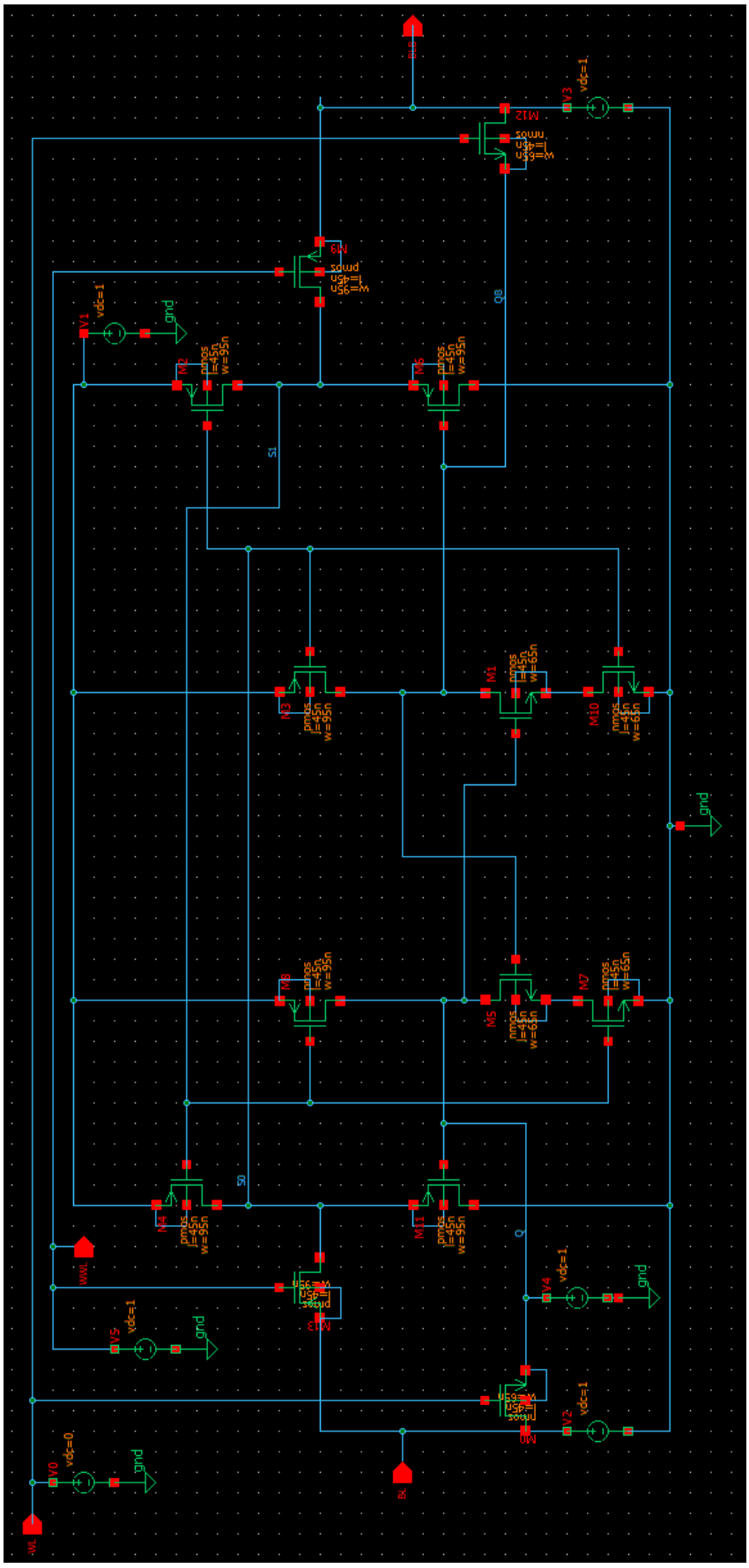

Figure 5. Reff 02. RHRD T2 12-T.

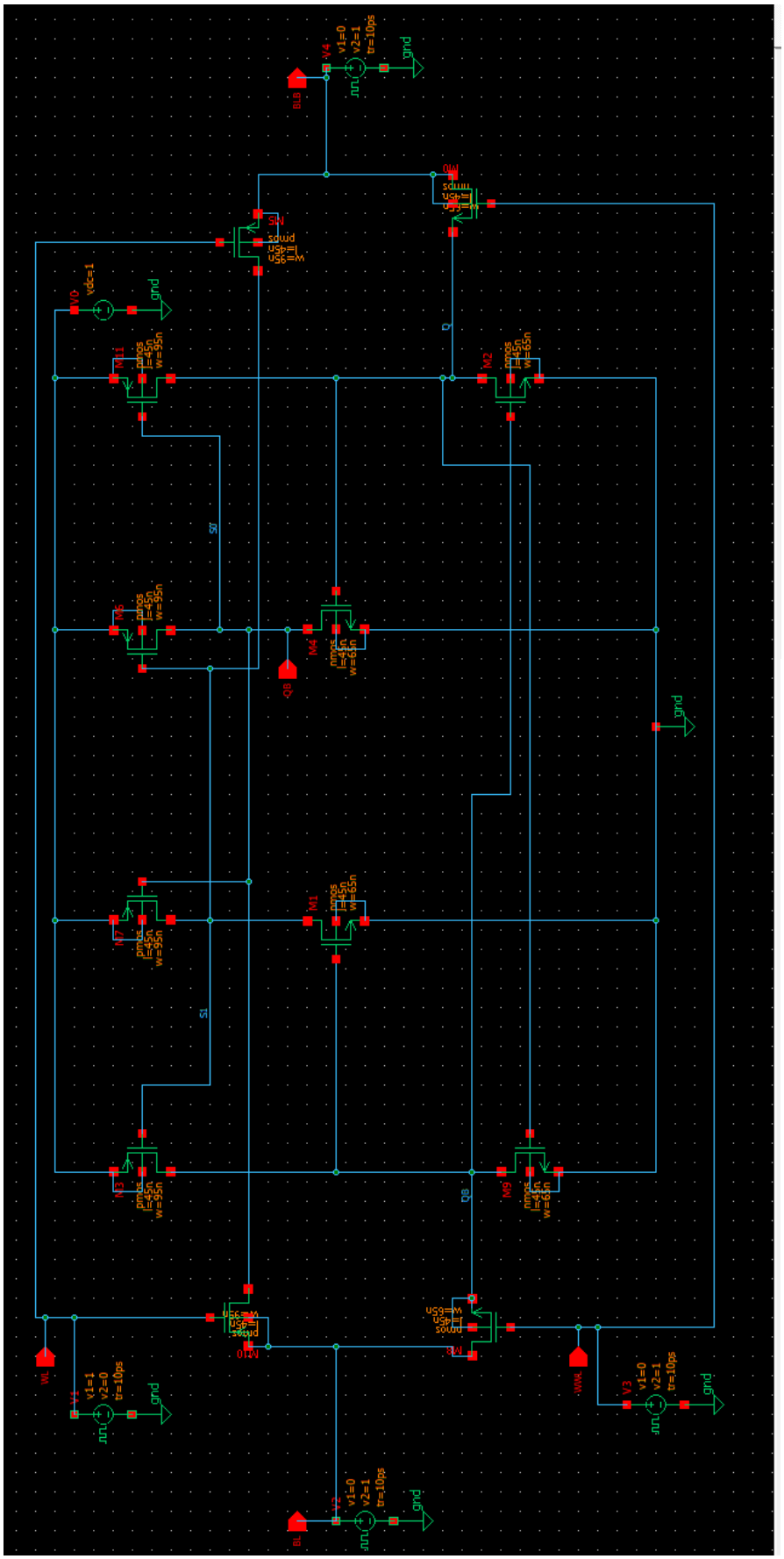

Figure 6. Reff 03. SEUH 12-T.

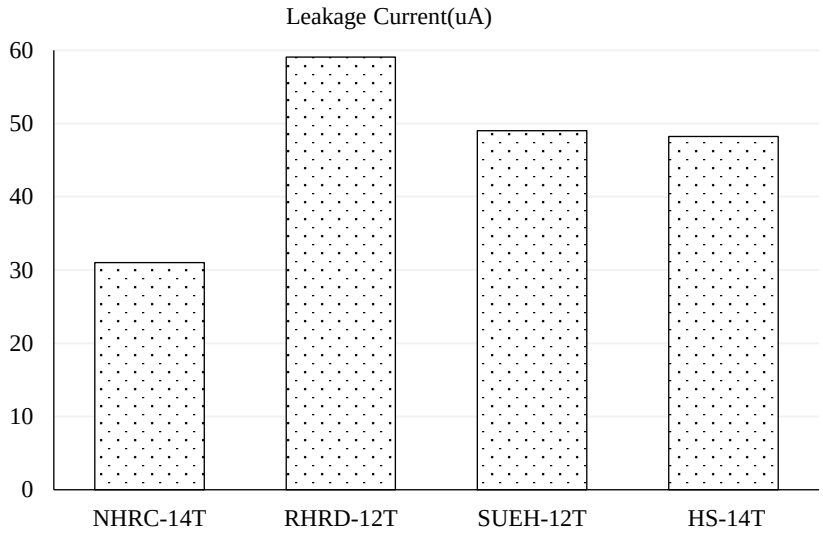

Figure 7. Leakage current comparison of SRAM.

Table 2. Comparison of proposed 14 T SRAM cell with Previous 12T SRAM cell.

Parameters	I4 T Proposed SRAM cell	REFF 01. NRHC 14T	REFF 02 RHRD T2 12T.	REFF 03 SEUH 12T
Read Delay (ps)	1	5	9	9
Write Delay (ps)	5	14.8	16	4
LC (μA)	46.24	31	59	49.4

CONCLUSION

The proposed HS-14T SRAM cell demonstrates significant advancements in high-speed aerospace applications, primarily through the optimization of delay and leakage current. Leveraging CMOS technology, the HS-14T SRAM cell achieves remarkably low power consumption and reduced read and write times, which are critical for enhancing overall system performance. Through the use of Symica software and 45 nm technology, the HS-14T design achieves a read delay of 1 ps and a write delay of 5 ps, outperforming other contemporary SRAM cells. This significant reduction in delay times translates to faster memory operations, making the HS-14T a superior choice for applications requiring rapid data access and storage. A comparative analysis reveals that the HS-14T SRAM achieves substantial improvements in read delay. It demonstrates an 80% reduction compared to the NHRC-14T SRAM, an 88% reduction compared to the RHRD-12T SRAM, and an 89% reduction compared to the SEUH-14 SRAM. These reductions underscore the HS-14T's exceptional speed in data retrieval, which is vital for high-performance computing systems. In terms of write delay, the HS-14T SRAM also showcases significant enhancements. It exhibits a 66% reduction compared to the NRHC-14T SRAM, a remarkable 98.75% reduction compared to the RHRD-12T SRAM, and a 25% reduction compared to the SEUH-14 SRAM. These improvements in write speed further solidify the HS-14T's capability to handle fast data storage and processing efficiently. While the HS-14T SRAM shows a 55% increase in leakage current compared to the NRHC-14T SRAM, it still offers notable reductions of 18 and 1.63% compared to the RHRD-12T and SUEH-12T SRAMs, respectively. These improvements highlight the HS-14T's energy-saving capabilities and its potential to enhance power efficiency, crucial for prolonging battery life in portable devices. In summary, the HS-14T SRAM cell presents a significant leap forward in memory technology, offering superior performance in read and write delays while maintaining competitive leakage current characteristics. These advancements position the HS-14T as a compelling option for future semiconductor designs, particularly in high-speed aerospace applications where rapid data access and efficient power consumption are paramount. The comparative evaluations underscore the HS-14T's potential impact on enhancing productivity and performance in various computing systems, paving the way for its adoption in cutting-edge technological applications.

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