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Fabrication, Numerical Simulation and Compact Modeling of Ph-BTBT-C10 Organic Thin Film Transistor

Shubham Dadhich[1,*], Vivek Upadhyay[2], Garima Mathur[3]

Abstract

Flexible and cost-effective electronics have been necessitated by the advent of organic thin-film transistors (OTFTs). This study aims to study the performance of OTFT using a 2-decyl-7-phenyl-[1]benzothieno[3,2-b][1]benzothiophene (Ph-BTBT-C10) organic semiconductor. The paper also explore accurate device modeling for technology optimization and circuit design that supports device improvement. This research includes device fabrication, numerical simulation using TCAD, compact modeling, and parameter extraction. By combining temperature-dependent bandgap narrowing with existing theories, this model can more accurately predict changes in the bandgap with respect to temperature which is critical in designing advanced semiconductor devices. The electrical behaviour of the device can be accurately simulated by refining the other equations related to semiconductors. The experimental data were compared with the results from ATLAS simulations and compact modelling. In addition, the study consists of simulating a P-type TFT-based inverter to evaluate its performance as applied to basic circuit applications using the compact model.

Keywords: Ph-BTBT-C10, Device Modeling, Compact Modeling, SMART SPICE, Device Physics, Density of States

INTRODUCTION

Organic electronics represents an emerging but fast-growing sector of technology. Replacing typical inorganic materials with organic alternatives involves considerable challenges. Despite these difficulties, organic materials are promising for applications such as photovoltaic light diodes and large-area electronics [1, 2]. However, obtaining efficient, competitive, and low-cost production still involves a substantial study of theoretical knowledge, material characteristics, and process approaches [3, 4]. This industry is anticipated to expand into a global market worth numerous millions of Euros, driven by the competitive areas of generating marketable goods [5–7]

The solution processability of organic semiconductors enables the production of a variety of lightweight, low-cost, flexible, foldable, and disposable devices, such as LEDs [5], AMOLED displays [8–9], bio-sensors [8], solar cells [10–12], and OTFT [1, 2]. The inclusion of organic materials in optoelectronics has transformed this discipline by providing efficient and flexible systems for light emission, detection, and modulation, thereby offering new opportunities for new optical technologies [11].

Rapid breakthroughs in neuromorphic devices are paving the way for the hardware implementation of neuromorphic computing systems, which promise exceptional possibilities for future artificial intelligence applications with improved efficiency, scalability, and cognitive

***Author for Correspondence**
Shubham Dadhich

[1]Research Scholar, Department of Electrical and Electronics Engineering, Poornima University Jaipur, Vidhani, India
[2]Assistant Professor, Department of Electrical and Electronics Engineering, Poornima University Jaipur, Vidhani, India
[3]Professor, Department of Electrical and Electronics Engineering, Poornima University Jaipur, Vidhani, India

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computing capabilities [12]. OTFTs are crucial components of organic electronics, and cooperation between academia and industry is required to address the rising demand for these devices [13]. The available Electronic Design Automation (EDA) technology is compatible with the current silicon devices, making a small model important for producing Organic Semiconductor (OSC) devices. This model acts as a bridge between semiconductor device physics and circuit design.

Understanding device physics is crucial for defining every semiconductor. Investigating the basic physical properties of molecules and charge transport pathways can aid in enhancing the OSC device performance, with these factors being highly reliant on the individual features of the semiconductor material. Unlike the well-established silicon industry, organic transistors lack a complete device model. The charge carrier movement in OTFTs differs significantly from that in crystalline silicon transistors, rendering conventional MOSFET models inappropriate for various disordered OSCs. Therefore, device modeling has to account the Density of States (DOS) and charge transport processes.

Previous models developed from silicon models were unable to adequately represent OSC properties because they depended largely on the fitting parameters. One such model estimates the drain current using other factors and incorporates a correction coefficient, making it highly reliant on the device and its structure rather than on fundamental device physics. For instance, a model based on drift-diffusion and the Poisson equation was used to predict the behaviour of pentacene TFTs but could not properly define OSCs based on their physical properties [14]. Another study focused on calculating trapped and mobile charges separately to construct a total charge density equation; however, the features did not match on a logarithmic scale, notably considering the leakage current [15].

Further studies updated the current-voltage equation with a channel length modifier parameter, but it remained dependent on MOSFET types and was tested on a single OSC (PTAA) [16]. Studies on the contact effects and current-voltage characteristics of pentacene with polyvinyl phenol have also aimed to solve the drain current using current density equations [17]. Another study focused on a self-consistent coupling method for biosensor OTFTs, concentrating primarily on P3HT OSC [18]. Efforts to simulate pentacene TFTs using space-charge-constrained current models require updating the Poisson equation with new formulae and applying the Monte Carlo technique to construct current-voltage relations. These models account for contact resistance and capacitance interactions with hopping transport, successfully simulating pentacene OTFTs [19, 20].

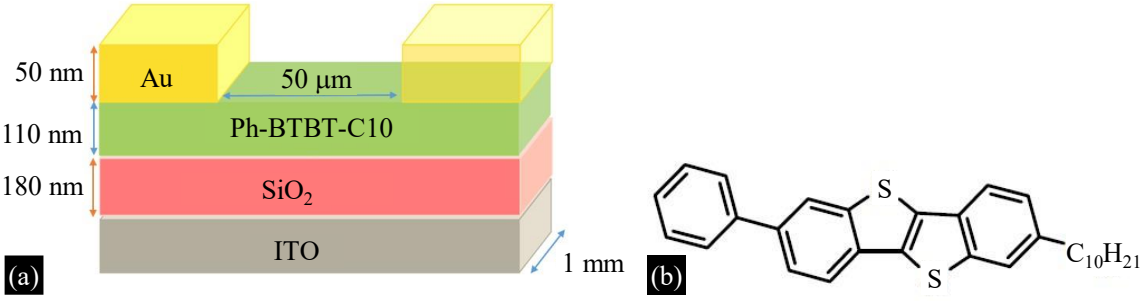
Effective models should display congruent behaviour, structural symmetry, adequate input physical parameter variables, simplicity of conversion, tunability for diverse experimental data, and flexibility for upgrades. To the best of our knowledge, no Technology Computer-Aided Design (TCAD) model has been developed for 2-decyl-7-phenyl-[1]benzothieno[3,2-b][1]benzothiophene (Ph-BTBT-C10) semiconductors that contains semiconductor physical parameters to anticipate TFT characteristics. The universal approach for OTFTs does not accommodate freshly synthesised OSCs. This article intends to establish a TCAD model to facilitate the understanding and improvement of organic electronics, easing the TCAD to SPICE model flow in a Design Technology Co-Optimization (DTCO) environment for logical circuit construction [25].

FABRICATION OF DEVICE

The fabrication of a bottom-gate, top-contact OTFT was attempted. The dimensions are shown in Figure 1(a) and the chemical formula of Ph-BTBT-C8 is shown in Figure 1 (b). This involved a detailed procedure in which silicon wafers with high dopant concentrations were developed for silicon dioxide (SiO_2) deposition. The first step is the cleaning process; to remove the surface of any contaminants that could affect the deposition quality, some steps are standardised. This was followed by exhaustive rinsing with deionised water to ensure a clean surface for deposition. Additionally, the surface was acid-treated moderately to optimise the surface for SiO_2 deposition. It also removes any remaining native oxide layers.

The substrate was prepared to low temperature chemical vapor deposition (CVD) in order to SiO_2 coating. During this stage, oxygen and silicon atoms are introduced into the chamber as gases. To support the cracking and deposition processes, the silicon substrate was heated from 100 °C to 150 °C. The inception point of the precursor molecules is on the substrate; hence, they start reactions that release oxygen and silicon atoms. Subsequently, these atoms were dispersed across the surface of the substrate where they formed a continuous and same SiO_2 layer. Adjusting either the deposition duration or precursor flow rate regulated the thickness of the deposited SiO_2.

The sample was treated with UV/ozone for 10 min before the final printing layer. The Si wafer was dipped in a mixture of 3% pentafluorothiophenol and ethanol for 10 min. After rinsing extensively, N_2 gas dried the sample. Ph-BTBT-C10 ink was printed using 0.5 mL droplets on the dielectric surface. The coated surface was then cured at 70°C on a hot plate for 20 min. For example, the OSC ink contained only Ph-BTBT-C10 (2 wt %), which was prepared in anisole with additives to improve printability.



2-Decyl-7-phenyl[1]benzothieno[3,2-b][1]benzothiophene

Figure 1. (a) Structure of Ph-BTBT-C10 OTFT, (b) Molecular Structural of Ph-BTBT-C10.

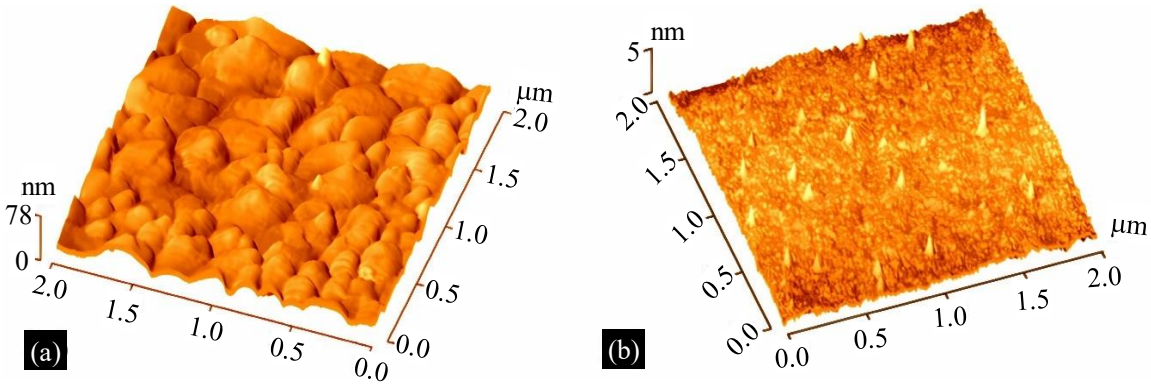


Figure 2. (a) AFM images of Ph-BTBT-C10 layer (b) AFM images of gold as S/D (Measured range is 2 µm× 2 µm).

To make source/drain electrodes (S/D) from gold on top of Ph-BTBT-C10 layer, low temperature deposition method had to be used. This ensured excellent formation of the electrode but minimised the heat stress within the organic semiconductor and substrate material. Sputtering has led to the development of S/D electrodes with thicknesses of approximately 50 nm. A deposition temperature between room temperature and approximately 100°C was used for this method. A stencil measuring 50 µm was used to determine the channel composition.

Figure 2 illustrates the surface morphology and structure from atomic force microscopy (AFM). These high-resolution images show the topography of the OSC layer, while also portraying features such as crystalline structures, grain boundaries, and roughness.

Subsequently, a NanoScan white light interferometer was used to determine the average thickness and roughness. Contact angle measurements were performed using a SEO Phoenix 200 Touch contact angle analyser, and the electrical behaviour was analysed using a Keithley 4100 SCS parameter analyser. Currents between source-drain(I_{DS}) were measured at gate to source voltages(V_{GS}), ranging from -10V to -60V and drain to source voltages (V_{DG}), ranging from -10V to -60V. The output characteristics were observed and compared with the simulation results in following section (Figure 3).

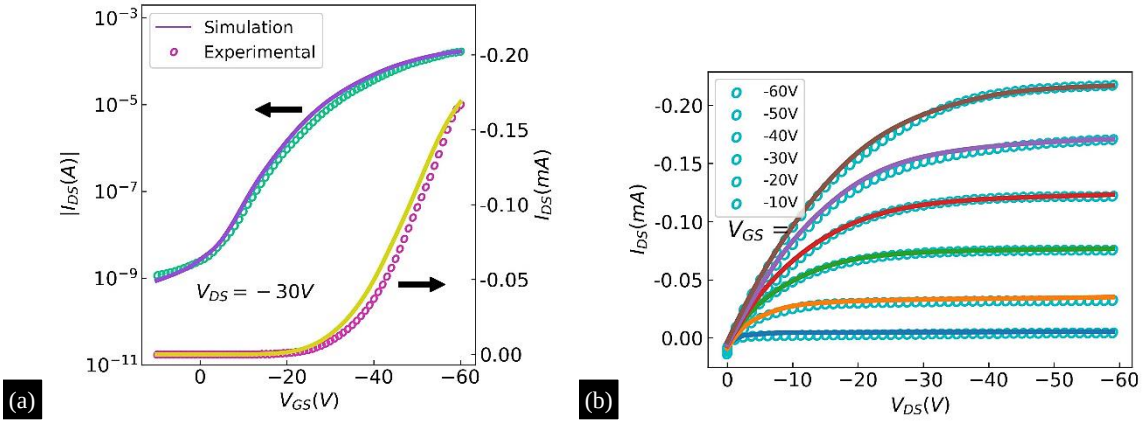


Figure 3. Simulated and Experimented Data of Ph-BTBT-C10 OTFT (a) (I_{DS} *vs* V_{GS}). (b) (I_{DS} *vs* V_{DS}).

TCAD Modeling

The SILVACO ATLAS software was used to define the semiconductor material parameters. These parameters were calculated by applying Maxwell's equations to the 2D/3D mesh points and solving the Poisson equation for the boundary conditions of the charge. Consequently, both the AC and DC transient models of any device can be developed using ATLAS [21].

Semiconductor Fundamental Modeling

Many materials, including crystals, stretched polymers, and liquid crystals, exhibit directional dependence [22] in their macroscopic properties such as strength, optical quality, and electrical properties, making them anisotropic. The electrical conductivity of a material can also varies depending on the direction, leading to anisotropy. Some carbon materials have three dimensions, whereas others are one-and two dimensional. For instance, diamonds, graphite, and polyacetylene exemplify three-dimensional, two-dimensional, and one-dimensional carbon structures [23].

To study the conductivity of one- or two-dimensional chains, we must observe that the conjugated backbone of these polymers contains alternating double and single bonds which cause distinctive electronic structures. The electron levels are arranged in the solid state, and there is a forbidden energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) [24]. (Figure 4) The valence band in silicon can be compared to the HOMO, whereas the LUMO can be likened to the conduction band. The energy gap (E_G) depends on the repeating unit of chemical structure, with E_G normally decreasing as chain length increases. Consequently, conjugated polymers exhibit semiconducting characteristics because they possess a band-like electronic structure with limited electronic mobility. The band gap depends upon temperature as well [25]. To model the band gap, a mathematical description is essential. The experimental bandgap of a material can be defined as E_{G300}, representing at 300K, and the effect of temperature can be adjusted from the variables below in the equation. The values that fit the experimental data during the last iteration of the simulation are given in Table 1 [26].

$$E_g(T_L) = E_{G300} + E_{G_\alpha}\left[\frac{300^2}{300+E_{G_\beta}} - \frac{T_L^2}{T_L+E_{G_\beta}}\right] \quad (1)$$

Table 1. Band Gap Parameters for Ph-BTBT-C10.

Parameter	Value	Units
E_{g300}	2.0 eV [26]	eV
E_{G_α}	6.25×10^{-4}	eV/K
E_{G_β}	236	K
E_{CB}	-3.21[26]	eV
E_{VB}	-5.21 [26]	eV
E_G	2.0 eV [26]	eV

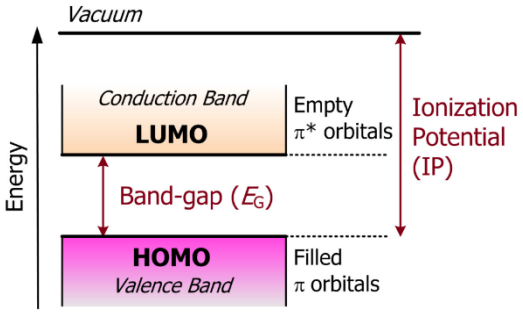


Figure 4. Representative Energy Band Diagram of an OSC.

DOS of Mobile Charge Carrier

The DOS of the mobile charge carriers in a semiconductor has a substantial impact on the concentrations of both electrons and holes [27]. In this context, the DOS refers to the number of energy states that exist within a given range of energy levels. A high DOS implies that there are sufficient unoccupied regions which affect the movement of charge carrier, and ultimately, the channel electricity. The concentration of electrons and holes that determines charge neutrality depends on factors such as the doping concentration and temperature. Combining Fermi-Dirac statistics with parabolic DOS in conduction and valence bands where E_C and E_V are respectively locations for their minimum energies [28].

Fermi-Dirac integral [29] is a mathematical function that gives an estimate of the possibility of an electron occupying a state with energy (E). The temperature dependence of the electron and hole concentrations was determined using the Fermi-Dirac integral. As temperature increases, the occupancy probability for states at the Fermi level rises, resulting to larger electron and hole concentrations. Using these formulae, we can determine the carrier concentration within a semiconductor material, which is an important parameter in defining the electrical characteristics of a material.

$NC \cdot F$	
$NV \cdot F$	
	$5.0 \times 10^{-2}\ cm^2/(V \cdot s)$
	$4.4 \times 10^{-1}\ cm^2/(V \cdot s)$
	1×10^{16}

$$N_C(T_L) = 2\left(\frac{2\pi m_e^* kT_L}{h^2}\right)^{\frac{3}{2}} = \left(\frac{T_L}{300}\right)^{NC\cdot F} NC300 \quad (2)$$

$$N_V(T_L) = 2\left(\frac{2\pi m_h^* kT_L}{h^2}\right)^{\frac{3}{2}} = \left(\frac{T_L}{300}\right)^{NV\cdot F} NV300 \quad (3)$$

$$n = N_C \exp\left(\frac{E_F - E_{CB}}{kT_L}\right) \quad (4)$$

$$p = N_V \exp\left(\frac{E_{VB} - E_F}{kT_L}\right) \quad (5)$$

In these formulations, n and p indicate the electron and hole concentrations, whereas N_C and N_V signify the DOS in the conduction and valence bands [30]. The function ($f_F(E)$) indicates the likelihood of an electron being in the conduction band and the probability of a hole being in the valence band. Conversely, the probability of an electron being in the valence band and a hole being in the conduction band is $(1 - f_F(E))$, as depicted in Figure 5. The symbol m^* symbolises the effective mass of the hole or electron, k represents Boltzmann's constant, T_L is the temperature variable in the model, and E_F is the Fermi level. The parameter values were acquired from literature and tweaked through simulated runs. Table 2. lists these parameter values.

Table 2. Mobile Charge Carrier DOS Parameter Values.

Parameters	**Values**
Effective DOS in the valence band (N_v 300)	1.1×10^{21} cm^{-3} [162]
Effective DOS in the conduction band (N_C 300)	1.2×10^{21} cm^{-3} [162]
$NC \cdot F$	1.43
$NV \cdot F$	1.58
Mobility of electron μ_n	5.0×10^{-2} $cm^2/(V \cdot s)$ [163]
Mobility of hole μ_p	4.4×10^{-1} $cm^2/(V \cdot s)$ [163]
Acceptor concentration	1×10^{16} [158]

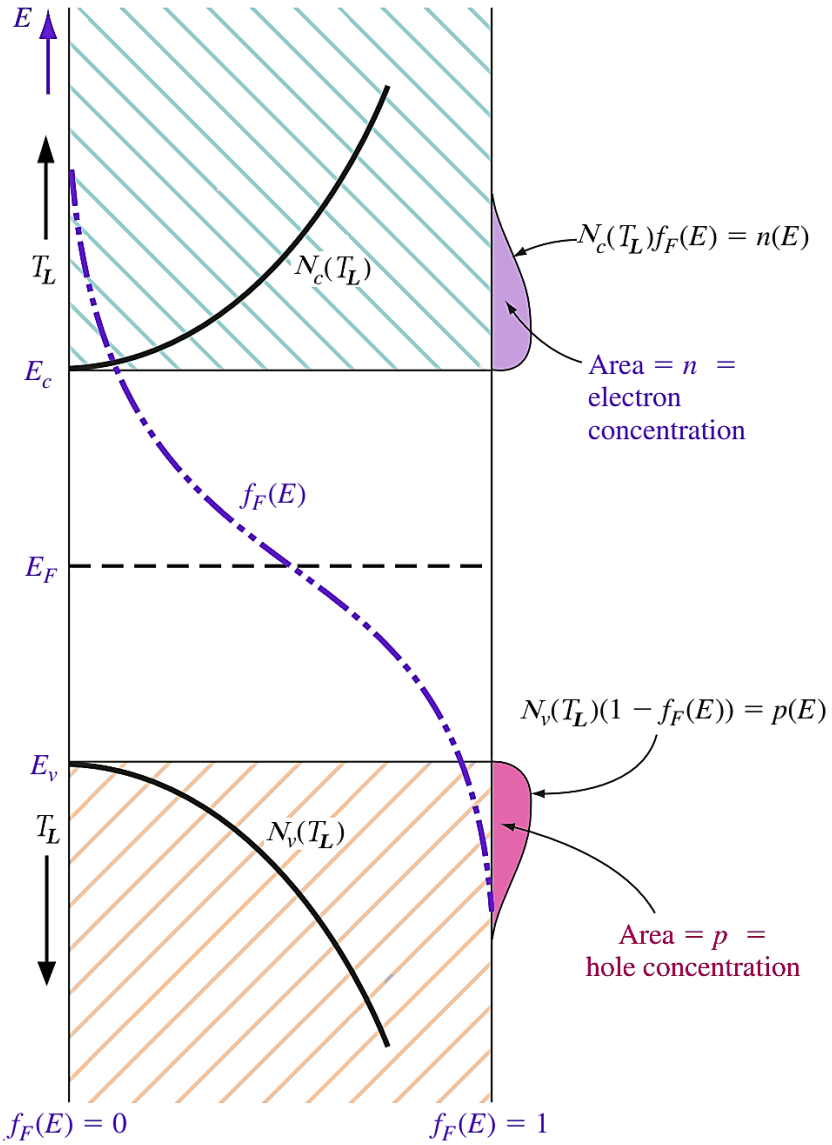


Figure 5. Density of States Functions, Fermi-Dirac Probability Function, and Areas Representing Electron and Hole Concentrations.

DOS of Acceptor and Donor

Disordered conductive semiconductors are defined by localised states and extended energy levels inside a forbidden energy gap. Charge transfer in these materials occurs via thermal activation, tunnelling, hopping, or a combination of these modes. In hopping transport, the energy necessary to overcome the potential barrier is provided by thermal vibrations [19]. The hopping effectiveness depends on the height of the potential barrier to the next site and the existence of thermal vibrations (temperature).

Both kinds of charges could move in a semiconducting film on the basis of theory. However, in most semiconductors, only one type of charge carrier is usually mobile. So contacts inject only this mobile charge and can be trapped. Owing to the broad energy bandgap, the thermal charge generation becomes very weak [31]. Thus, it is often presumed that every molecule donates a single charge carrier. The total density of states (DOS) typically equals to molecular concentration usually about 10^{20} to 10^{21} cm^3. The DOS has been described for two charge carriers: the first mobile charge carrier (hold and electron), and the second static charge carrier (acceptor and donor). The DOS is assumed to consist of four bands: two tail bands (representing a donor-like valence band and an acceptor-like conduction band), and two

deep-level bands (one being acceptor-like and the other donor-like). The deep-level bands are modelled using Gaussian distributions.

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad (6)$$

$$g_{TA}(E) = N_{TA} \exp\left[\frac{E-E_c}{W_{TA}}\right] \quad (7)$$

$$g_{TD}(E) = N_{TD} \exp\left[\frac{E_v-E}{W_{TD}}\right] \quad (8)$$

$$g_{GA}(E) = N_{GA} \exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^2\right] \quad (9)$$

$$g_{GD}(E) = N_{GD} \exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \quad (10)$$

In tunnelling, the transition probability is controlled by the form of the potential barrier, particularly its width and height. A combination of tunnelling and hopping, typically referred to as thermally or phonon-assisted tunnelling, is also frequent. Potential barriers can be uniform or non-uniform, with non-uniform barriers further divided into exponential and Gaussian forms.

In terms of the DOS description [32, 33], two different distributions were considered: an exponential tail distribution and a Gaussian distribution. The intercept densities at conduction and valence band (N_{TA} and N_{TD}) as well as the decay energies (W_{TA} and W_{TD}) represent DOS of exponential tail distribution. On the other hand, DOS for Gaussian distribution is denoted by peak energy distributions (E_{GA} and E_{GD}), total DOS (N_{GA} and N_{GD}) and characteristic decay energies (W_{GA} and W_{GD}). These distributions can be represented mathematically in terms of the equations (7) to (10)

The total ionised DOS can be estimated using eq.(11) and (12) with the help of (13)–(16). In physical representation, all these denote associated impurities or dopant atoms that have been ionised. Impurities or molecule are introduced into semiconductors to modify their electrical properties. They can either be donors or acceptors based on their influence on the conductivity of the semiconductor. Whenever a dopant atom is added to the lattice of a semiconductor, it may donate an electron to the conduction band or accept an electron from the valence band. In this process, ionising dopants are formed. The p_T stands for the ionised density of the acceptor-like states and n_T stands for donors. Usually, the p_T values and n_T values are mutually constrained such that if p_T is high, then $n_T$is low and vice versa [34]. This is simply because a OSC has fewer free charge carriers compared to other materials; hence, one type of ionised dopant tends to suppress the presence of another type of ionised dopant because they occupy almost similar spaces in a crystal silicon lattice. In general, these densities increase as the temperature increases, while decreasing depending on the direction of the electric field.

The ionised density affects the overall conduction of semiconductor devices [35]. Electrical engineers who manufacture semiconductors can change their material resistivity by altering its concentration and distribution, with special attention being paid to conductivity, among other factors.

$$p_T = p_{TA} + p_{GA} \quad (11)$$

$$n_T = n_{TD} + n_{GD} \quad (12)$$

where p_{TA}, p_{GA}, n_{TD} and $n_{GD}$are given below

$$p_{TA} = \int_{E_V}^{E_C} g_{TA}(E) \cdot f_{t_{TA}}(E,n,p)dE \quad (13)$$

$$p_{GA} = \int_{E_V}^{E_C} g_{GA}(E) \cdot f_{t_{GA}}(E,n,p)dE \quad (14)$$

$$n_{TD} = \int_{E_V}^{E_C} g_{TD}(E) \cdot f_{t_{TD}}(E, n, p) dE \quad (15)$$

$$n_{GD} = \int_{E_V}^{E_C} g_{GD}(E) \cdot f_{t_{GD}}(E, n, p) dE \quad (16)$$

$f_{t_{TA}}(E, n, p)$ and $f_{t_{GA}}(E, n, p)$ are the ionisation probabilities for the tail and Gaussian acceptor DOS, while $f_{t_{TD}}(E, n, p)$ and $f_{t_{GD}}(E, n, p)$ are the ionisation probabilities for the donors.

In a steady state, the probability of occupancy is given by the following equations:

$$f_{t_{TA}}(E, n, p) = \frac{v_n \sigma_{TAE}\, n + v_p \sigma_{TAH}\, n_i \exp\left[\frac{E_i - E}{kT}\right]}{v_n \sigma_{TAE}\left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \sigma_{TAH}\left(p + n_i \exp\left[\frac{E_i - E'}{kT}\right]\right)} \quad (17)$$

$$f_{t_{GA}}(E, n, p) = \frac{v_n\, \sigma_{GAE}\, n + v_p\, \sigma_{GAH}\, n_i \exp\left[\frac{E_i - E}{kT}\right]}{v_n\, \sigma_{GAE}\left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \sigma_{GAH}\left(p + n_i \exp\left[\frac{E_i - E_0}{kT}\right]\right)} \quad (18)$$

$$f_{t_{TD}}(E, n, p) = \frac{v_p \sigma_{TDH}\, p + v_n \sigma_{TAE}\, n_i \exp\left[\frac{E - E_\zeta}{kT}\right]}{v_n \sigma_{TAE}\left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \sigma_{TDH}\left(p + n_i \exp\left[\frac{E_i - E'}{kT}\right]\right)} \quad (19)$$

$$f_{t_{GD}}(E, n, p) = \frac{v_p \sigma_{GDH}\, p + v_n \sigma_{GDE}\, n_i \exp\left[\frac{E - E_i}{kT}\right]}{v_n \sigma_{GDE}\left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \sigma_{GDH}\left(p + n_i \exp\left[\frac{E_i - E^-}{kT}\right]\right)} \quad (20)$$

$$v_t \text{ (Thermal Velocity)} = \sqrt{\frac{3kT}{m}} \quad (21)$$

In semiconductor physics uses electron thermal velocity ('v_n') [36], it is important component to capture the attribute and movement of electrons in materials. The kinetic energy of free electrons increased with the increase in temperature leading to higher thermal velocities. Electron transport properties such as drift and diffusion, which are essential for semiconductor devices, also rely on the electron thermal velocity. In a similar way, the hole thermal velocity ('v_p') is a measure of how fast holes in semiconductors move around due to heat. Like electrons, holes have also thermal energy that stimulate them to move. Thus both` are essential aspects when considering overall charge transport characteristics for semiconductors. Intrinsic carrier concentration 'n_i' is one of the basic properties of any semiconductor materials. It is a quantity that the number density or concentration at which intrinsic charge carriers exist before being doped with any impurity atoms. Under conditions of thermodynamic equilibrium, a balance between generation rate and recombination rate [37] happens. As a result, there is steady-state carrier concentration at thermal equilibrium.

Here, we would discuss the electron capture cross-sections [38], σ_{TAE} and σ_{GAE} which represent the probabilities of electrons getting captured by acceptor like states in semiconductors. When less valence electrons are introduced by impurity atoms with respect to those in the host material, acceptor states traps come into existence. These quantum mechanical descriptions give us a picture of how many carrier dynamics will be affected and recombination processes can occur when an electron is trapped within these impurities. Different energy configurations for the acceptors as well as their corresponding capture cross sections can be provided through the analysis of such quantities as the acceptor tail and Gaussian states.

Similarly, the hole capture cross-sections, σ_{TAH} and σ_{GAH}, The same way, hole capture cross sections are σ_{TAH} and σ_{GAH}. This discloses how likely a hole is captured by an acceptor like state. These capture cross sections provide insight on the mechanisms of recombination and trapping of holes. In the case of donor states, we use symbols as σ_{TDH} , σ_{TDE}, σ_{GDE}, σ_{GDH} . All these parameters values were given under Table 3. So when talking about donor states , their capture cross-sections refer to both electron and hole being enclosed by these donor-like levels. Besides it is notable for charge carriers interacting with those

donor states since they influence carrier life times, recombination rates and other semiconductor device features.

Table 3.: Parameters Values of Acceptor and Donor DOS

Parameters	Values	Unit	Parameters	Values	Unit
	1.2				
	0.6	**eV**			
	0.7	**eV**			
	0.32	**eV**			
	0.61	**eV**			
	0.14	**eV**		**0.15**	**eV**

By studying and manipulating these properties, semiconductor engineers can optimise the device characteristics, enhance the efficiency, and develop advanced electronic technologies. In the context of steady-state conditions in a semiconductor material, the net recombination and generation rates for electrons (R_n) and holes (R_p) are equal, resulting in what is known as instantaneous equilibrium [39]. This implies that the rate at which electrons recombine and holes are generated is balanced, maintaining a steady carrier concentration within the material. This equilibrium is crucial for maintaining the stable electrical properties of semiconductor devices.

$$
\begin{aligned}
R_{n,p} = \int_{E_V}^{E_C} \Bigg(& \frac{v_n v_p \, \sigma_{TAE} \, \sigma_{TAH} (np - n_i^2) g_{TA}(E)}{v_n \left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) \times \sigma_{TAE} + v_p \, \sigma_{TAH} \left(p + n_i \exp\left[\frac{E_i - E}{kT}\right]\right)} \\
& + \frac{v_n v_p \, \sigma_{TGAE} \, \sigma_{GAH} \, (np - n_i^2) g_{GA}(E)}{v_n \sigma_{GAE} \left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \, \sigma_{GAH} \left(p + n_i \exp\left[\frac{E_i - E}{kT}\right]\right)} \\
& + \frac{v_n v_p \, \sigma_{TGAE} \, \sigma_{GAH} \, (np - n_i^2) g_{GA}(E)}{v_n \sigma_{GAE} \left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \, \sigma_{GAH} \left(p + n_i \exp\left[\frac{E_i - E}{kT}\right]\right)} \\
& + \frac{v_n v_p \, \sigma_{TDE} \, \sigma_{TDH} \, (np - n_i^2) g_{TD}(E)}{v_n \sigma_{TDE} \left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \sigma_{TDH} \left(p + n_i \exp\left[\frac{E_i - E_T}{kT}\right)\right.} \\
& + \frac{v_n v_p \sigma_{GDE} \, \sigma_{GDH} \, (np - n_i^2) g_{GD}(E)}{v_n \sigma_{GDE} \left(n + n_i \exp\left[\frac{E - E_i}{kT}\right]\right) + v_p \sigma_{GDH} \left(p + n_i \exp\left[\frac{E_i - E}{kT}\right]\right)} \Bigg) dE
\end{aligned}
\tag{22}
$$

Charge Transportation

In disordered semiconductors, charge transportation occurs via many methods. Unlike crystalline semiconductors, where charge carriers flow along well-defined energy bands, disordered semiconductors contain disrupted energy bands, resulting in localised energy states. These localised states, also known as trap or leaping sites, are dispersed throughout the material. Charges travel from the source to the drain through these trap sites in a process known as hopping charge transfer.

The two primary hopping transport behaviours are thermal activation and quantum tunnelling. In thermal activation, charge carriers acquire sufficient energy from an electric field or heat to surmount the energy barrier between hopping sites. However, for the wave-like nature of conducting charges, in quantum tunnelling, they can pass through energy barriers without sufficient energy required by their wave-like character [40].

Hopping conduction normally becomes more important at higher temperatures or larger trap site densities, and affects the electrical properties of TFTs. Although it restricts carrier mobility and decreases device performance relative to crystalline semiconductors, hopping charge transport improves the characteristics of disordered semiconductors, as well as finding new materials for better performance.

$$\mu_{n_{hop}} = \frac{qV_{0nhop}}{kT_L}\left[\int_{-\infty}^{E_{trn}} g_a(E)dE\right]^{-\frac{2}{3}} \exp\left[-2\left(\frac{3\beta_{n\_hop}}{4\pi}\right)^{1/3} \gamma_{n\_hop}\left[\int_{-\infty}^{E_{trn}} g_a(E)dE\right]^{-1/3}\right] \quad (23)$$

$$\mu_{p_{hop}} = \frac{qV_{0phop}}{kT_L}\left[\int_{-\infty}^{E_{trn}} g_d(E)dE\right]^{-\frac{2}{3}} \exp\left[-2\left(\frac{3\beta_{p\_hop}}{4\pi}\right)^{1/3} \gamma_{p\_hop}\left[\int_{-\infty}^{E_{trn}} g_d(E)dE\right]^{-1/3}\right] \quad (24)$$

The hopping model was presented in [40]. In this model, the effective mobility of electrons and holes is given as $\mu_{n_{hop}}$ and $\mu_{p_{hop}}$, respectively. Eq. (23) pertains to electrons, where $V_{0_{nhop}}$ indicates the frequency of the electron tries to jump within the conduction band, and $g_a(E)$ reflects the DOS for the acceptor-like conduction band. The values $\beta_{n_{hop}}$ and $\gamma_{n_{hop}}$ denote the percolation constant and the reciprocal of the carrier localisation radius, respectively. The carrier is expected to move from its present occupied state to a hopping site positioned within the effective transport level of energy E_{tr}.

Similarly, in the comparable equation for holes, 'p' is used to signify holes, and the parameters are identical to those described above for holes using the hopping mobility model. These formulae describe the behaviour of charge carriers in disordered or amorphous materials by hopping among localised states.

SIMULATION OF MODEL AND RESULT DISCUSSION

The simulation was initiated by defining the structure shown in Figure 1 and defining the mesh accordingly. Because the semiconductor-dielectric interface and near source/drain electrodes are regions where significant potential and charge density variations exist, this mesh becomes denser in these parts. The next step involves defining the material properties using SOPRA files. A position-dependent function is used to define its bandgap, thus enabling matching well with the varied OTFT across different regions.

Table 4. Simulated vs. Experimented Performance Parameters Compassion.

Parameter	Experimented	Simulated	Unit
μ_{lin} (V_{GS} =-1.0 V)	1.3×10^{-5}	1.6×10^{-5}	$cm^2/(V \cdot s)$
G_m (V_{GS} =-1.0 V)	4.60×10^{-6}	5.4×10^{-6}	Siemens
μ_{sat} (V_{GS} =-40.0 V)	2.9×10^{-2}	3.0×10^{-2}	$cm^2/(V \cdot s)$
Sub-threshold slop (SS)	5.73	5.65	V/dec
Threshold Voltage (V_{TH})	-1.9	-2.2	Volt
I_{on}/I_{off}	10^5	10^5	(Ratio)

For mobility, we set the values of the hopping model variable with the help of the literature and recursion of simulations. The charge transport model studied charge creation and recombination to predict the charge flow. This model takes into account temperature and field dependence of charge transport to give pragmatic simulation results at various operating conditions.

The current flow lines are displayed using Silvaco ATLAS simulation with TonyPlot. Figure 6(b) shows the flow of charge carriers across the OSC layer. The simulation produced graphs of drain current (I_{DS}) vs. gate voltage (V_{GS}) and drain voltage (V_{DS}). These results were verified using experimental data to validate the simulation. Figure 3 (a) illustrates the I_{DS} vs. V_{GS} graph in both logarithmic and standard scales. The logarithmic scale offers a sharper perspective at low current values, while the regular scale illustrates the overall I_{DS} vs. V_{GS} relationship.

Figure 3 (b) shows simulated and experimental data for I_{DS} vs. V_{DS}. This comparison verified that the simulation results matched the experimental data. The graph illustrates the similarities and discrepancies between the simulated and actual data, enabling researchers to assess the accuracy of the simulation.

The threshold voltage, obtained by the graphical technique given in Figure 6(a), was extracted to be approximately -2.2 V. The Table 4 shows comparison of experimental and simulated device performance parameter.

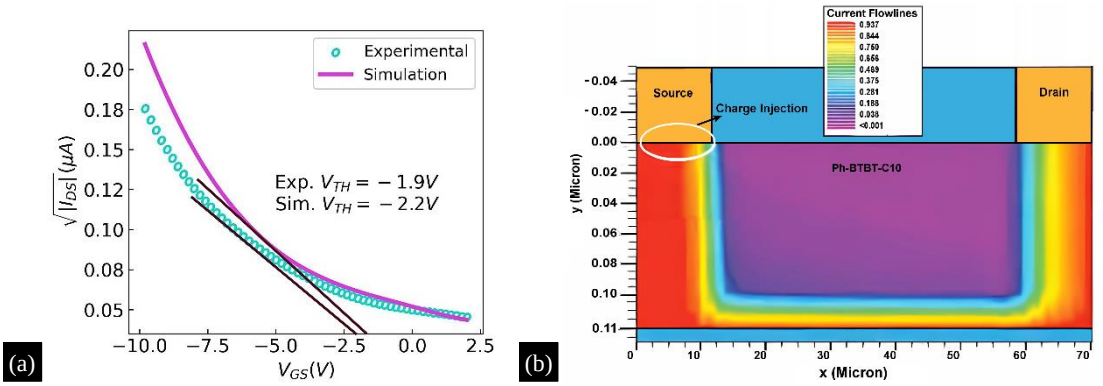


Figure 6. Threshold Voltage Extraction using Graphical Method. (b)Simulation Shows Charge Concentration and Charge Flow Lines Generated in Tonyplot.

COMPACT MODELING

Compact modelling is a useful tool in integrated circuit (IC) design. This assists in understanding the behaviour of circuit elements in a detailed but efficient manner. These models form an integral part of computer-aided design (CAD) and simulation, thus revolutionising electronic design. Compact models can capture the intricacies involved in various devices by incorporating some key features of the fabrication technology using physics-based analytical expressions. Complex device characteristics are represented through these expressions, which are further improved with specifics regarding the manufacturing processes used in such technologies. In fact, when included within circuit simulators during IC design, it gives complete insights into circuit behaviour. Figure 7 shows the components of the Compact Model.

I_{DS} is a key component of the DC analysis. For the AC, DC, Transient and Noise simulations, these are the key driving elements which are obtained from partial derivatives as seen below. Two voltage variables V_{GS} and V_{DS} may be employed to identify changes in I_{DS} which reflect transconductance and output conductance respectively [41]. These formulas are shown below:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=const} \tag{25}$$

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}}\Big|_{V_{GS}=const} \tag{26}$$

For drain current computation in TFT model, the inherent voltages (V_{GS} and V_{DS}) have to be employed. This equation is discussed in Refs. [42].

$$I_{DS} = G_{ch} \cdot V_{dse} \cdot (1 + \lambda \cdot V_{DS}) \tag{27}$$

Channel conductance (G_{ch}) and fitting parameter for output conductance modulation λ might be characterised as an important effect. V_{DS} is modulated with V_{dse} variable, includes saturation and sharpness of transition. In Ref. [43] a on modification of V_{DS} is provided as bellow:

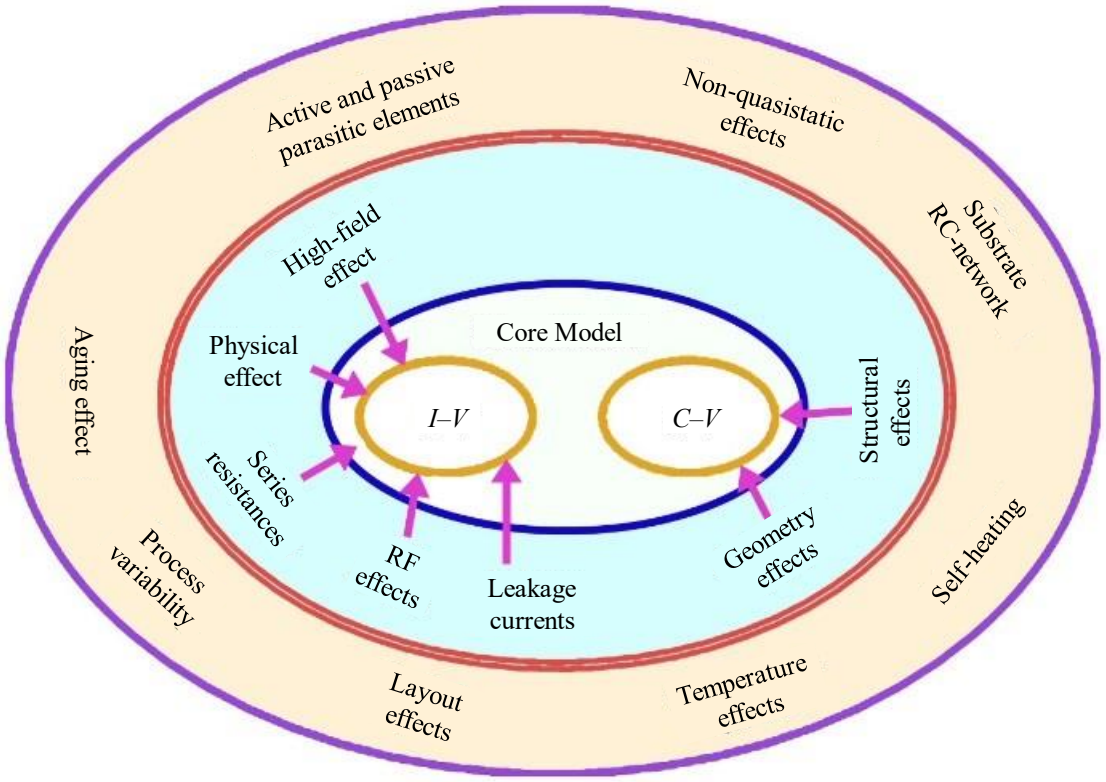


Figure 7. Representation of Compact Model.

$$\mathbf{V_{dse}} = \frac{\mathbf{V_{DS}}}{\left[\mathbf{1}+\left(\frac{\mathbf{V_{DS}}}{\mathbf{V_{dsat}}}\right)^{\mathbf{M}}\right]^{\frac{\mathbf{1}}{\mathbf{M}}}} \tag{28}$$

'M' is extracted by drawing two straight lines on curve of the drain current (I_D) vs. gate-to-source voltage (V_{GS}). The first line should on saturation regime and second on linear regime of experimental data, the slope of the line best fits the transition between the saturation and linear regimes [44]. It can also be estimated using Eq.

$$I_{lin} = I_{sat} - \Delta I \approx I_{sat}/2^{1/M} \tag{29}$$

$$M \approx \frac{\log(2)}{\log[I_{sat}/(I_{lin})]} \approx \frac{\log(2)}{\log[I_{sat}/(I_{sat}-\Delta I)]} \tag{30}$$

If M is larger linear regimes change more sharply in saturation regime Smaller M draw the smooth transition between the saturation and linear regimes. The saturation voltage approximation is

$$V_{dsat} = \alpha_{SAT}(V_{GS} - V_{TH}) \tag{31}$$

Saturation modulation parameter α_{SAT} may be calculated by analysing the gate voltage and drain voltage of experimental data. At the point when linear region transit to saturation region, the ratio of the drain current represent α_{SAT} . This parameter is not insignificant for long conducting channels, but can be significant for short channels. The channel conductance is defined as

$$G_{ch} = \frac{q \cdot N_s \cdot W_{eff} \cdot \mu_0}{L_{eff}} \tag{32}$$

$$N_s = \frac{\epsilon_{r_{di}} \cdot \epsilon_0 \cdot V_{gte}}{q \cdot t_{di}} \cdot \left(\frac{V_{gte}}{V_{AA}}\right)^{\gamma} \tag{33}$$

$$V_{gte} = \frac{V_{MIN}}{2} \cdot \left[1 + \frac{V_{gt}}{V_{MIN}} + \sqrt{\Delta^2 + \left(\frac{V_{gt}}{V_{MIN}} - 1\right)^2}\right] \quad (34)$$

$$V_{gt} = V_{GS} - V_{TO}(\text{Temp});$$
$$V_{TO}(\text{Temp}) = V_{TH} + K_{VT}(\text{Temp} - 300\text{K}) \quad (35)$$

The thickness of the dielectric is shown as t_{di}, and the gate dielectric's relative permittivity as $\varepsilon_{r_{di}}$. These have been described earlier. The power law mobility factor γ influences the relationship between the gate voltage overdrive and the channel conductance.

The equation for V_{gte} is an adjustment of the gate voltage [45], V_{AA} [43] represents the characteristic voltage for minimum field-effect mobility and determines the number of tail states in the DOS. Both V_{AA} and γ have been adjusted such that computation converges. It is fine-tuned using parameters such as transition width, (Δ), the minimum value of the effective gate voltage (V_{MIN}), and the temperature coefficient of the threshold voltage (K_{VT}). When creating an efficient circuit simulator or device model it's necessary to choose these parameters in such a way that they will provide for desirable resolution or sampling size and guarantee convergence.

In the simulation, it was observed that the effect of a higher drain-to-source voltage on OTFTs may be captured by the output conductance modulation (λ). A higher value of V_{DS} leads to an increase in I_{DS}, It also dependents on the device channel length. In short-channel devices, this effect is more pronounced. It helps provide a more accurate representation of OTFT behaviour by including λ in the drain current equation. The role of λ in the drain current equation also allows for better modeling of how the device responds to variations in V_{DS}.

In Figure 8 (a), I_{DS} becomes linear with respect to V_{DS}. Higher values of λ lead to an increased modulation effect implying that at higher V_{DS} the drain current increases sharply even in the saturation regime. However, smaller values for λ depict a weaker channel-length modulation effect resulting in less change in drain current for any given increment in V_{DS}. Typically, λ ranges between 10^{-3} and 10^{-8} depending on average output drain currents and channel lengths (output range). The value of λ is influenced by several factors such as the technology node (size of transistors on the circuit), doping concentration in the channel region and semiconductor material properties.

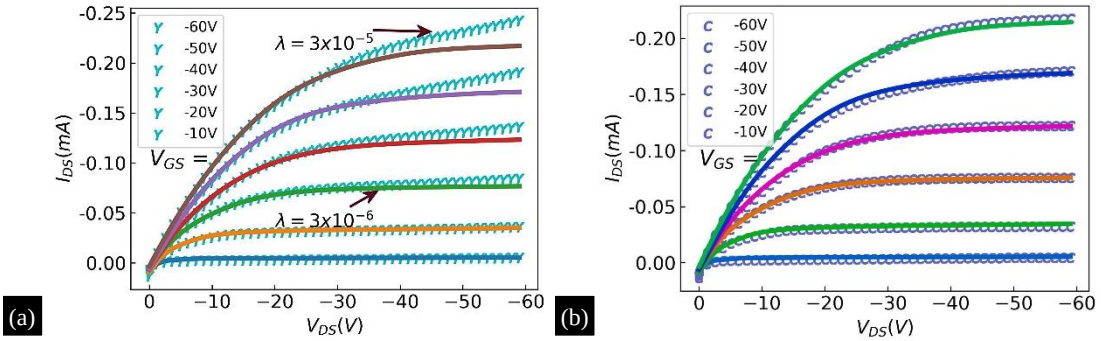


Figure 8. (a) Effect of λ Output Conductance Modulation Parameter (b) Compact Model Output Characteristic Fitted with Experimental Data

λ		3.10×10^{-6}	1/V
M		1.16	
α_{SAT}		0.58	
V_{MIN}		−1.50	V

Δ		4.0	
V_{TO}		-1.21	V
μ_0		4.3×10^{-2}	$cm^2/(V \cdot s)$
T_{OX}		1.80×10^{-9}	m
V_{AA}		1.72	V
γ		1.10	
V_0		2.66×10^{-2}	V
G_{MIN}		1.3×10^{9}	$m^{-3}eV^{-1}$
V_{FB}		-0.51	V
K_{VT}		-2.4×10^{-2}	$V/^{\circ}C$

The discussed parameter 'M' is another significant one in the context of curve fitting and it is necessary to provide control of the curve and define the transition from one operating area to another. In a particular circuit or an individual basic building block circuit, the value of M would have different values depending on how OTFT behaves. This may also be influenced by various OSC materials and device geometries. The typical value ranges between 2.5 to 1.3.

At M = 2.5, there will be a sharp knee-like bending in its curve as it goes from linear region (saturation). At M = 1.3, on other hand, transistor possesses a smoother transition which is gradual from linear to saturation region. All other parameter effects are observed but important has been discussed.

Thus, the compact model simulations of Ph-BTBT-C10 OTFT have successfully replicated the experimental I_{DS} vs. V_{DS} characteristics which are ascertained. Excellent agreement with experimental data, as depicted in Figure 8 (b), is achieved by iterative adjustment of model parameters across multiple simulation cycles. The values of all the parameters are shown in Table 5. The ability to accurately predict device behaviour under varying voltage conditions has been shown by the simulations. This indicates how reliable it is when capturing key operational aspects that are essential for optimising OTFT designs.

Table 5. Simulated vs. Experimented Performance Parameters Compassion.

Parameter	Description	Value	Unit
λ	Output conductance parameter	3.10×10^{-6}	$1/V$
M	Knee shape parameter	1.16	-
α_{SAT}	Saturation modulation parameter	0.58	-
V_{MIN}	Minimum Value of V_{gte}	-1.50	V
Δ	Transition width parameter	4.0	-
V_{TO}	Zero-bias threshold voltage	-1.21	V
μ_0	Conduction band mobility	4.3×10^{-2}	$cm^2/(V \cdot s)$
T_{OX}	Thin-oxide thickness	1.80×10^{-9}	m
V_{AA}	Characteristic voltage for gate voltage	1.72	V
γ	Power law mobility parameter	1.10	-
V_0	Characteristic voltage for deep states	2.66×10^{-2}	V
G_{MIN}	Minimum density of deep states	1.3×10^{9}	$m^{-3}eV^{-1}$
V_{FB}	Flat band voltage (type-dependent)	-0.51	V

K_{VT}	Threshold voltage temperature coefficient	-2.4×10^{-2}	V/ °C

CIRCUIT SIMULATION

One way of overcoming the limitations of n-type organic semiconductors (OSCs) is by using zero-load logic (ZLL) inverters. This is because these types of inverters are exclusively made from p-type OSCs, thereby doing away with n-types which are in short supply. By simplifying circuit design by reducing the overall semiconductor requirements they use, ZLL inverters employ dynamic load logic (DLL). Moreover, they make it possible for one to achieve energy-efficient operation, better noise robustness and low-cost mass production hence making them a good choice when it comes to the problem of material scarcity in organic inverter circuits.

A capacitor as a load that charges and discharges periodically to stabilize output voltage underlies typical DLL approach. High gain and low power consumption in inverters can be achieved using this method. The ZLL inverter is an example of a DLL inverter built with p-type transistors. In this setup, Figure 9(a) shows the constant conducting p-type transistor's drain being connected to the output. When the input is low, the output is high and vice versa. Another example is diode-load inverter where its output is connected to drain-gate junction of a p-type transistor acting as a diode. Once again, when its input is low its output goes high and when its input becomes high then its output falls down low too.

The inverter's input-output characteristics are shown by the simulation results in Figure 9 (b). This plot represents how changes in input voltage (V_{in}) cause output voltage (V_{out}) to vary. There is always on and off states depicted as high and low voltage respectively when it comes to an inverter circuit since its output voltage shifts between these modes when the input crosses specific thresholds, implying that this device can be employed for digital logic operations.

The simulation also educates designers on parameter optimization like transistor sizes, biasing conditions, and interconnects, hence validating their designs. These design improvements increase the speed of operation, minimize power loss and allow a good spread of noise margins among others which are vital for real-world applications.

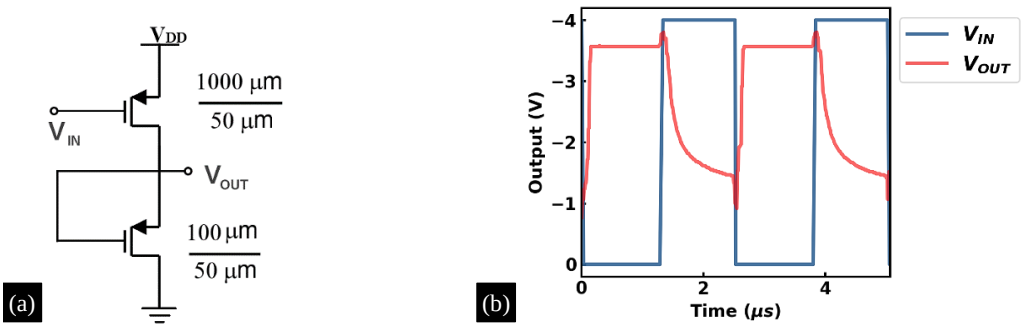


Figure 9. (a) Inverter circuit using Ph-BTBT-C10 OTFT (b) Input-Output Characteristics of Inverter.

CONCLUSION

The study focus the discussion of organic semiconductor device where we delve into the intricate world of compound physical phenomenon theory, with particular emphasis on energy bandgap. This study has been adapted for Ph-BTBT-C10 OSC devices and tested against real experimental data. The final model has a high degree of realism as can be seen from the simulated parameters closely matching the experimental observations. In conclusion, TCAD simulation offers a complete outline for research purposes and enhancing the performance of semiconductor devices. Implementation of small models into Utmost IV SILVACO enhances our understanding and makes it possible to carry out experiments in practice By using such a small model, we modeled an inverter circuit within SMART SPICE SILVACO that smoothly transformed theoretical modeling to practical implementation By doing so,

we intend not only to affirm the efficacy of compact model but also its suitability to circuit level simulations bench marking towards sophisticated electronic systems As such, through extensive testing and advanced modelling, there were groundbreaking insights about dynamic behaviour as well as performance analysis of semiconductor device. By bridging theoretical knowledge and practical application, we contribute significantly to the ongoing advancement of electronic devices and systems, encouragement innovation and propelling the field of semiconductor engineering forward.

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