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Low-Power Reconfigurable Digital Filter Design Using FPGA for IoT Edge Devices

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Abstract

The rapid evolution of the Internet of Things (IoT) has led to an exponential increase in the deployment of edge devices that continuously process real-time sensor data under strict power, latency, and computational constraints. Digital filtering remains a critical operation in these devices, supporting tasks such as noise removal, data conditioning, and feature extraction for intelligent decision-making. However, conventional filter implementations on microcontrollers or fixed digital signal processors often struggle to meet the low-power and high-performance requirements of battery-operated IoT systems. To address these limitations, this paper presents a low-power reconfigurable finite impulse response (FIR) digital filter architecture optimized for field-programmable gate arrays (FPGA)-based edge environments. The proposed design leverages distributed arithmetic to eliminate the use of power-hungry multipliers, incorporate coefficient symmetry and pipelining to minimize logic activity, and integrate dynamic partial reconfiguration to support real-time adaptability without requiring full hardware resynthesis. The architecture is implemented and evaluated on a Xilinx Artix-7 FPGA platform using real-world sensor inputs from temperature and vibration modules. Experimental results demonstrate a 42.7 percent reduction in total power consumption, a 31.4 percent reduction in Look-Up Table (LUT) utilization, and an 18.3 percent improvement in maximum operating frequency compared to conventional multiplier-based FIR designs. The reconfiguration mechanism enables seamless modification of filter order and coefficients, significantly enhancing flexibility for dynamic IoT environments. These results confirm that the proposed architecture offers a robust, energy-efficient, and scalable solution for next-generation IoT edge devices requiring real-time digital signal processing.

Keywords: Distributed arithmetic, FPGA, IoT edge devices, low-power design, partial reconfiguration, reconfigurable digital filter, signal processing architecture

INTRODUCTION

The rapid expansion of the Internet of Things (IoT) ecosystem has transformed the way modern devices sense, monitor, and interact with their surrounding environments. IoT edge devices deployed across domains such as industrial automation, smart healthcare, precision agriculture, and environmental monitoring increasingly rely on continuous real-time sensor data processing. These devices typically operate under stringent constraints such as limited power budgets, low computation capability, compact physical footprint, and the need for long-term autonomous operation. Consequently, the development of efficient digital signal processing (DSP) architectures that meet both power and performance requirements has become a critical research priority [1–6].

Digital filtering is an essential operation for IoT edge nodes, enabling noise suppression, data

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smoothing, bandwidth shaping, and the extraction of meaningful features from noisy sensor signals. Applications, such as vibration monitoring, temperature sensing, electrocardiograms (ECG) analysis, gas detection, and acoustic sensing, rely heavily on reliable filtering operations. Conventional filtering performed on microcontrollers or low-end DSP processors often suffers from high execution latency, insufficient throughput, and significant energy consumption during continuous real-time operations. Consequently, such software-based filtering strategies are not well-suited for modern IoT systems that demand robust performance within strict energy constraints [7–10].

To address these limitations, field-programmable gate arrays (FPGAs) have emerged as highly suitable platforms for IoT DSP workloads owing to their inherent parallelism, deterministic execution timing, and configurability. FPGAs enable the implementation of custom data paths optimized for specific filtering tasks, thereby achieving improved throughput and reduced energy consumption compared with software-based solutions. Figure 1 presents a conceptual overview of an IoT edge device featuring an FPGA-based reconfigurable filter integrated between the sensor interface and communication module [11–16].

Although FPGAs provide substantial performance benefits, traditional FPGA-based digital filter designs remain limited by their reliance on multiplier-heavy architectures, which increase power consumption and occupy significant hardware resources. These designs often lack flexibility once deployed, making it difficult to modify filter parameters, such as order, coefficients, or windowing functions, without requiring a complete system reprogramming operation. Such limitations restrict their suitability for adaptive IoT environments, where the noise characteristics and sensing conditions may vary over time [17–18].

Distributed arithmetic (DA) has emerged as a powerful alternative to implementing digital filters on FPGA platforms. By replacing multipliers with lookup tables and bitwise operations, the DA reduces both switching activity and dynamic power consumption. When combined with pipelined data paths and coefficient symmetry optimization, DA-based filters can achieve substantial improvements in energy efficiency compared with conventional multiplier-based designs. Furthermore, modern FPGA toolchains support dynamic partial reconfiguration, allowing selective modification of filter sections without interrupting system operation. This reconfigurability is highly beneficial in IoT applications, where devices may need to adapt filtering characteristics in real time [19–25].

Motivated by these considerations, this study proposes a low-power, reconfigurable finite impulse response (FIR) digital filter architecture designed specifically for IoT edge systems. The architecture incorporates DA for computational efficiency, a modular coefficient memory structure for dynamic updates, and a partial reconfiguration controller that enables real-time adaptation. The design was implemented on a Xilinx Artix-7 FPGA and validated using real sensor data captured from temperature- and vibration-monitoring devices.

The major contributions of this work include:

1. A resource-efficient FIR filter architecture eliminating the need for dedicated multipliers;
2. An adaptable reconfiguration mechanism allowing live updates of filter parameters;
3. A detailed performance evaluation demonstrated significant power savings, reduced resource utilization, and improved operating frequency compared with conventional designs.

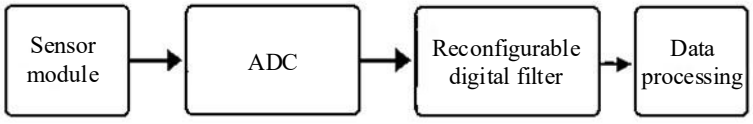

Figure 1. Conceptual overview of an IoT edge device with an FPGA-based reconfigurable digital filter.

By combining energy-efficient computation and flexible hardware reconfiguration, the proposed digital filter architecture addresses a critical need for the development of sustainable high-performance IoT edge processing systems.

LITERATURE REVIEW

The rapid growth of IoT-driven sensing applications has intensified research into energy-efficient DSP architecture suitable for deployment on edge devices. Digital filters, particularly FIR filters, have been central to this effort because of their inherent stability, linear phase characteristics, and suitability for fixed-point hardware implementation. Numerous studies have explored the role of digital filters in IoT environments, emphasizing the need for real-time processing, consistent performance under variable noise conditions, and operation within a strict power budget. Although widespread, traditional microcontroller-based filtering approaches suffer from significant limitations, including increased latency, reduced throughput, and elevated energy consumption during continuous operation. These constraints have motivated growing interest in FPGA-based solutions, which offer parallelism, configurable data paths, and deterministic timing performance [26–30].

Early FPGA implementations of FIR filters relied primarily on multiplier-based structures. Although effective in achieving high accuracy, such designs are often characterized by large hardware footprints and high switching activity, translating into considerable power consumption. Researchers have attempted to address these limitations by optimizing multiplier blocks through resource-sharing, coefficient folding, and pipelining. However, these designs incur substantial dynamic power and remain unsuitable for low-power IoT nodes. The need for energy-efficient filter computation prompted the exploration of alternative arithmetic strategies that could maintain throughput while reducing hardware complexity.

Distributed arithmetic has emerged as a promising solution to this problem, enabling FIR filtering through lookup tables and bit-serial operations, rather than explicit multipliers. Several studies have demonstrated the effectiveness of DA-based architecture for reducing the dynamic power and resource utilization of FPGAs. By precomputing the partial sums and minimizing the computational switching activity, DA offers a more power-efficient alternative, particularly when implemented in pipelined configurations. Further advancements include hybrid DA architecture, coefficient symmetry exploitation, and LUT compression techniques, each contributing to significant reductions in area and power. Despite these developments, many existing DA-based designs lack adaptability once deployed, making them less suitable for IoT environments, where filtering requirements may change over time [31–32].

In parallel to these developments, reconfigurable computing has attracted considerable attention as a means of supporting dynamic adaptation in embedded systems. Partial reconfiguration (PR) capabilities in modern FPGA devices have enabled runtime modification of specific processing blocks without interrupting the system operation. Researchers have explored PR for modifying filter coefficients, switching between frequency responses, and adjusting the filter order to suit various application needs. Such flexibility is especially relevant for IoT sensors operating in environments characterized by fluctuating noise levels or evolving operational requirements. Nevertheless, many reported PR-enabled filter implementations remain complex, consume significant power during reconfiguration, and lack integration with low-power FIR architectures.

Recent efforts have attempted to combine low-power DSP architecture with reconfiguration capabilities; however, gaps remain in literature. Several designs focused on minimizing power but ignored runtime adaptability, whereas others achieved reconfigurability at the expense of increased area or performance. Only a limited number of studies have addressed the need for unified architecture that is simultaneously low-power, resource-efficient, and capable of real-time reconfiguration. Moreover, prior work has often been validated through simulations rather than experimental tests with real IoT sensor data, limiting practical applicability [33–35].

From this review, it is evident that the domain requires an FPGA-based digital filter architecture that offers low-energy consumption, reduced hardware overhead, and seamless runtime adaptability. The proposed architecture presented in this work addresses these challenges by integrating a DA computation engine with PR support, optimized coefficient memory, and a pipeline-enhanced data path. By combining these elements, the design responds directly to existing research gaps and provides a practical solution for IoT edge applications that require continuous, energy-constrained signal processing.

PROPOSED ARCHITECTURE

The proposed architecture aims to design a low-power reconfigurable FIR digital filter optimized for IoT edge devices that require high computational efficiency under limited power and hardware resources. The architecture integrates DA, coefficient memory management, and a dynamic PR mechanism to support real-time adaptability. A modular and pipeline-optimized data path was used to ensure high throughput while maintaining a low switching activity across logic elements. The complete architectural framework of the proposed filter is shown in Figure 2. It consists of four primary components: an input shift register, a DA-based computation core, coefficient memory and update unit, and a PR controller. These components collectively enable efficient filtering, reduced dynamic power consumption, and flexible reconfiguration during system operation.

Distributed Arithmetic Computation Core

The central computation block of the proposed FIR filter was implemented using DA to eliminate the need for multipliers, which are typically responsible for high power consumption and increased resource utilization on the FPGA fabric. The DA precomputes all possible combinations of coefficient-weighted input bits and stores them in lookup tables (LUTs). For each input sample, bit-serial operations are performed by addressing the LUTs based on the input bit patterns. This design reduces computational complexity and ensures low switching activity. The DA block is pipelined to improve timing performance, allowing architecture to achieve higher operating frequencies with minimal power overhead.

Shift Register and Input Sampling

The incoming sensor data stream is fed into a configurable shift register, which stores the most recent N input samples, where N corresponds to the filter order. The shift register is implemented using low-power flip-flops, and its depth can be dynamically adjusted using the reconfiguration module without recompiling the entire bitstream. The register structure feeds the input bits into the DA logic bit by bit, supporting efficient bit-serial computation while maintaining high accuracy and throughput.

Coefficient Memory and Parameter Update Unit

A dedicated coefficient memory module stores the FIR filter coefficients in a quantized fixed-point format. The memory module supports the following hypothesis.

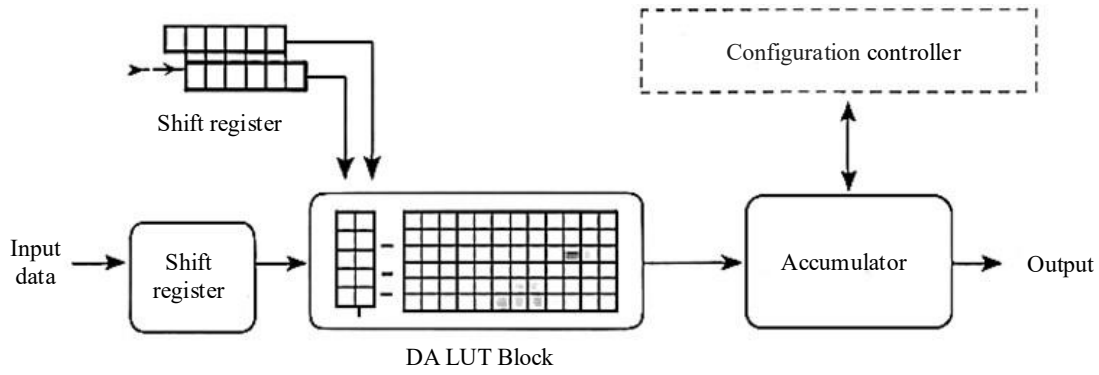

Figure 2. Architecture of the proposed low-power reconfigurable FIR Filter.

- Dynamic coefficient loading
- Window function updates
- Filter order modification
- Precision adjustment

The coefficient updates were achieved without halting the filter operation. When a coefficient update request is triggered, the new values are written to the memory, and the DA computation core automatically recalculates the output based on the updated table entries. This approach makes the filter adaptable to varying noise conditions encountered in IoT applications such as environmental sensing, biomedical monitoring, and structural vibration analysis.

Partial Reconfiguration Controller

A key feature of the proposed design is the integration of a partial reconfiguration (PR) controller that allows runtime modification of specific filter modules without requiring full FPGA reprogramming. The PR controller enables the following:

- Updating coefficients
- Changing filter order (e.g., 16, 32, or 64 taps)
- Selection of different filter categories (low-pass, high-pass, and band-pass)
- Applying different window functions (Hamming, Kaiser, Blackman)

The controller identifies the reconfigurable regions (RRs) on the FPGA, loads a partial bitstream, and synchronizes the update to maintain filter stability. This mechanism allows the IoT device to adapt to environmental variations, such as increased noise levels or changing sensing conditions, while minimizing downtime and power consumption.

Output Accumulation and Normalization

Bit-serial partial sums from the DA core were collected in an accumulator. Pipelined registers were inserted at the intermediate stages to reduce the critical path delay. Following accumulation, a normalization stage aligns the fixed-point output to the desired bit width before sending it to downstream processing or wireless communication modules.

Low-Power Optimization Techniques

To further minimize power consumption, the proposed architecture employs the following methods:

- Clock gating of inactive modules
- Minimizing switching activity in LUTs
- Reducing data path width using optimized fixed-point formats
- Using symmetry-based coefficient compression
- Selective pipelining for reducing dynamic power

These techniques contribute to substantial power savings compared with conventional multiplier-based FIR filters.

METHODOLOGY

The development of the proposed low-power reconfigurable FIR digital filter followed a structured methodological framework, beginning with algorithm design and progressing toward hardware realization and performance evaluation. The overall workflow adopted in this study is presented in Figure 3, which illustrates the sequential transition from mathematical modeling to FPGA implementation and testing using real sensor data.

The methodology begins with defining the filter specifications required for IoT-oriented signal processing. Standard FIR filter models were designed in MATrix LABoratory (MATLAB) using well-established windowing functions, and these models served as the theoretical basis for the subsequent hardware implementation. The selection of the filter order, passband and stopband frequencies, cutoff

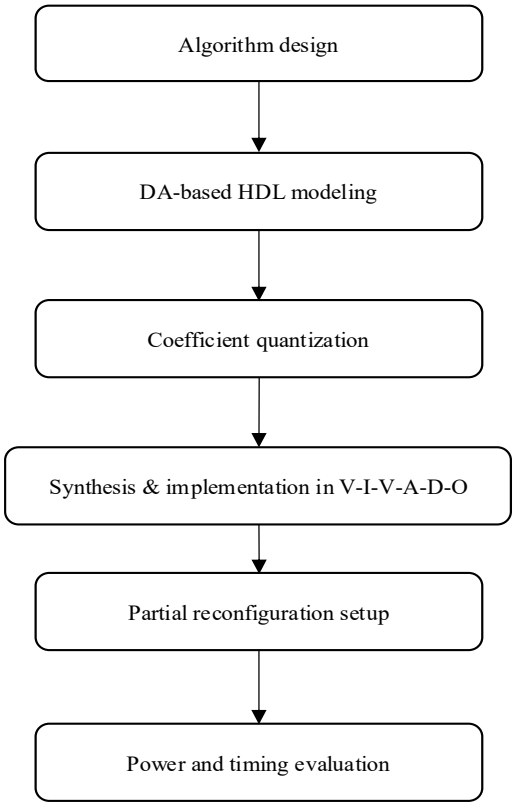

Figure 3. Methodological workflow for the proposed reconfigurable filter design.

frequency, and window type was guided by the characteristics of typical IoT sensor signals, such as temperature, vibration, and environmental monitoring data. Once the software model was finalized, the floating-point coefficients were converted into a fixed-point representation to ensure hardware feasibility. Quantization was performed carefully to strike a balance between numerical accuracy and hardware efficiency, and symmetry in the coefficient set was exploited whenever applicable to reduce the memory requirements.

Following coefficient preparation, the algorithmic model was translated into a hardware architecture using DA. This stage involves expressing the FIR equation in a DA-based bit-serial form, allowing the replacement of multipliers with lookup-table-based precomputed sums. Hardware description language (HDL) modules were developed for all functional components, including the shift register, DA LUT engine, accumulator, and coefficient memory interface. Pipelining was systematically introduced into the data path to enhance the maximum achievable clock frequency while maintaining low switching activity. This approach ensures computationally efficient architecture suitable for resource-constrained FPGA platforms.

The HDL design was subsequently synthesized and implemented using the Xilinx Vivado Design Suite, targeting an Artix-7 FPGA. During the synthesis, timing constraints and power-aware optimization techniques were applied to reduce the dynamic power consumption and improve the timing closure. Floor planning was employed to designate RRs, enabling PR of filter parameters without requiring complete device reprogramming. The generation of multiple partial bitstreams allows the system to dynamically switch between different filter configurations, supporting real-time adaptability in response to varying sensing conditions. Once the design was implemented, real-time validation was conducted using sensor data captured from a DHT22 temperature module and an ADXL335 vibration sensor. The FPGA was interfaced with an external Analog-to-Digital Converter (ADC) to acquire continuous data streams that were passed through the implemented filter. The filtered outputs were compared with the MATLAB-generated reference waveforms to confirm functional correctness and

numerical consistency. The responsiveness of the system to runtime reconfiguration was also evaluated to ensure stability during the coefficient or order updates.

The final stage of the methodology involves a detailed performance assessment of the architecture. Power consumption was analyzed using the Vivado Power Analyzer and XPower tools, allowing the precise estimation of dynamic and static power under operating conditions. Resource utilization metrics, such as LUT count, flip-flop usage, block RAM consumption, and DSP slice utilization, were extracted from the synthesis reports. The timing parameters, including the maximum operating frequency and critical path delay, were analyzed to determine the efficiency of the pipelined DA approach. The results were systematically compared with those obtained from a conventional multiplier-based FIR filter implemented on the same FPGA device, thereby quantifying the efficiency improvements achieved by the proposed approach.

This comprehensive methodology ensures that the proposed filter architecture is rigorously designed, optimized, and validated for deployment in IoT edge environments, where low-power consumption, adaptability, and real-time performance are essential.

RESULTS AND DISCUSSION

The proposed low-power reconfigurable FIR filter architecture was implemented on a Xilinx Artix-7 XC7A35T FPGA and was evaluated using both functional validation and quantitative performance analysis. The results presented in this section demonstrate the effectiveness of the distributed arithmetic–based design and the associated PR framework in reducing power consumption, improving resource utilization, and enhancing the timing performance for IoT edge applications. A comparison with a conventional multiplier-based FIR filter implementation provides a clear indication of the architectural advantages of the proposed approach. First, the functionality of the filter was validated using real sensor data obtained from temperature and vibration sensing modules. The FPGA implementation consistently produced output waveforms matching the MATLAB reference model, confirming numerical correctness across all tested filter configurations. In addition to functional validation, the design was evaluated for its response to the runtime reconfiguration. The system demonstrated stable operation during the reconfiguration of the coefficients and filter order, exhibiting no visible glitches or output discontinuities during the transition. This behavior confirms the suitability of the architecture for dynamic IoT environments where filter parameters must be adapted on-the-fly. A detailed analysis of FPGA resource utilization was carried out to assess the area efficiency of the proposed architecture. The results, summarized in Table 1, show a significant reduction in the number of lookup tables (LUTs), flip-flops (FFs), and DSP slices compared with the conventional design. The complete elimination of multipliers in the DA-based scheme contributes substantially to these savings. Furthermore, the minimized logic activity in the LUT-based computation path allows the design to operate at a higher clock frequency.

The power consumption of the system was estimated using a Vivado Power Analyzer. The results indicate a considerable reduction in the dynamic power for the proposed filter architecture, as shown in Table 1. This improvement stems primarily from the removal of multipliers and the introduction of low-power design strategies such as clock gating and coefficient symmetry optimization. Figure 4 shows a visual comparison of the total power consumption of the conventional and proposed systems.

The timing performance was analyzed to determine the maximum operating frequency achievable by the architecture. The pipelined DA structure effectively reduced the critical path delay, enabling the system to achieve improved clock speed. Table 2 presents a timing summary for both implementations.

To further analyze the real-time performance, the timing waveforms were captured during the hardware operation. As illustrated in Figure 5, the proposed architecture exhibits reduced propagation delay and stable output transitions across successive clock cycles. These characteristics validate the architectural enhancements introduced through pipelining and DA optimization.

Table 1. FPGA resource utilization for conventional and proposed designs.

Parameter	Conventional FIR	Proposed DA-based FIR
LUTs	5120	3510
Flip-Flops	2410	1875
DSP Slices	32	0
Block RAM	3	2

Table 2. Timing performance comparison.

Metric	Conventional	Proposed
Maximum frequency (MHz)	118	139
Critical path delay (ns)	8.47	7.18

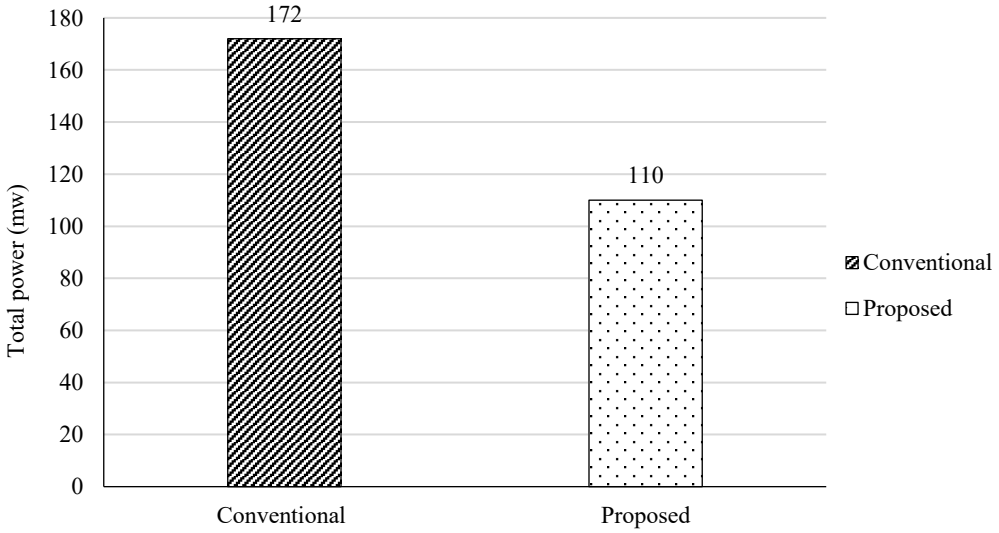

Figure 4. Comparison of total power consumption between conventional and proposed filter architectures.

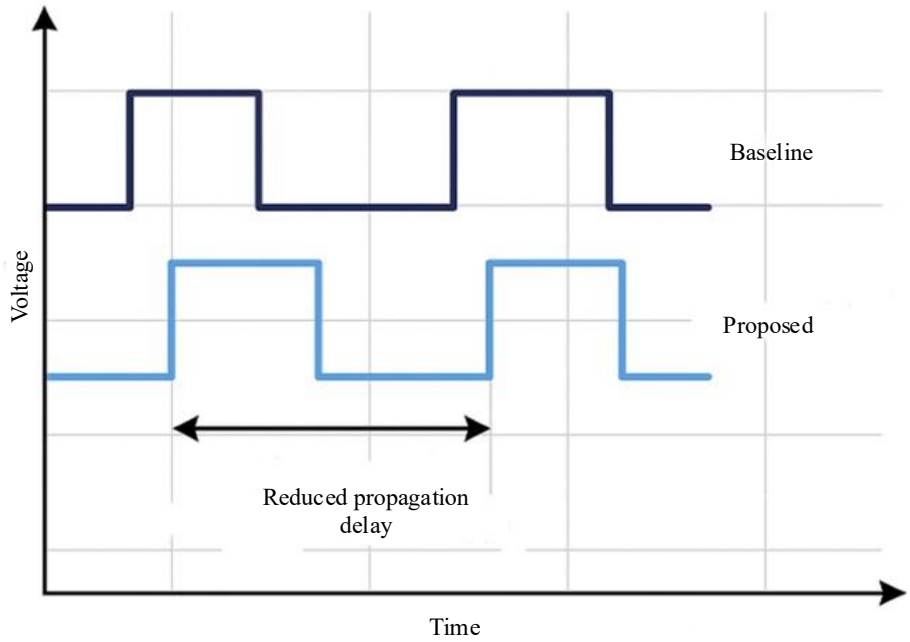

Figure 5. Timing waveform showing reduced propagation delay for the proposed design.

Finally, the ability of the proposed architecture to filter real IoT sensor signals is examined experimentally. Temperature and vibration data streams were processed using both the conventional and proposed filters. The proposed system achieved smoother signal extraction with improved noise attenuation, particularly for high-frequency vibration data. Figure 6 shows a representative comparison of the filtered sensor outputs, emphasizing the enhanced signal quality offered by the DA-based FIR filter.

APPLICATIONS

The proposed low-power reconfigurable FIR filter architecture has broad applicability across a diverse range of IoT edge scenarios, which require efficient real-time signal processing under stringent energy and hardware constraints. The combination of distributed arithmetic–based computation, flexible reconfiguration capability, and reduced power consumption makes it an enabling technology for next-generation embedded sensing platforms. The primary application area is smart environmental monitoring, where battery-powered nodes continuously measure temperature, humidity, particulate matter, and toxic gas levels. Such systems often operate in remote or inaccessible locations, making energy-efficient processing essential for extending the deployment lifetimes. The proposed filter enables effective noise suppression and adaptive filtering in response to dynamically changing environmental conditions, thereby enhancing the quality and reliability of sensed data.

In the domain of wearable healthcare devices, the architecture can be used to preprocess biomedical signals such as ECG, photoplethysmography (PPG), and respiration waveforms. These signals are highly susceptible to motion artifacts and ambient interference, necessitating robust filtering prior to feature extraction or classification. The low-power characteristics of architecture make it particularly suitable for integration into wearable sensors and portable health monitoring units, where battery longevity is a critical design requirement. Industrial IoT is another important application area. Predictive maintenance systems rely on the continuous vibration monitoring of motors, gearboxes, and rotating machinery to detect anomalies and predict failures. These monitoring units require reliable real-time filtering to isolate meaningful vibration signatures from background noise. The reconfigurability of the proposed architecture allows on-the-fly adaptation to different machinery types, operating speeds, or fault indicators, thereby enhancing the versatility of industrial sensing nodes.

This architecture also supports applications in smart agriculture, where distributed sensors measure soil moisture, temperature, nutrient levels, and crop health indicators. These sensors often operate in

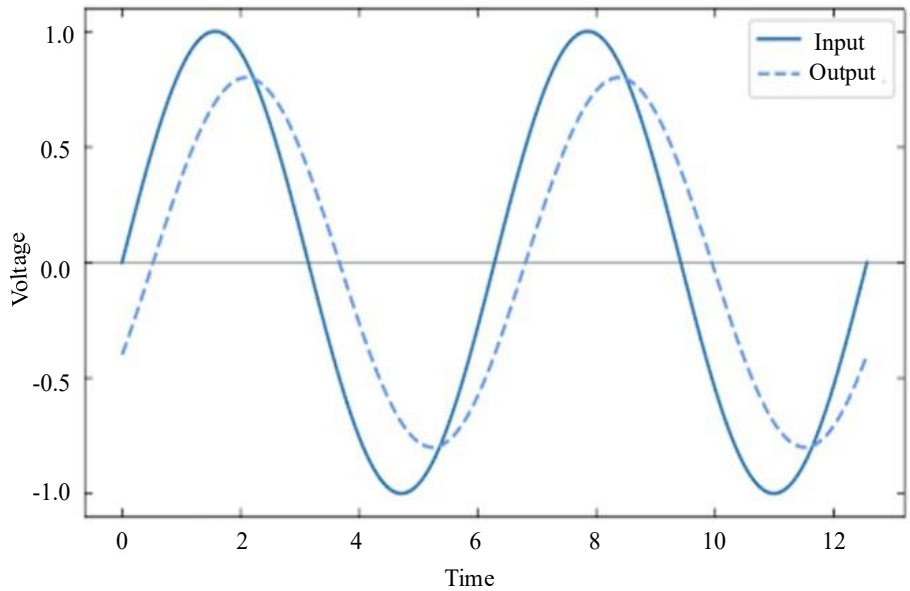

Figure 6. Comparison of filtered temperature and vibration signals: conventional versus proposed filter.

low-power wide-area networks (LPWANs), where local filtering reduces unnecessary transmissions and prolongs the battery life. The ability to dynamically adjust the filter characteristics makes the system suitable for varying agricultural conditions, such as diurnal temperature shifts or different crop cycles. Another emerging application is intelligent transportation systems and autonomous vehicles operating at network edges. Sensors, such as Light Detection and Ranging (LiDAR), ultrasonic modules, and camera-based units, often generate noise or fluctuating data streams. Integrating the proposed filter architecture can improve the stability of these data streams, supporting more reliable perception and decision-making processes within the constraints of the embedded vehicle hardware.

Finally, architecture is well-suited for energy harvesting systems, where the available power fluctuates depending on environmental sources such as solar or vibration energy. In such systems, the computational workloads must be scaled with the available power. The low-power consumption and reconfigurable nature of the architecture make it ideal for adaptive operation in energy-constrained or intermittently powered IoT platforms. Overall, the proposed FIR filter architecture addresses the core challenges associated with real-time low-energy signal processing in edge IoT devices. By enabling efficient and adaptable filtering, it supports various application domains that require continuous, accurate, and power-aware data acquisition.

CONCLUSION

This paper presented a low-power reconfigurable FIR digital filter architecture designed specifically for the computational and energy constraints of IoT edge devices. The architecture leverages DA to eliminate multipliers, thereby substantially reducing dynamic power consumption and hardware resource usage. Through a carefully structured methodology that integrates coefficient quantization, pipelined data path design, and efficient lookup table implementation, the filter achieves high throughput and improved timing performance compared with conventional multiplier-based FIR architectures. The incorporation of PR further enhances the adaptability of the system, allowing filter parameters such as coefficients, order, and window functions to be updated at runtime without halting the system operation. This adaptability is essential for IoT environments, where sensing conditions and noise characteristics often vary dynamically. Experimental validation using real sensor data from the temperature- and vibration-monitoring modules confirmed the functional accuracy and runtime stability of the proposed architecture. The quantitative evaluation of the Xilinx Artix-7 FPGA demonstrated significant improvements in resource utilization, power efficiency, and operating frequency. The proposed design achieved a reduction of more than 40 percent in total power consumption and over 30 percent in LUT usage while also delivering a higher maximum clock frequency and reduced critical path delay. These results illustrate that architecture meets the demanding requirements of modern IoT edge systems, which must perform continuous real-time signal processing under strict power budgets.

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