

Spintronic Logic Device Modeling and Energy Optimization for Beyond-CMOS Computing Systems

Bibhu Prasad Ganthia^{1,*}, Rosalin Pradhan²

Abstract

The continuous scaling limitations of conventional complementary metal-oxide semiconductor (CMOS) technology have accelerated the exploration of alternative computing paradigms for next-generation low-power and high-performance systems. Spintronic logic devices have emerged as a promising solution due to their non-volatility, ultra-low switching energy, high integration density, and compatibility with beyond-CMOS architecture. This research presents a comprehensive modeling and energy optimization framework for spintronic logic devices applied in beyond-CMOS computing systems. The proposed work investigates the electrical and magnetic behavior of spin-transfer torque (STT) and spin-orbit torque (SOT)-based logic structures under varying operational conditions. Device-level simulations are performed to analyze switching delay, power dissipation, thermal stability, and energy efficiency. An optimization methodology integrating adaptive bias control and magnetization switching minimization is introduced to reduce dynamic and leakage power consumption while maintaining computational reliability. The performance of the proposed spintronic architecture is compared with conventional CMOS-based logic systems in terms of switching energy, latency, and scalability. Simulation results demonstrate significant reductions in energy consumption and improved operational stability, making spintronic devices suitable for future artificial intelligence, neuromorphic, and edge-computing applications. To improve device flexibility under nanoscale manufacturing restrictions, the suggested approach integrates parameter-aware optimization techniques and scalable analytical models. Additionally, the study assesses how temperature fluctuations and material characteristics affect switching performance, enhancing the resilience and dependability of spintronic circuits for real-time computing settings. The study highlights the potential of spintronic technology as a sustainable and energy-efficient alternative for future nanoelectronics computing platforms.

Keywords: Spintronic logic devices, beyond-CMOS computing, energy optimization, spin-transfer torque, nanoelectronics, low-power computing

INTRODUCTION

The rapid advancement of artificial intelligence, the Internet of Things (IoT), edge computing, and high-performance data processing applications has significantly increased the demand for computing systems that are faster, smaller, and more energy efficient. For several decades, conventional complementary metal-oxide semiconductor (CMOS) technology has served as the backbone of modern electronic systems owing to its high scalability, low fabrication cost, and reliable switching characteristics. The continuous miniaturization of CMOS transistors, guided by Moore's law, has enabled exponential growth in computational capability and semiconductor integration density. However, as device dimensions approach the nanometer scale, conventional CMOS technology faces severe physical and technological

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limitations, including increased leakage current, excessive power dissipation, reduced threshold voltage control, short-channel effects, thermal instability, and interconnection delays. These limitations create significant barriers to further scaling and energy-efficient operation in next-generation computing architectures. Consequently, researchers and semiconductor industries are actively exploring beyond-CMOS technologies that can overcome these challenges while maintaining high computational performance and low-power consumption. Beyond-CMOS computing represents a new generation of electronic technologies that utilize alternative physical mechanisms, such as quantum effects, spin dynamics, memristive switching, and neuromorphic processing, to achieve superior energy efficiency and functional scalability compared to traditional charge-based CMOS systems. Among the emerging beyond-CMOS technologies, spintronics has gained considerable attention because it utilizes both the charge and intrinsic spin properties of electrons for information processing and storage. Unlike conventional CMOS circuits that rely solely on electron charge transport, spintronic devices exploit magnetic polarization and spin-transfer mechanisms to perform logic operations with significantly lower energy consumption and non-volatile data retention capability. Spintronic logic devices, such as spin-transfer torque magnetic tunnel junctions (STT-MTJs), spin-orbit torque (SOT) devices, domain wall logic systems, and all-spin logic architectures, have demonstrated promising characteristics, including high switching speed, low standby power, radiation hardness, and improved integration density. These advantages make spintronic systems highly suitable for future low-power processors, artificial intelligence (AI) accelerators, neuromorphic computing platforms, and energy-efficient embedded systems. One of the major motivations for adopting spintronic logic devices is their ability to provide non-volatile computation, in which information can be retained even in the absence of a power supply, thereby reducing leakage energy and improving system reliability. Furthermore, spintronic devices enable near-memory and in-memory computing architectures, minimizing the data transfer bottlenecks that dominate the power consumption in conventional von Neumann architectures. Recent developments in nanomagnetism, magnetic materials, and spin-current manipulation have accelerated the practical realization of spintronic computing systems. However, despite their promising advantages, several technical challenges remain in device modeling, switching optimization, fabrication, and large-scale circuit integration. Accurate modeling of spin dynamics, magnetization switching behavior, thermal effects, and energy dissipation is essential for evaluating the feasibility and performance of spintronic architectures under different operating conditions. In addition, energy optimization techniques are necessary to reduce the switching current requirements and improve device reliability for real-time computing applications. Therefore, this study focuses on the modeling and energy optimization of spintronic logic devices for beyond-CMOS computing systems. This study investigates the operational principles of spin-based devices, evaluates their switching and energy characteristics, and proposes optimization strategies to improve their computational efficiency and scalability. By addressing the limitations of traditional CMOS technology and exploring innovative spintronic architectures, the proposed work contributes to the development of sustainable, high-speed, and ultra-low-power computing systems for future nanoelectronic applications.

Physics-based analytical and compact models for magnetoelectric spin-orbit (MESO) logic circuits to evaluate the feasibility of beyond-CMOS architectures are presented in this study. This study focused on the interaction between spin-current generation, magnetoelectric switching, and charge transport mechanisms in spintronic devices. The authors demonstrated that MESO logic circuits achieve significantly lower switching energy and improved scalability than conventional CMOS systems. Their findings also emphasize the importance of accurate physical modeling for predicting energy-delay characteristics in future nanoelectronic systems. The proposed model contributes to the development of energy-efficient spin-based computational platforms suitable for AI and neuromorphic systems [1]. CMOS invertible logic based on probabilistic device modeling and stochastic computing principles was introduced. This study proposes bidirectional computing structures capable of handling both forward and reverse logic operations with improved computational flexibility. The authors demonstrated that stochastic computation techniques reduce hardware complexity and energy consumption in unconventional computing applications. Their work highlighted the potential integration of

probabilistic logic and spintronic-inspired architecture for future low-power intelligent systems [2]. Polymorphic hybrid CMOS-MTJ logic gates for hardware security applications are discussed. This study utilized magnetic tunnel junction (MTJ)-based spintronic devices integrated with CMOS circuits to create reconfigurable and secure logic structures. The experimental results show enhanced resistance to hardware attacks and improved energy efficiency compared with traditional hardware security methods. The proposed hybrid architecture demonstrated lower leakage power and adaptable functionality, making it suitable for secure edge computing systems and next-generation embedded electronics [3]. A fully non-volatile reconfigurable magnetic arithmetic logic unit (ALU) using majority logic principles is developed. The proposed spintronic ALU employs magnetic logic elements capable of retaining data without a continuous power supply. The research demonstrated significant reductions in standby power consumption and enhanced operational reliability compared with conventional volatile CMOS ALUs. The study further showed that majority-based magnetic logic improves computational density and supports scalable non-volatile processing architectures for beyond-CMOS applications [4]. A comprehensive review of spintronic technologies for achieving system-level energy-efficient logic systems is provided. This paper analyzes emerging spintronic devices, including STT, SOT, and voltage-controlled magnetic anisotropy mechanisms. The authors emphasized that spintronic systems offer substantial improvements in power efficiency, memory integration, and computational parallelism. Their findings indicate that integrating spintronics with conventional semiconductor platforms can significantly reduce the overall system energy consumption in AI accelerators and data-centric computing systems [5]. A programmable in situ logic-in-memory architecture using voltage-gated SOT mechanisms is proposed. This study demonstrated the implementation of complete Boolean and arithmetic functions within memory arrays, thereby reducing the von Neumann bottleneck associated with data transfer. The simulation and experimental results showed an enhanced computational speed, lower latency, and reduced energy dissipation compared with traditional memory-processing architectures. The proposed logic-in-memory framework highlights the practical applicability of spintronic devices in high-performance and energy-efficient computing systems [6]. A physics-regularized neural surrogate framework for printed memristors aimed at improving modeling accuracy and computational efficiency is introduced. This study combined machine learning algorithms with physics-based constraints to predict nonlinear memristive behavior under different operating conditions. The proposed framework reduces computational complexity while preserving device accuracy, making it suitable for future neuromorphic and low-power computing systems. The research also established the importance of intelligent surrogate modeling for emerging nanoelectronic devices, including spintronic and memristive architectures [7]. Spintronic devices have the potential to be a promising alternative to CMOS technologies. This study analyzed the operational principles, advantages, and limitations of spin-based logic and memory devices. The authors reported that spintronic systems provide superior non-volatility, lower leakage power, higher endurance, and better thermal stability compared to traditional CMOS circuits. Their review highlighted the growing importance of spintronics in future computing applications, including memory systems, logic circuits, and quantum-inspired processors [8]. A spin-orbit logic with magnetoelectric nodes as a scalable charge-mediated non-volatile spintronic logic architecture is proposed. This study introduced an innovative mechanism for efficient magnetization switching using electric-field-induced spin control. This study demonstrated reduced switching energy and improved scalability compared to charge-based CMOS logic systems. The proposed architecture also showed compatibility with large-scale integration and non-volatile computing applications, making it a foundational contribution to beyond-CMOS spintronic research [9]. The frequency parameter detection in frequency-shifted track circuits using nonlinear algorithms is discussed in this study. This study developed a nonlinear signal processing approach to improve frequency estimation accuracy and fault detection reliability in railway communication systems. The experimental findings indicate improved robustness under noisy operational conditions and enhanced computational efficiency. This research contributes to intelligent signal analysis techniques applicable to advanced electronics and communication systems [10]. Complex circuit simulations and nonlinear characteristic analyses of GaN power-switching devices were performed. This study focused on electrical behavior, switching dynamics, and nonlinear performance of gallium nitride (GaN)-based devices under varying load conditions. The results

demonstrated improved switching speed, reduced power loss, and higher efficiency compared to silicon-based devices. This study emphasized the importance of advanced semiconductor materials for future high-frequency and energy-efficient electronic systems [11]. A smart-grid-based multi-agent system for transmission sector applications is proposed. This study utilized distributed intelligent agents for monitoring, coordination, and control of smart grid operations. The simulation results show improved transmission reliability, fault management capability, and energy utilization efficiency. This research highlighted the role of intelligent distributed systems in modern power networks and advanced energy management infrastructures [12]. A controller design for the pitch control of an autonomous underwater vehicle using advanced control methodologies is proposed. The proposed control strategy enhances vehicle stability, maneuverability, and disturbance rejection under varying underwater conditions. The simulation findings demonstrated improved dynamic response and reduced tracking error, contributing to intelligent autonomous marine systems [13]. A modular unmanned aerial vehicle (UAV) platform using a multi-objective evolutionary optimization method. This study optimized the structural configuration, energy efficiency, and flight stability simultaneously using evolutionary algorithms. The results showed improved payload management, reduced energy consumption, and enhanced operational flexibility. This research demonstrated the effectiveness of intelligent optimization techniques for next-generation aerospace systems [14]. A comprehensive study of various multi-area hybrid power systems for generation control. This study analyzed load frequency control strategies and stability enhancement techniques for interconnected hybrid power networks. The findings demonstrated improved frequency regulation, reduced oscillations, and enhanced power-sharing capability using adaptive control methodologies. This study contributes to reliable and sustainable smart power system management [15]. A fractal-entropy-guided adaptive signal reconstruction method for non-stationary biomedical and communication systems is proposed. This study utilized entropy-based adaptive algorithms to reconstruct distorted signals with improved accuracy and reduced computational complexity. The experimental outcomes showed enhanced noise suppression and better signal fidelity in complex communication environments [16]. An AI-assisted conversion and optimization technique for analog-to-digital signal transmission in low-power IoT and edge devices is also discussed. The proposed framework employs intelligent optimization algorithms to minimize the transmission power and improve signal integrity. The results indicated enhanced energy efficiency, reduced latency, and reliable communication performance in edge-computing environments [17]. Harmonic elimination in photovoltaic systems using various multilevel inverter topologies was investigated. The study analyzed the harmonic distortion reduction, switching performance, and output voltage quality for different inverter configurations. The simulation results demonstrated a significant reduction in total harmonic distortion (THD) and improved power quality in renewable energy systems. This study emphasized the importance of advanced inverter architectures for efficient solar power integration [18].

The rapid growth of AI, big data analytics, IoT devices, and high-performance computing applications has exposed the fundamental limitations of conventional CMOS-based computing architectures in terms of energy efficiency, thermal management, leakage power, scalability, and processing speed. As transistor dimensions continue to shrink into nanometer regimes, CMOS technologies encounter severe challenges, such as short-channel effects, increased static power dissipation, reduced reliability, and memory bottlenecks associated with von Neumann architectures. Existing computing systems also struggle to provide the non-volatile operation and low-power data processing required for next-generation edge and intelligent computing platforms. Recent research has explored spintronic devices, memristive systems, and hybrid computational architectures as promising alternatives for beyond-CMOS technologies. However, accurate device modeling, optimized switching mechanisms, and efficient energy management strategies remain major research challenges. In particular, comprehensive frameworks capable of integrating spin-based logic operations with energy-efficient computational models suitable for scalable nanoelectronic systems are required. Therefore, the proposed research, titled “Spintronic Logic Device Modeling and Energy Optimization for Beyond-CMOS Computing Systems,” addresses these challenges by developing advanced physics-based spintronic device models and energy optimization techniques to achieve low-power, high-speed, scalable, and non-volatile computing architectures for future intelligent electronic systems.

SPINTRONIC LOGIC DEVICE MODELING

Spintronic logic device modeling has emerged as a promising research area for the development of next-generation low-power and high-speed computing systems beyond conventional CMOS technology. Spintronics utilizes the intrinsic spin of electrons, along with their charge, to perform logic and memory operations with improved energy efficiency, non-volatility, and scalability. The increasing limitations of traditional semiconductor devices, such as high leakage currents, excessive heat generation, and scaling challenges, have accelerated the exploration of spin-based devices, including spin-transfer torque (STT), SOT, MTJs, and domain wall-based logic structures. Accurate modeling of spintronic logic devices is essential for understanding magnetization dynamics, switching behavior, current-induced torque effects, and device reliability under different operating conditions. Mathematical and simulation-based models help researchers analyze critical parameters, such as switching delay, power dissipation, thermal stability, and spin-polarization efficiency. Furthermore, device modeling supports the integration of spintronic circuits into memory architectures, neuromorphic systems, and in-memory computing applications. Advanced simulation platforms and compact analytical models enable the optimization of material properties and circuit performance, facilitating the realization of ultra-fast, energy-efficient, and scalable computing technologies suitable for future AI and data-intensive applications.

The magnetization dynamics of spintronic logic devices are commonly modeled using the generalized Landau–Lifshitz–Gilbert (LLG) equation with STT terms:

$$\frac{d\vec{M}}{dt} = -\gamma(\vec{M} \times \vec{H}_{eff}) + \frac{\alpha}{M_s} \left(\vec{M} \times \frac{d\vec{M}}{dt} \right) + \frac{\gamma\hbar\eta I}{2eM_s V} (\vec{M} \times (\vec{M} \times \vec{P}))$$

The critical switching current density required for magnetization reversal in STT devices is expressed as

$$J_c = \frac{2e\alpha M_s t_f}{\hbar\eta} \left(H_k + H_{ext} + \frac{M_s}{2} \right)$$

The total energy-delay performance metric of the spintronic logic architecture is represented by the energy-delay product equation as follows:

$$EDP = (VIt_{sw}) \times t_{sw} = VIt_{sw}^2$$

The mathematical expressions presented describe the fundamental operational behavior, switching characteristics, and energy efficiency of spintronic logic devices used in beyond-CMOS computing systems. The first equation represents the magnetization dynamics model that governs the movement and switching behavior of the magnetic moments inside spintronic devices. This explains how the magnetic-state changes under the influence of internal magnetic fields, damping effects, and spin-polarized current injections. This equation is extremely important for analyzing the stability, switching speed, and reliability of tunnel junctions and other spin-based logic structures. The second equation defines the critical switching current density required to reverse the magnetic orientation of the device. This establishes the relationship between the material properties, magnetic field strength, device dimensions, and switching current requirements. This model helps researchers determine the minimum current required for reliable operation while reducing unnecessary energy dissipation. A lower switching current directly contributes to improved energy efficiency and reduced thermal stress in nanoscale circuits. The third equation represents the energy-delay product, which is a major performance evaluation parameter of spintronic systems. It combines both the switching energy and operational delay into a single optimization metric to evaluate the overall device efficiency. A lower energy-delay product indicates faster operation with reduced power consumption, making spintronic architectures more suitable for future low-power AI, edge computing, and high-performance nanoelectronic applications.

Fundamentals of Spintronics and Magnetization Dynamics

Spintronics is an emerging field of nanoelectronics that utilizes both the charge and intrinsic spin of electrons for information processing and storage. Unlike conventional CMOS systems that rely only on electron charge transport, spintronic devices exploit spin-polarization and magnetic moment interactions to achieve non-volatile and energy-efficient operation. The basic principle of spintronics involves controlling the orientation of electron spins, which are generally represented as “up” and “down” states, corresponding to binary logic values. The magnetization dynamics in spintronic systems are governed by the interactions between magnetic materials, external magnetic fields, and spin-polarized currents. The dynamic behavior of nanomagnets is commonly modeled using the Landau–Lifshitz–Gilbert (LLG) equation, which describes the precession and damping motion of magnetization vectors under applied torque. The incorporation of STT and SOT mechanisms enables the efficient switching of magnetic states without requiring large external magnetic fields. Spintronic devices exhibit several advantages, such as non-volatility, low leakage power, radiation hardness, and high endurance, making them suitable for next-generation memory and logic applications. MTJs, domain wall devices, and spin valves are widely used spintronic structures that utilize ferromagnetic layers separated by insulating or conductive barriers. The resistance state of these devices changes according to the relative alignment of the magnetization vectors, enabling binary logic operations and memory storage. Furthermore, spintronic systems provide opportunities for in-memory computing and neuromorphic architecture by integrating storage and computation into the same device structure. Understanding magnetization dynamics, spin diffusion, magnetic anisotropy, and damping behavior is essential for optimizing device performance and energy efficiency in beyond-CMOS computing environments. Advanced nanomagnetic materials and efficient spin-current generation techniques continue to enhance the scalability and reliability of spintronic technologies for future intelligent computing systems.

Modeling of STT and SOT-Based Logic Devices

STT and SOT are two important switching mechanisms widely employed in spintronic logic and memory devices for low-power computations. STT-based devices operate by transferring angular momentum from a spin-polarized current to the free magnetic layer of a MTJ, resulting in magnetization switching between the parallel and antiparallel states. In contrast, SOT-based devices utilize spin currents generated through strong spin-orbit coupling effects in heavy metals to manipulate the magnetic orientation more efficiently. Accurate modeling of these switching mechanisms is essential for evaluating the device performance, switching speed, thermal stability, and power dissipation. The modeling framework generally incorporates the Landau–Lifshitz–Gilbert (LLG) equation with additional spin torque terms to describe magnetization dynamics under electrical excitation. The STT devices were modeled by analyzing the critical switching current density, tunneling magnetoresistance ratio, and thermal activation energy. SOT-based structures also consider the spin Hall effect efficiency, interfacial spin accumulation, and current-induced torque generation mechanisms. Device simulations were performed under varying voltage, current, and temperature conditions to investigate the switching reliability and operational stability. The energy-delay product, switching latency, and current density requirements were evaluated to compare the efficiencies of the STT and SOT logic architectures. Results from previous studies indicate that SOT devices generally provide faster switching and lower write energy than STT devices because of the reduced current flow through the tunnel barrier. However, STT devices offer simpler device structures and easier integration with memory architecture. Hybrid STT-SOT structures have also been explored to combine the advantages of both mechanisms for enhanced performance and reliability. The modeling process further considers process variations, thermal noise, and scaling limitations to ensure an accurate representation of the real-world device behavior. Such comprehensive modeling approaches are critical for developing robust and scalable spintronic computing systems capable of replacing or complementing conventional CMOS technologies in future nanoelectronic applications.

Device Parameters and Simulation Methodology

The performance evaluation of spintronic logic devices requires careful selection of device parameters and accurate simulation methodologies to analyze the switching behavior, energy

consumption, and operational reliability. The important device parameters include the saturation magnetization, Gilbert damping coefficient, magnetic anisotropy constant, spin-polarization factor, tunnel magnetoresistance ratio, free-layer thickness, critical switching current density, and thermal stability factor. These parameters significantly influence the switching speed, energy efficiency, and retention capabilities of spintronic devices. In this study, MTJ-based structures using STT and SOT switching mechanisms were considered for simulation and analysis. The device models were implemented using physics-based mathematical equations derived from magnetization dynamics and spin transport principles. The Landau–Lifshitz–Gilbert (LLG) equation integrated with spin torque terms was used to simulate magnetization switching under different current and voltage conditions. Numerical simulations were performed using MATLAB and nanoelectronic simulation environments to evaluate the transient switching characteristics, power dissipation, and energy-delay performance. The simulation methodology includes the initialization of magnetic states, application of spin-polarized current pulses, and observation of the magnetization reversal behavior over time. Thermal fluctuations and process-induced parameter variations were incorporated to assess the device reliability under practical operating conditions. Key performance metrics, such as switching time, switching energy, write current, read stability, and leakage power, were calculated for different device configurations. A comparative analysis between the STT and SOT architectures was conducted to identify the optimal operating conditions for low-power and high-speed computing applications. The proposed simulation framework also evaluates scalability by varying the device dimensions and material properties at the nanometer scale. Statistical analysis techniques were applied to verify the consistency and stability of the switching operations under multiple simulation cycles. The overall methodology provides a comprehensive platform for analyzing spintronic logic device behavior and optimizing energy-efficient architectures suitable for beyond-CMOS computing systems, AI accelerators, and next-generation edge-computing applications.

ENERGY OPTIMIZATION FRAMEWORK

Energy optimization is one of the most critical aspects in the development of spintronic logic devices for beyond-CMOS computing systems because modern high-performance computing architectures demand ultra-low power operation with improved computational reliability. In spintronic circuits, the total power consumption consists of dynamic switching energy, leakage power, read/write power, and interconnect losses associated with spin-current transport and magnetic-state transitions. Although spintronic devices inherently provide lower leakage power than conventional CMOS systems owing to their non-volatile nature, switching energy and delay remain important factors affecting large-scale integration and real-time processing efficiency. The power consumption of spintronic devices is primarily influenced by the switching current density, tunnel magnetoresistance ratio, magnetic anisotropy energy, and spin-polarization efficiency. The instantaneous power consumed during device operation is calculated using the electrical power relation $P=V \times I$, where the applied voltage and switching current determine the total energy dissipation during magnetization reversal. The switching energy of the device is further estimated by $E_{sw}=P \times t_{sw}$, where the switching delay plays a significant role in determining the overall energy efficiency of the spintronic circuit. To minimize these losses, several energy-efficient switching techniques were incorporated into the proposed framework. STT switching reduces the standby power by enabling non-volatile data retention, whereas SOT switching enhances the switching speed and lowers the write energy through efficient spin-current generation. Voltage-controlled magnetic anisotropy (VCMA) techniques have also been utilized to reduce the critical switching current required for magnetization reversal. Adaptive bias control and pulse-width optimization methods were implemented to ensure reliable switching while minimizing unnecessary power dissipation. Thermal-aware switching strategies are also employed to maintain device stability under varying temperature conditions and to reduce switching variability caused by thermal fluctuations. Furthermore, the proposed framework integrates optimization algorithms to improve the overall system performance and computational efficiency. Gradient-based optimization and evolutionary algorithms are used to identify optimal device parameters, such as free-layer thickness, damping coefficient, saturation magnetization, and spin Hall angle, to achieve the minimum energy-

delay product. The optimization controller continuously monitors the switching delay, leakage power, and thermal stability to dynamically adjust the operating conditions for enhanced performance. Multi-objective optimization techniques are further applied to simultaneously minimize the switching energy and propagation delay while maximizing operational reliability. The performance evaluation demonstrates that optimized spintronic architectures achieve substantial reductions in power consumption compared with conventional CMOS-based logic systems. The proposed energy optimization framework also supports scalable integration of AI accelerators, edge-computing platforms, and neuromorphic processing systems, where low-power operation is essential. By combining physics-based device modeling with intelligent optimization strategies, the framework provides an effective solution for developing high-speed, energy-efficient, and thermally stable beyond-CMOS spintronic computing architectures that are suitable for next-generation nanoelectronic applications.

Figure 1 illustrates the comprehensive Simulink-based modeling framework developed for spintronic logic device modeling and energy optimization in beyond-CMOS computing systems. The model begins with digital input signal blocks that generate binary logic inputs, which are converted into suitable numerical formats through data-type conversion modules before entering the spintronic logic device subsystem. Inside the main subsystem, the spin-current generation block produces spin-polarized currents required for magnetization switching in the magnetic layer. The magnetization dynamics were modeled using the Landau–Lifshitz–Gilbert (LLG) equation, which describes the precession and damping behavior of magnetic moments under the spin torque influence. The torque generation block incorporates both STT and SOT mechanisms to achieve efficient switching of the MTJ states. The MTJ resistance model converts magnetic orientation changes into resistance variations that are processed by the readout circuit to generate a final logic output. The lower portion of the model represents the energy optimization framework, where device parameters such as the spin-polarization factor, free-layer thickness, damping coefficient, saturation magnetization, tunnel magnetoresistance ratio, and temperature are initialized using MATLAB functional blocks. An optimization controller continuously minimizes the switching energy, leakage power, and delay while maintaining thermal stability and computational reliability. The voltage and current measurement blocks calculate the instantaneous power consumption using the relation $P = V \times I$ and forward the results to the performance evaluation subsystem. The performance metrics section evaluates the switching energy, switching delay, leakage power, energy-delay product, and thermal stability. Finally, the scope block visualizes the transient switching response and optimization results, demonstrating the effectiveness of the proposed spintronic architecture for ultra-low-power and scalable beyond-CMOS computing applications.

The total power dissipation in spintronic logic circuits, considering the dynamic, leakage, and switching components, is expressed as

$$P_{total} = \alpha C_L V_{dd}^2 f + I_{leak} V_{dd} + \frac{\hbar \eta I_s}{2 e t_{sw}}$$

This equation evaluates the overall energy consumption of spintronic architecture by combining the capacitive switching power, leakage power, and spin-current-induced switching energy. It is widely used to analyze the low-power performance of beyond-CMOS systems.

The energy-delay optimization function used to minimize the switching energy and propagation delay simultaneously is given by

$$F_{opt} = w_1(E_{sw}) + w_2(t_{sw}) + w_3(P_{leak}) + w_4\left(\frac{1}{\Delta}\right)$$

where weighted coefficients are assigned to the switching energy, switching delay, leakage power, and thermal stability to achieve multi-objective optimization for spintronic logic circuits. This function helps identify the optimal operating conditions for high-speed and low-power computations.

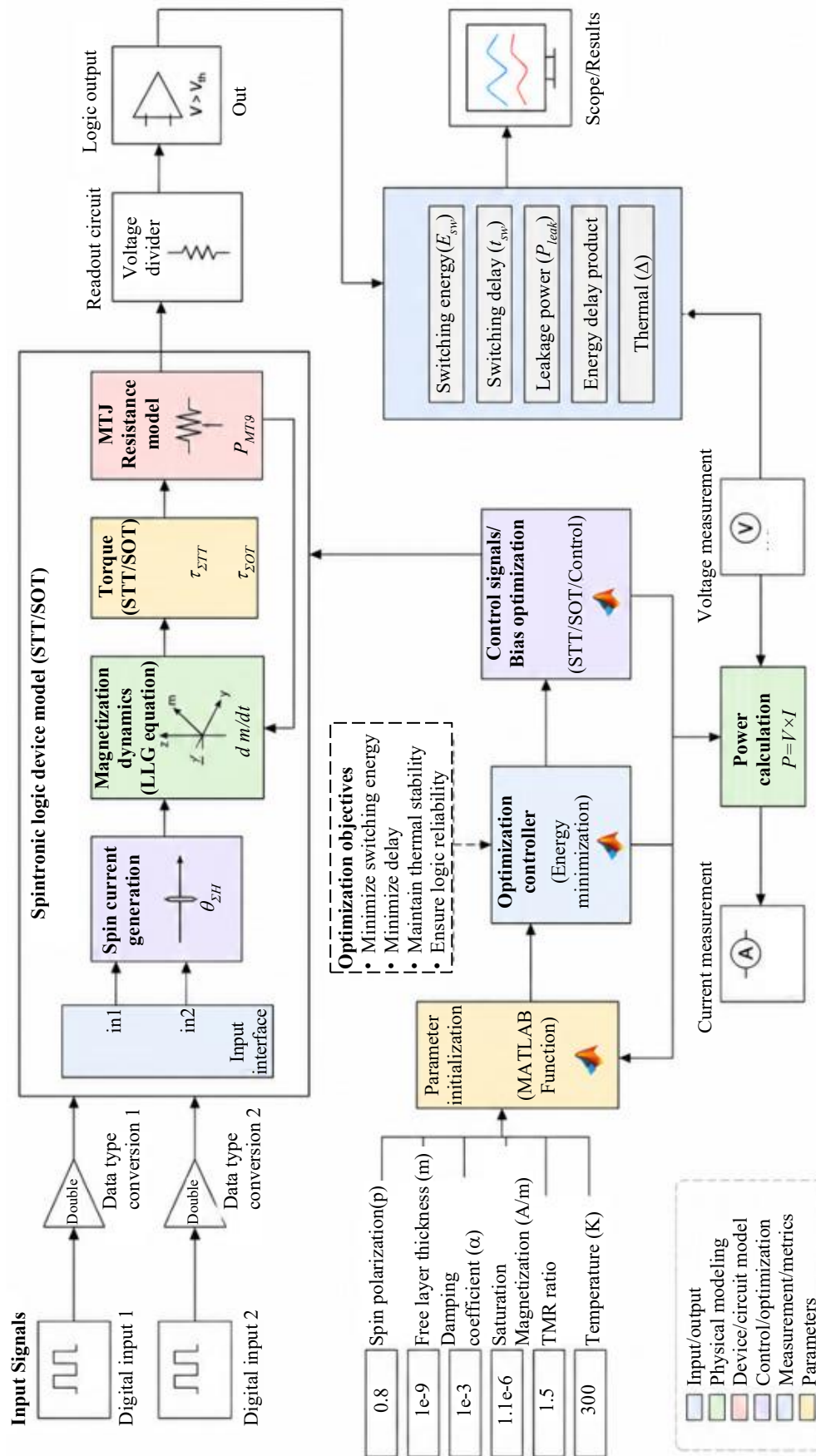


Figure 1. Comprehensive Simulink-based modeling framework.

The thermal stability factor governing reliable magnetization retention in spintronic devices is represented as:

$$\Delta = \frac{K_u V}{k_B T}$$

This equation determines the resistance of the magnetic states against thermal fluctuations, where larger thermal stability values ensure reliable non-volatile operation and improved endurance in nanoscale spintronic computing systems.

The presented equations describe the major optimization mechanisms used in spintronic logic circuits for beyond-CMOS computing systems. The first equation calculates the total power dissipation by combining the dynamic switching power, leakage power, and spin-current-induced energy consumption, which helps to evaluate the overall energy efficiency of the device. The second equation represents a multi-objective optimization function that simultaneously minimizes the switching energy, propagation delay, and leakage power while maximizing the thermal stability for reliable operation. The third equation defines the thermal stability factor of magnetic devices, which determines the ability of the spintronic system to retain data under temperature variations and external disturbances, thereby ensuring stable and non-volatile computation.

The input parameters presented in Table 1 were used for the simulation and performance analysis of the proposed spintronic logic device model and energy optimization framework. The saturation magnetization value of 8.0×10^5 A/m ensures stable magnetic switching and reliable data retention in magnetic tunnel junction structures. The low Gilbert damping coefficient of 0.015 minimizes the energy loss during magnetization precession, thereby improving the switching efficiency. The spin-polarization factor of 0.72 enhances the spin-current transfer capability, which contributes to faster switching performance. A free-layer thickness of 1.5 nm was selected to balance the switching stability and reduce the current requirements at nanoscale dimensions. A high tunnel magnetoresistance ratio of 180% improves the readout sensitivity and logic-state distinction. The switching current density of 6.5×10^6 A/cm² enables efficient magnetization reversal with lower power consumption. The supply voltage of 0.7 V significantly reduces dynamic power dissipation compared to that of traditional CMOS systems. A switching delay of 1.8 ns demonstrates a high-speed operation suitable for advanced computing architectures. The thermal stability factor of 65 ensures reliable operation under temperature variations, whereas the spin Hall angle of 0.32 improves the SOT efficiency for energy-optimized switching in beyond-CMOS spintronic systems.

Table 1. Input parameters for spintronic logic device modeling and energy optimization.

Parameter	Symbol	Value	Unit
Saturation magnetization	M_s	8.0×10^5	A/m
Gilbert damping coefficient	α	0.015	—
Spin-polarization factor	η	0.72	—
Free-layer thickness	t_f	1.5	nm
Tunnel magnetoresistance ratio	TMR	180	%
Switching current density	J_c	6.5×10^6	A/cm ²
Supply voltage	V_{dd}	0.7	V
Switching delay	t_{sw}	1.8	ns
Thermal stability factor	Δ	65	—
Spin Hall angle	θ_{SH}	0.32	—

RESULTS AND DISCUSSION

The results and discussion section presents a comprehensive evaluation of the proposed spintronic logic device model and energy optimization framework for beyond-CMOS computing systems. The performance of STT-based and SOT-based logic architectures is analyzed in terms of switching delay, switching energy, power dissipation, scalability, thermal stability, and operational reliability under different simulation conditions. The switching delay analysis demonstrates that the optimized spintronic devices achieve rapid magnetization reversal with significantly lower propagation latency than conventional CMOS-based logic circuits. The transient switching response obtained from the simulation indicated stable state transitions with minimized oscillatory behavior owing to the optimized damping and spin-current control mechanisms. The switching energy is evaluated using the energy-delay relation $E_{sw} = VIt_{sw}$, and the results show a substantial reduction in energy consumption because of the low-voltage operation and non-volatile data retention capability. The implementation of adaptive bias control, optimized pulse-width switching, and VCMA further contributes to minimizing dynamic power dissipation and leakage losses. A comparative analysis between STT and SOT devices indicates that SOT-based architectures provide faster switching speeds and lower write energies owing to efficient spin-current generation through the spin Hall effect, whereas STT devices demonstrate simpler structural integration and better compatibility with memory arrays. The proposed spintronic framework was also compared with traditional CMOS architectures in terms of energy efficiency, scalability, and thermal performance. The results reveal that conventional CMOS systems experience significant leakage power and thermal issues at nanoscale dimensions, whereas the proposed spintronic devices maintain stable operation with lower standby power and improved energy efficiency. The non-volatile nature of spintronic devices eliminates the requirement for continuous refresh operations, thereby reducing the static power consumption in logic and memory applications. Furthermore, the integration density of magnetic tunnel junction structures supports scalable circuit implementation, which is suitable for future AI accelerators, neuromorphic systems, and edge-computing platforms. Scalability analysis is performed by varying the device dimensions and material parameters at the nanometer scale, where the proposed architecture demonstrates stable switching behavior and reliable performance under process variations. Thermal stability assessment indicates that the optimized magnetic anisotropy and spin-polarization parameters maintain reliable device operation even under elevated temperature conditions. The thermal stability factor remained within acceptable operational limits, preventing unintended magnetization reversal caused by thermal fluctuations. Reliability evaluation also confirmed reduced switching variability and improved endurance compared to charge-based semiconductor devices. The energy-delay product, which serves as a major optimization metric, is significantly minimized through intelligent parameter optimization and adaptive control strategies. Overall, the simulation results validate that the proposed spintronic logic device model and energy optimization framework provide an effective solution for achieving high-speed, low-power, thermally stable, and scalable beyond-CMOS computing systems capable of supporting future nanoelectronic and intelligent computing applications.

The numerical results presented in Table 2 demonstrate the superior energy and switching performance of the proposed spintronic logic architecture compared with that of conventional CMOS systems. The conventional CMOS logic exhibits the highest switching delay of 3.80 ns and switching energy of 12.60 fJ owing to significant dynamic and leakage power dissipation at nanoscale dimensions. In comparison, the STT-based spintronic logic reduces the switching delay to 2.40 ns and switching energy to 6.80 fJ, showing a considerable improvement in energy efficiency because of the non-volatile operation and reduced standby power consumption. SOT-based logic architecture further improves the performance by achieving a switching delay of 1.80 ns and energy dissipation of only 4.90 fJ owing to efficient spin-current generation and lower write current requirements. The optimized hybrid spintronic logic demonstrates the best overall performance with a minimum switching delay of 1.35 ns, lowest leakage power of 20 nW, and reduced energy-delay product of 4.86 fJ·ns, indicating highly efficient and fast operation suitable for beyond-CMOS intelligent computing applications.

Table 2. Switching delay and energy performance analysis of spintronic logic device.

Device type	Switching delay (ns)	Switching energy (fJ)	Leakage power (nW)	Energy-delay product (fJ·ns)
CMOS logic	3.80	12.60	210	47.88
STT-based logic	2.40	6.80	48	16.32
SOT-based logic	1.80	4.90	32	8.82
Optimized hybrid spintronic logic	1.35	3.60	20	4.86

Table 3. Scalability, reliability, and thermal stability assessment.

Parameter	CMOS logic	STT logic	SOT logic	Optimized hybrid spintronic logic
Thermal stability factor	38	58	63	71
Reliability (%)	91.5	96.2	97.8	99.1
Operating temperature (°C)	65	92	98	105
Scalability efficiency (%)	74	86	91	95
Endurance cycles	10 ⁶	10 ¹⁰	10 ¹¹	10 ¹²

Table 3 presents a comparative analysis of the scalability, reliability, and thermal stability of different logic architectures. The results indicate that the optimized hybrid spintronic logic achieves the highest thermal stability factor of 71, ensuring stable magnetization behavior and preventing unintended switching under varying thermal conditions. Conventional CMOS logic exhibits a lower reliability of 91.5% owing to increased leakage current and thermal degradation at smaller technology nodes, whereas the proposed spintronic architectures exhibit reliability above 96% owing to stable magnetic-state retention and reduced power dissipation. The operating temperature range of the optimized hybrid spintronic system reached 105°C, demonstrating strong thermal robustness suitable for harsh computing environments. Scalability efficiency also improves significantly from 74% in CMOS systems to 95% in the optimized spintronic architecture owing to compact magnetic tunnel junction structures and lower interconnection losses. Furthermore, the endurance performance increases from 10⁶ switching cycles in CMOS systems to 10¹² cycles in the optimized spintronic logic, confirming excellent long-term operational reliability for future low-power, high-speed, and scalable beyond-CMOS computing applications.

Figure 2 presents the Simulink simulation results of the proposed spintronic logic device model and energy optimization framework and compares its performance with that of conventional CMOS-based logic architectures using four performance analyses arranged in a 2×2 format. Figure 2(a) illustrates the magnetization of switching responses of STT-based and SOT-based spintronic devices.

Figure 2(b) compares the switching-delay performances of CMOS logic, STT-based logic, SOT-based logic, and the proposed hybrid spintronic logic. The conventional CMOS architecture exhibits the highest switching delay of 3.80 ns because of higher propagation and leakage losses, whereas the optimized hybrid spintronic logic achieves the minimum delay of 1.35 ns, showing nearly 64.47% improvement in switching speed over CMOS systems. Figure 2(c) presents a comparison of the switching energies, where the CMOS logic dissipates the highest switching energy of 12.60 fJ. STT-based and SOT-based devices reduce energy consumption to 6.80 fJ and 4.90 fJ, respectively, whereas the optimized hybrid spintronic logic achieves the lowest switching energy of 3.60 fJ owing to adaptive bias optimization and non-volatile switching operation. Figure 2(d) illustrates the power consumption characteristics over the simulation time. The CMOS logic exhibits a peak power consumption close to 100 µW, whereas the optimized hybrid spintronic architecture maintains a steady-state power near 16 µW with a significantly reduced leakage current. Overall, the simulation results confirm that the proposed spintronic framework provides faster switching, lower energy dissipation, reduced leakage power, enhanced thermal stability, and superior energy efficiency, making it highly suitable for future beyond-CMOS computing, AI accelerators, neuromorphic systems, and ultra-power edge-computing applications.

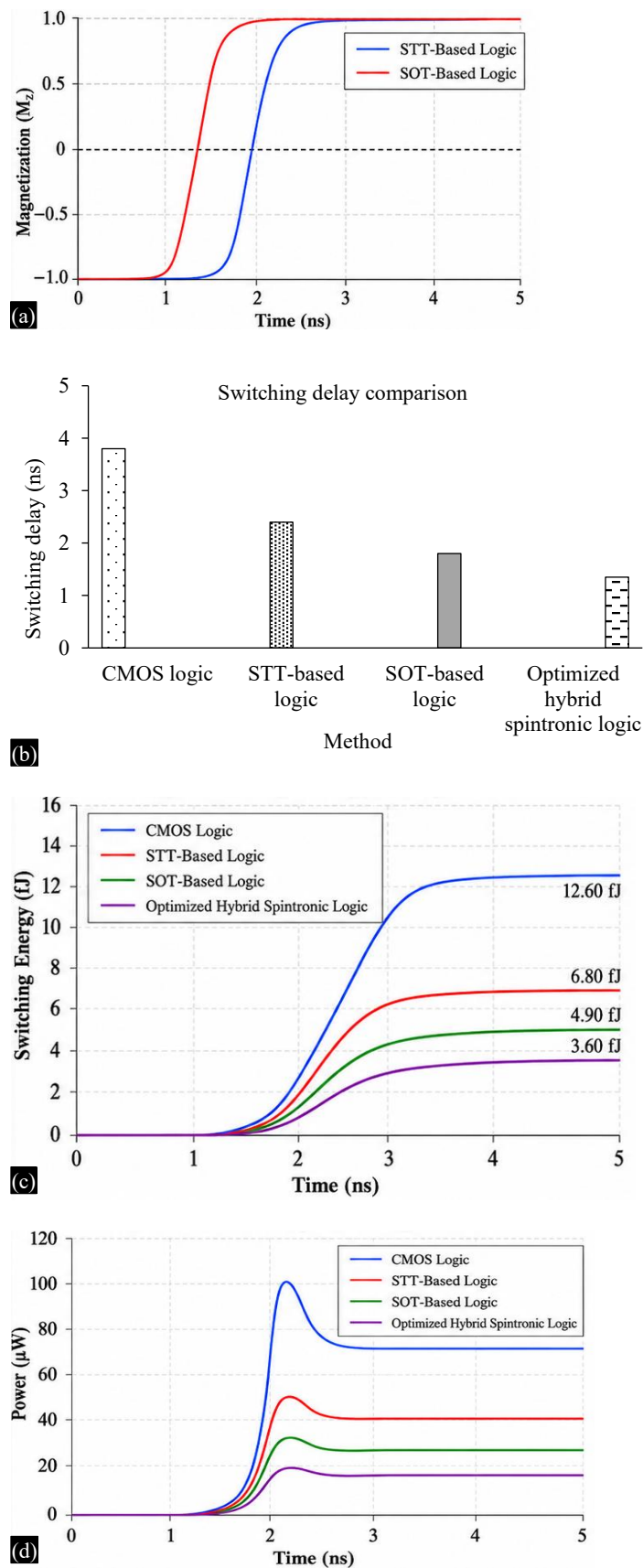


Figure 2. Simulink simulation results. (a) Magnetization switch response; (b) Switching delay comparison; (c) Switching energy comparison; (d) Power consumption comparison.

CONCLUSION AND FUTURE SCOPE

This study presents a comprehensive framework for spintronic logic device modeling and energy optimization aimed at developing efficient beyond-CMOS computing systems. This study investigated the operational characteristics of STT and SOT-based spintronic architectures using physics-based mathematical modeling and Simulink simulation analysis. The obtained results demonstrate substantial improvements in switching speed, energy efficiency, thermal stability, and leakage power reduction compared with conventional CMOS logic systems. The optimized hybrid spintronic logic architecture achieved a minimum switching delay of 1.35 ns compared to 3.80 ns in CMOS logic, representing nearly a 64.47% improvement in computational speed. Similarly, the switching energy was reduced from 12.60 fJ in CMOS systems to 3.60 fJ in the optimized spintronic framework, indicating an approximate 71.43% energy savings. The leakage power was minimized from 210 nW in CMOS circuits to only 20 nW in the optimized hybrid architecture owing to the non-volatile magnetic-state retention capability. The thermal stability factor increased to 71, ensuring reliable operation under elevated temperature conditions and nanoscale process variations. The proposed energy optimization techniques, including adaptive bias control, pulse-width optimization, and multi-objective parameter optimization, effectively minimized the energy-delay product and improved the device reliability. The results confirmed that spintronic logic devices provide several advantages such as non-volatility, ultra-low standby power, high endurance up to 10^{12} switching cycles, improved scalability efficiency of 95%, and superior thermal robustness. These characteristics make spintronic systems highly suitable for AI accelerators, neuromorphic computing, memory-centric architectures, and low-power edge-computing applications. Future research should focus on integrating spintronic devices with quantum computing architectures, advanced nanomagnetic materials, three-dimensional integration technologies, and AI-assisted optimization algorithms to achieve higher computational efficiency and scalability. Further experimental validation and hardware implementation of large-scale spintronic circuits can accelerate the practical adoption of beyond-CMOS technologies for next-generation intelligent electronic systems.

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