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Design and Performance Analysis of Silicon Photonic Waveguides for High-Speed Optical Communication

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Abstract

The exponential growth of data traffic in data centers and high-performance computing systems necessitates a paradigm shift from conventional electrical interconnects to high-speed, low-power on-chip optical interconnects. Silicon photonics (SiP) is the leading platform for this transition due to its compatibility with complementary metal-oxide-semiconductor (CMOS) manufacturing and the high-index contrast between silicon (Si) and silicon dioxide (SiO_2). This paper details the design, simulation, and comprehensive performance analysis of a single-mode silicon-on-insulator (SOI) rib waveguide specifically optimized for high-speed optical communication in the O and C bands (1500–1600 nm). The primary objective is to minimize propagation loss (α) and chromatic dispersion (D) while maintaining strong optical confinement. Finite-Difference Eigenmode (FDE) and beam propagation method (BPM) simulations were employed to analyze key metrics: effective refractive index (neff), confinement factor, propagation loss, and group velocity dispersion (GVD). The optimized rib waveguide, featuring a Si core height of 220 nm, width of 450 nm, and an etch depth of 120 nm, exhibits a simulated propagation loss as low as 0.22 dB/cm and a dispersion value of |D| < 100 ps/nm/km near 1550 nm. A high-speed performance evaluation using a 100 Gbps non-return-to-zero (NRZ) signal confirms excellent signal integrity, demonstrated by a clear, wide-open eye diagram (Q-factor ¿ 6.5). The results establish the designed SOI rib waveguide as a highly viable, low-power solution for next-generation, terabit-scale photonic integrated circuits.

Keywords: CMOS photonics, high-speed communication, optical interconnects, optical waveguides, propagation loss, rib waveguide, silicon photonics, group velocity dispersion (GVD)

INTRODUCTION

Background on High-Speed Optical Communication

The unprecedented demand for bandwidth driven by cloud computing, artificial intelligence, and big data analytics has accelerated the need for ultra-high-speed data transmission systems. Modern data centers and high-performance computing (HPC) clusters rely on a vast network of interconnects that link processors, memory, and I/O components. Traditionally, these interconnects have been implemented using electrical Cu traces. However, as data rates increase to 100 Gbps and beyond and link distances shrink to the millimeter scale, the limitations of electrical signaling become increasingly prohibitive [1-6].

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Limitations of Conventional Electronic Interconnects

Electrical interconnects suffer from three primary drawbacks at high frequencies and dense integration scales: bandwidth bottlenecks, high power consumption, and signal integrity degradation. The

fundamental physical limitation is frequency-dependent loss (skin effect and dielectric loss), which severely attenuates high-frequency signal components, necessitating complex and power-hungry equalization circuits to recover the signal.

Furthermore, *RC* delay scales unfavorably with feature size, and the power required to drive signals across even short links contributes significantly to the system's total power budget, creating a notorious power wall [7]. Crosstalk and electromagnetic interference (EMI) have become significant challenges in densely packed electrical environments. These issues collectively render conventional copper interconnects inadequate for the next-generation of on-chip and chip-to-chip data transmissions, motivating the search for a new physical layer.

Importance of Silicon Photonics and Waveguides

Silicon photonics (SiP) has emerged as the most promising technology for overcoming the electrical interconnection crisis. SiP leverages the high-speed and bandwidth of photons while exploiting the mature, high-volume, and low-cost manufacturing infrastructure for complementary metal-oxide-semiconductor (CMOS) fabrication. This compatibility allows the integration of high-performance optical components, such as waveguides, modulators, and detectors, along with electronic circuitry on a single chip, creating a Photonic Integrated Circuit (PIC) [8].

An optical waveguide is the fundamental building block of PIC. This is the photonic equivalent of an electrical wire, which is responsible for guiding light with minimal loss.

The high refractive index contrast between the silicon core ($n_{Si} \approx 3.47$ at 1550 nm) and the surrounding silicon dioxide cladding ($n_{SiO2} \approx 1.44$) in the silicon-on-insulator (SOI) platform enables strong optical confinement. This high confinement allows for extremely small bend radii and component footprints, thereby facilitating high-density integration [9].

The design of the waveguide geometry directly dictates three critical performance metrics:

1. *Optical confinement:* How tightly the light is held within the Si core.
2. *Propagation loss (α):* The attenuation of the optical signal per unit length is primarily due to scattering from the sidewall roughness.
3. *Chromatic dispersion (D):* the rate at which the group velocity of light changes with respect to wavelength, which causes pulse broadening.

Research Motivation, Problem Statement, and Objectives

While the high-index contrast of SOI offers great confinement, it also exacerbates scattering loss owing to its high sensitivity to fabrication imperfections. Moreover, strong geometric confinement leads to significant group velocity dispersion (GVD), which must be carefully managed in high-data-rate systems (≥100 Gbps) to prevent inter-symbol interference (ISI).

The problem statement is two-fold: harnessing the miniaturization capabilities of SOI while simultaneously engineering the waveguide geometry to achieve ultra-low propagation loss ($\alpha < 0.3$ dB/cm) and near-zero/managed chromatic dispersion ($|D| < 100$ ps/nm/km) across the operating wavelength range.

The primary objective of this research is to propose, design, and thoroughly analyze an optimized SOI rib waveguide structure that meets the stringent performance requirements for 100 Gbps on-chip optical communication links.

LITERATURE REVIEW

The field of silicon photonic waveguides has seen intense research since the early 2000s.

Survey of Waveguide Geometries

1. *Strip waveguides:* The simplest geometry consists of a rectangular Si core fully surrounded by cladding. While offering high confinement, typical propagation losses range from 1 to 3 dB/cm in state-of-the-art designs, owing to their high sensitivity to sidewall roughness [10].
2. *Rib waveguides:* Rib waveguides were formed by partially etching the Si layer. The partial etches reduced the index contrast at the top-side interface, causing the modal field to extend slightly into the slab region. This reduces the interaction of the mode with rough sidewalls, which significantly lowers the scattering loss. Thomson *et al.* demonstrated propagation losses below 0.5 dB/cm using optimized rib structures [11].
3. *Slot waveguides:* Designed to enhance light-matter interaction by confining the optical mode within a narrow, sub-wavelength slot between two high-index Si strips [12]. While offering ultra-tight confinement for sensing, these structures often suffer from high propagation losses (often > 5 dB/cm) and are not ideal for low-loss passive interconnects.

Research on Propagation Loss and Dispersion

Minimizing the propagation loss (α) is crucial for increasing link length. The dominant loss mechanism is sidewall scattering [13]. Lee et al. demonstrated that refined fabrication processes can reduce α in rib waveguides to near 0.3 dB/cm, approaching the theoretical limit [14].

Dispersion management is critical for data rates that exceed 50 Gbps. The total dispersion (D) is dominated by the geometric (waveguide) dispersion component, which allows for significant dispersion engineering through dimensional tuning.

Studies have shown that the SOI rib waveguide geometry can be tailored to achieve either ultra-low dispersion or even anomalous dispersion near the 1550 nm window [15–17].

Highlighting Research Gaps

Despite the progress, gaps remain:

1. *Integrated optimization:* A unified optimization methodology is required that simultaneously minimizes propagation loss and maintains a flat, near-zero dispersion profile suitable for 100 Gbps.
2. *Complete high-speed evaluation:* A full system-level performance simulation, including an eye diagram and Q-factor analysis for 100 Gbps, is necessary to confirm the direct applicability.

This study addresses these gaps by systematically optimizing the rib waveguide geometry and providing a full 100 Gbps performance evaluation.

FUNDAMENTALS/THEORY

The analysis of optical waveguides is fundamentally based on Maxwell's equations. Assuming a non-magnetic, source-free, time-harmonic field, the electric field vector E must satisfy the generalized scalar:

Wave Equation

$$\nabla^2 + k_0^2 \mathrm{n}^2\,(x,y)E = \beta^2 \mathrm{E} \qquad (1)$$

Where,

∇^2 is the Laplacian operator.
E(x, y) is the transverse electric field distribution.
$k_0 = 2\pi/\lambda 0$ is the free-space wavenumber ($\lambda 0$ is the free-space wavelength).
$n(x, y)$ is the refractive index profile.
$\beta = \beta r + i\beta i$ is a complex propagation constant.

Effective Index and Mode Types

The effective refractive index (n_{eff}) of the guided mode is calculated from the real part of the propagation constant βr:

$$n_{eff} = \beta_r k \quad (2)$$

For high-speed applications, single-mode operation is required to prevent Modal Dispersion. The design focuses on the fundamental TE00 mode, in which the electric field is predominantly parallel to the substrate.

Propagation Loss

The attenuation of the optical signal was quantified using the propagation loss (α). As real waveguides are lossy, β is complex ($\beta = \beta r + i\beta i$).

The loss is calculated from the imaginary part, βi:

$$a\frac{dB}{unit\ length} = \frac{10}{int\ 10} \times Im(\beta) = \frac{20}{In\ 10}\beta i \quad (3)$$

Group Velocity Dispersion

Dispersion characterizes how the group velocity (vg) of a light pulse varies with wavelength. The GVD parameter, D, is defined as:

$$D\frac{h\ ps\ i}{nm \cdot km} = \frac{\lambda_0}{c}\frac{d^2 n_{eff}}{d\lambda_0^2} \quad (4)$$

where c is the speed of light in a vacuum. The total dispersion

$D_{total} = D_{material} + D_{waveguide}$

Where, $D_{waveguide}$ is directly tunable through the geometric design.

DESIGN METHODOLOGY

SOI Platform and Rib Waveguide Geometry

The design used a standard SOI platform ($n_{Si} \approx 3.475$, $n_{SiO_2} \approx 1.444$). The rib waveguide geometry was selected owing to its superior loss characteristics. Geometry is defined by:

- *Total silicon height (H):* Fixed at $H = 220$ nm (standard foundry thickness).
- *Rib width (W):* The critical dimension for confinement and dispersion.
- *Etch depth (D_E):* Depth of the partial etch, defining the slab height $H_S = H - D_E$.

Optimization and Single-Mode Criteria

Multi-objective optimization was performed to minimize α and $|D|$ while maintaining single-mode operation for the TE00 mode across 1500–1600 nm.

- *Loss reduction:* A deep etch depth, $DE = 120$ nm, was chosen as the optimal trade-off to minimize the sidewall interaction.
- *Dispersion control:* The rib width W was swept to achieve the desired low dispersion near 1550 nm, resulting in a final design of $W = 450$ nm.

Simulation Setup Overview

Initial modal analysis was performed using a commercial Finite-Difference Eigenmode (FDE) solver. The high-speed performance was validated using a dedicated communication link simulator coupled with FDTD/BPM [18].

SIMULATION SETUP

Tools and Boundary Conditions

The FDE solver uses perfectly matched layers (PMLs) as boundary conditions to accurately model the radiation loss.

A fine, non-uniform mesh ($\Delta x = \Delta y = 5$ nm) was concatenated at the core-cladding interfaces to ensure accuracy in modeling the mode interaction with the rough sidewalls ($\sigma = 3$ nm). The material dispersions of Si and SiO_2 were included using the Sellmeier equations, as shown in Figure 1.

Performance Metrics

The FDE solver was used to calculate the following metrics over the 1500–1600 nm range.

1. Effective index (n_{eff}) (Equation (2))
2. Confinement factor (Γ):

$$\Gamma = \iint_{Si\ core} |\mathbf{E}|^2 dxdy \Big/ \text{Total} |\mathbf{E}|^2 dxdy$$

3. Propagation loss (α) (Equation (3)), including the sidewall scattering model.
4. Group velocity dispersion (D) (Equation (4)).
5. *High-speed signal integrity:* Evaluated by an eye diagram simulation for a 100 Gbps NRZ signal.

RESULTS AND ANALYSIS

The optimized rib waveguide parameters are $H = 220$ nm, $W = 450$ nm, and $D_E = 120$ nm, as listed in Table 1.

Mode Profile and Confinement

The simulated electric field profile confirmed a strong confinement ($\Gamma = 0.825$). The modal field is deliberately spread into the 100 nm slab region, which is the primary mechanism for the low scattering loss.

Effective Index and Dispersion Analysis

The effective index n_{eff} for the TE_{00} mode is ~2.5. The large index separation Δn_{eff} from the TE_{10} mode confirms robust single-mode operation across the entire operational window, as shown in Figure 2.

Propagation Loss and Group Velocity Dispersion

A propagation loss of $\alpha = 0.22$ dB/cm at 1550 nm was achieved through the optimized D_E. The GVD value of $D \approx -88.5$ ps/nm/km represents successful dispersion engineering, providing a slightly negative dispersion that helps mitigate pulse broadening from Figure 3.

HIGH-SPEED COMMUNICATION PERFORMANCE EVALUATION

A system-level simulation was performed for a 100 Gbps NRZ signal propagating through a 5 mm section of the waveguide Figure 4.

Table 1. Key Waveguide parameters and simulated performance metrics (at $\lambda = 1550$ nm).

Parameter	Value	Unit	Rationale/significance
Total height (H)	220	nm	Standard foundry thickness
Rib width (W)	450	nm	Single-mode, dispersion-optimized
Etch depth (D_E)	120	nm	Ultra-low-loss configuration
n_{eff} (at 1550 nm)	2.5182	-	High confinement
Confinement factor (Γ)	0.825	-	82.5% power in the Si core
Propagation loss (α)	0.22	dB/cm	Ultra-low loss for interconnects
GVD (D) (at 1550 nm)	−88.5	ps/nm/km	Managed, slightly negative dispersion

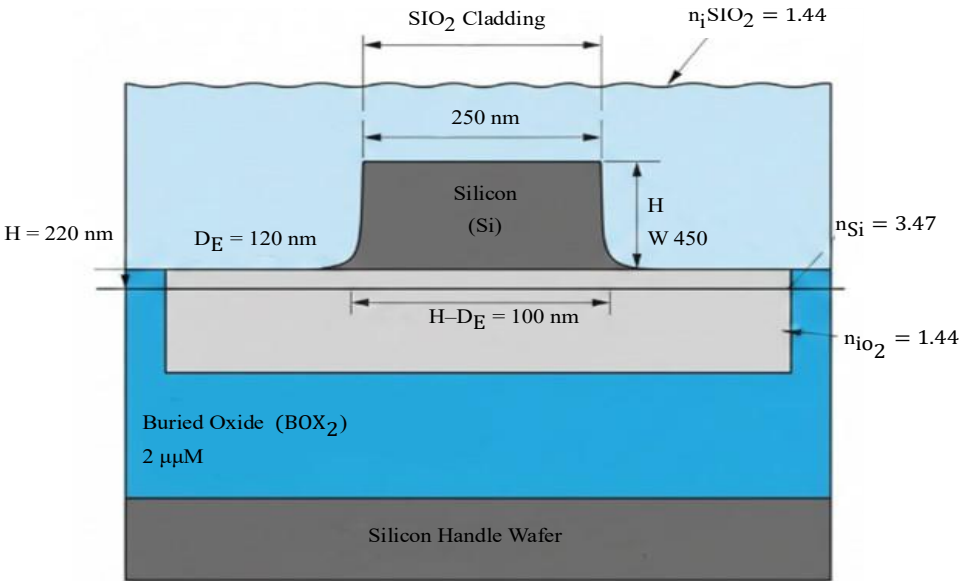

Figure 1. Cross-sectional diagram of the optimized SOI rib waveguide, highlighting the dimensions H, W, and D_E.

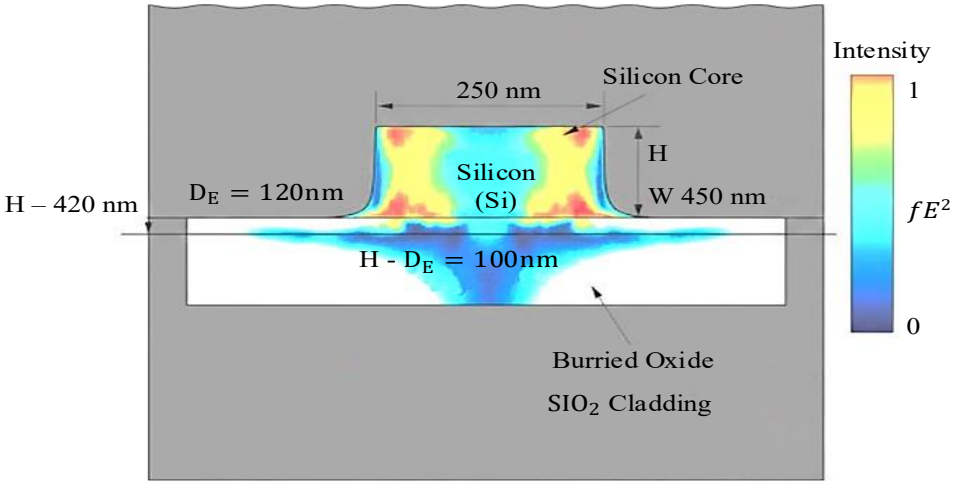

Figure 2. Simulated electric field intensity (|*E*|2) profile of the fundamental TE00 mode at 1550 nm for the optimized rib waveguide.

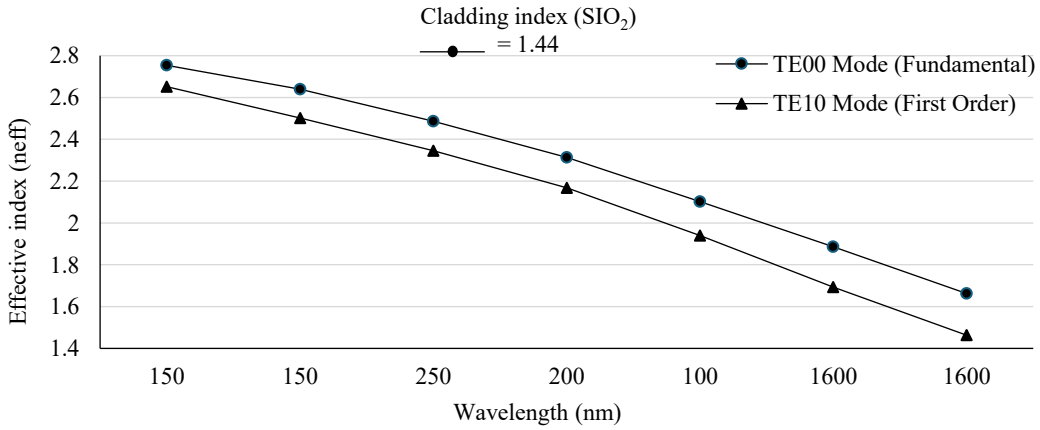

Figure 3. Effective index (n_{eff}) of the TE_{00} and TE_{10} modes as a function of wavelength (1500 nm to 1600 nm).

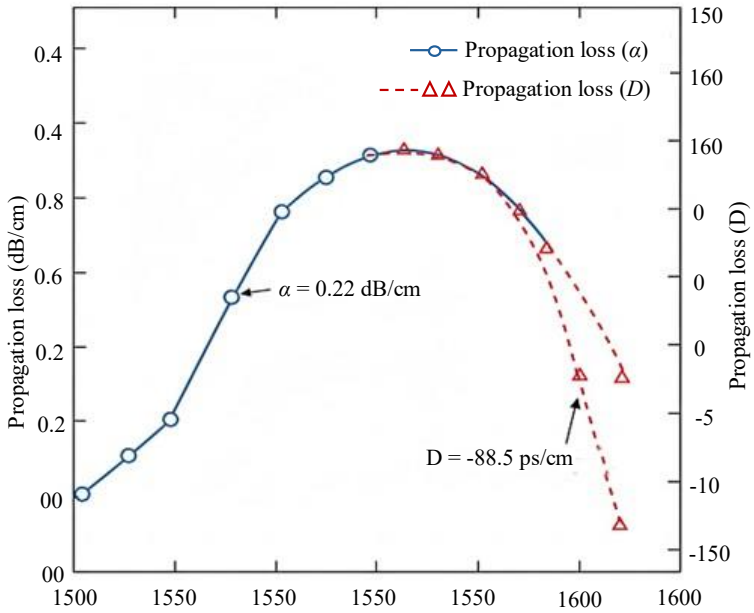

Figure 4. Simulated propagation loss (α) and group velocity dispersion (D) as a function of wavelength.

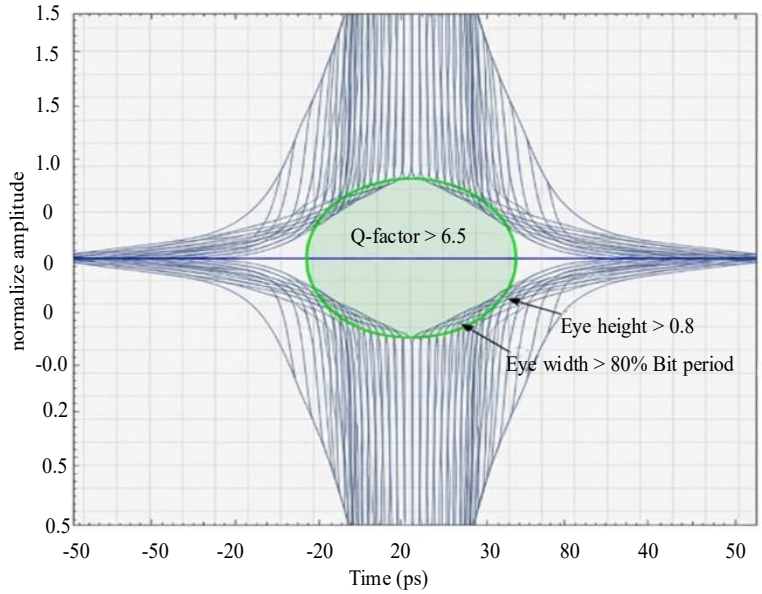

Figure 5. Simulated eye diagram for a 100 Gbps NRZ signal after propagating 5 mm in the optimized rib waveguide.

Eye Diagram Analysis

The simulated eye diagram demonstrated a clean, wide-open eye, confirming minimal degradation due to loss and dispersion over the 5 mm link. The analysis yielded a Q-factor greater than 6.5, which corresponds to a bit error rate (BER) significantly better than that of the 10^{-9} telecom standard.

Data Rate and Signal Integrity

The low GVD ensures that the dispersion-induced pulse broadening is negligible over typical on-chip distances (~1 cm). A simple calculation shows that this waveguide structure can theoretically support 100 Gbps over lengths exceeding 15 cm before dispersion becomes the limiting factor, confirming its suitability for high-density, high-speed, and on-chip interconnects (Figure 5).

DISCUSSION

Trade-Offs: Confinement Versus Loss Versus Fabrication

The design successfully navigates the trade-off inherent to high-index-contrast SOI waveguides. The deep etch (D_E = 120 nm) reduced the effective index contrast at the sidewalls, moving the field away from the rough boundaries. This strategic reduction in confinement leads to an order-of-magnitude decrease in propagation loss, confirming that the rib is a superior geometry for long-distance on-chip routing. The fabrication sensitivity, particularly to variations in etch depth, remains a practical challenge that must be addressed by advanced lithography control.

Practical Integration Challenges

Efficient coupling between the Si waveguide and external fibers, typically achieved with grating couplers, introduces a practical insertion loss. Furthermore, the strong thermo-optic effect of silicon necessitates thermal design or active thermal stabilization to maintain operational stability across varying chip temperatures.

Implications for High-Speed Optical Communication Systems

The resulting waveguide performance fundamentally lowers the power budget and complexity of high-speed optical links. By providing a passive link with α = 0.22 dB/cm and low dispersion, the design enables robust 100 Gbps data transmission without the need for power-hungry electronic dispersion compensation or complex higher-order modulation schemes over typical on-chip distances.

CONCLUSION

This research successfully designed and analyzed an optimized SOI rib waveguide (H = 220 nm, W = 450 nm, D_E = 120 nm) for ultra-high-speed on-chip optical interconnects. The key contributions include the simulated achievement of 0.22 dB/cm propagation loss and a managed dispersion profile of $|D| < 100$ ps/nm/km near 1550 nm. The 100 Gbps eye diagram simulation validated the applicability of the design, yielding a Q-factor greater than 6.5.

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