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Performance Comparison of Noise-Tolerant, High-Performance CMOS Domino Logic Configurations

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Abstract

In high-performance VLSI chip design, domino logic configuration is often preferred over static logic due to its faster operation and smaller area footprint, especially in deep submicron (DSM) technology. However, DSM noise has become a significant challenge in domino-based circuits, leading to compromises in the reliability and signal integrity of integrated circuits (ICs). The switching threshold of domino logic, defined as the input voltage level at which the gate output changes state, is typically determined by the NMOS transistor threshold voltage (Vt). Consequently, domino logic exhibits poor noise tolerance, making it a critical vulnerability in high-performance VLSI design. Additionally, high dynamic power dissipation remains a major drawback of domino circuits. Despite these limitations, wide fan-in domino logic remains widely used in applications such as microprocessors, digital signal processors (DSPs), and dynamic memory systems. However, as the fan-in increases, the delay performance of the circuit tends to degrade significantly. Over the past two decades, several domino-based design techniques have been proposed to address these weaknesses. While these approaches have successfully improved noise tolerance, they often come at the expense of other critical design metrics such as power consumption, delay, or silicon area. As a result, there is a growing demand for noise-tolerant domino techniques that introduce minimal overhead in key design parameters, particularly in today's DSM technology. In this study, two novel techniques are presented: 1) One technique enhances noise immunity and optimizes the noise immunity vs. power and delay trade-off for wide fan-in circuit configurations. 2) The other technique improves noise tolerance while achieving better delay performance in wide fan-in domino logic. Key findings include: Wide Fan-in (AND8): The Novel technique excels in both ANTE/Power and ANTE/Delay metrics; Small Fan-in (AND2): Bobba's technique demonstrates significant superiority in ANTE/Power; and ANTE/Delay metrics and Width Adjustment (WMN): Increasing transistor width enhances ANTE, but at the cost of higher power consumption and increased delay in the Novel technique. This research offers a balanced approach to overcoming the challenges associated with domino logic in high-performance VLSI circuits.

Keywords: CMOS, SSRS, RSMRD, Domino logic, PDN, RSDLS, DSM, BSIM4

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INTRODUCTION

Domino logic configuration is preferred in the design of high-performance VLSI chip especially in wide fan-in circuits against static configuration, which is slower and occupies larger area in deep submicron technology. Deep submicron noise has emerged as a critical issue in high performance ICs using domino implementation. This in turn asks for a compromise in reliability and integrity of the chip [1–4].

Switching threshold of logic is the input voltage at which gate output changes state. This voltage of

static CMOS logic is typically around half the supply voltage ($V_{DD}/2$). In domino logic configuration, it is usually transistor threshold voltage V_t (20 to 30% of V_{DD}). Therefore, a domino logic gate is having poor noise tolerance as compared to static logic gate and considered as a weak link in high performance VLSI chip [5, 6] design in the current submicron technologies (i.e., 65 nm, 90 nm etc.) [7–9].

Domino circuit configuration also suffers from higher dynamic power dissipation because of mainly two reasons. (i) rail-rail switching (V_{swing}) is formed at internal (dynamic) node [8]. (ii) For any random input, usually two transitions take place (pre-charge and evaluation) at the internal node in domino logic, while in static logic, such transitions are absent at the internal node.

A number of domino-based design techniques have been proposed in the last two decades in order to strengthen the above-mentioned weak link [5, 10]. For example, Bobba's technique [11], which increases the noise immunity by raising V_{th} by pre-charging the internal node, Mendoza technique [10] and Proposed technique [6], which increase the noise immunity by controlling the evaluation period and pre-charging the internal node. However, such techniques enhance the noise tolerance but at the significant cost in terms of one or more important design metrics (overhead) like power consumption, delay or silicon area. Hence, the noise tolerance domino techniques with only little overhead in silicon area, power consumption and speed are extremely desired in today's deep submicron (DSM) technology.

In this study, we propose a novel technique which not only enhances noise tolerance of domino logic but incur only minor overhead in design metrics as compared to above mentioned techniques by pre-charging the internal node as well as controlling the evaluation period. For validation, we compare the performance of the technique with the above-mentioned techniques in terms of various trade-offs like Noise immunity (ANTE) vs. Power consumption, Noise immunity vs. delay and Noise immunity vs. area trade-off. Performance comparison is presented by considering 2i/p AND gate as a digital bench mark circuit. The results are confirmed in 90 nm technology.

Organization of the paper is as follows: Next, we discuss in brief the related work. After that, we describe the environment adopted for our simulation-based experiments. Implementation of circuit configuration is discussed later. *W*e also discuss here simulation results of the techniques. Lastly, the simulation results are analyzed in order to compare the performance of novel technique with other techniques considered in this study.

RELATED WORK

Noise in Dynamic (Domino) Circuits

Deep submicron noise degrades the domino circuits' performance and produces the erroneous result which are classified under two major categories: (i) pre-charging noise; and (ii) external noise. Pre-charging noise occurs due to primarily charge sharing [12] and leakage noise [13–16]. Charge sharing noise is caused by charge redistribution between the dynamic node of domino logic and the internal nodes of PDN. Redistribution causes degradation in the voltage level at the dynamic node and subsequently erroneous result may be produced by domino logic gate [17–19]. Leakage noise refers to the possible charge loss in the evaluation phase due to flow of sub-threshold leakage current from the off PDN transistors. Since leakage current increases exponentially with respect to transistor threshold voltage, which is continuously scaled down as per reduction in the power supply voltage. Hence, leakage current is a significant source of noise in wide fan-in domino logic gates. External noise (i/p noise) is the noise presented at the inputs of domino gates. They are primarily caused by coupling effect i.e. crosstalk among adjacent signal wires.

If some precautionary actions are not taken against these noises, then they can significantly reduce the reliability and signal integrity of the dynamic circuits. In this study we have considered the impact of external noise and pre-charging noise as a major noise source.

Noise Tolerant Domino Techniques

Raising the noise threshold voltage V_{th} of the transistor and controlling the evaluation period using delayed clock are reported as the effective ways to enhance the noise tolerance of domino gates [6]. Noise tolerant domino techniques based upon the above approaches were reported in literatures [10, 11]. Implementation of 2i/p AND gate using twin-transistor technique [5] is as shown in Figure 1 that each N-logic transistor of PDN requires additional pre-charge transistor (MTT) [1]. MTT increases the noise threshold voltage of N-logic due to body-effect.

Subsequently, noise tolerance of the gate improves. Though, for wide fan-in (AND logic) use of such technique is not preferable as it requires one extra transistor per N-logic (Area penalty). Other significant drawback of the technique is that using gate inputs to raise the voltage of the N-logic internal nodes increases load capacitance of the gate input drivers which slow down the switching of the gates (delay penalty). Further, this technique is not suitable for certain logic functions because it may short circuit input nodes [20]. Bobba's technique also increases the noise immunity by pre-charging the internal node which is as discussed below.

Implementation of AND2 using Bobba's technique is shown in Figure 2 [11]. The technique uses one extra nMOS transistor and pMOS transistor in the N-logic per NMOS transistor in the pull-down network. The pMOS transistors are used to pre-charge the internal node (p1 &p2) up to V_{DD} in the pre-charge phase. Due to voltage at the intermediate node increases, V_{SB} increases at each node and subsequently Vth increases as per the following Eq. (1).

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{|2\emptyset_F|}\right) \quad (1)$$

Since the technique requires two additional transistors per transistor in N-logic, power consumption and delay in this technique is significantly higher.

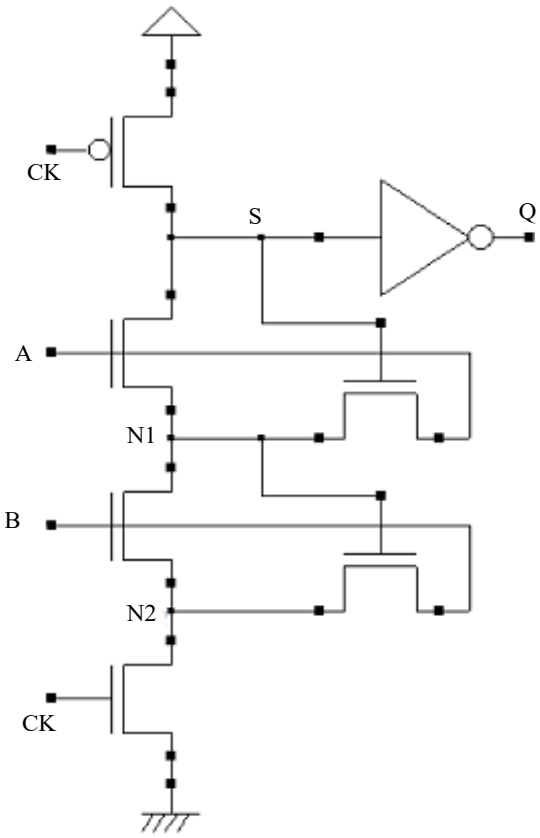

Figure 1. Twin-transistor technique.

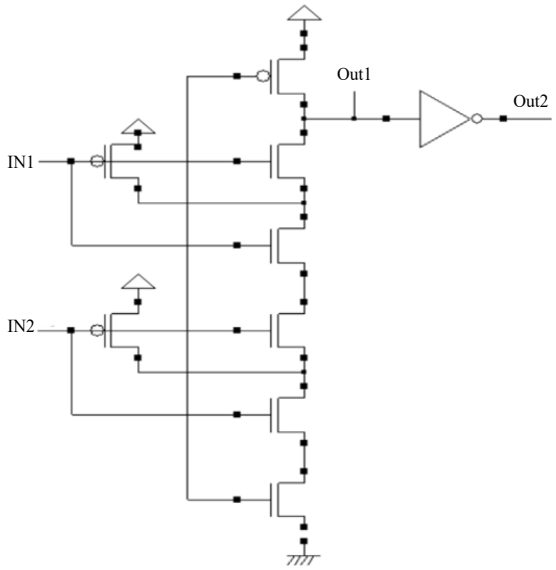

Figure 2. Bobba's technique.

Power consumption penalty is due to two reasons: (i) If the internal node p1 and p2 discharged during evaluation phase and as per operation they are required to charge up to V_{DD} in the pre-charge phase; hence, the node capacitance formed at the node p1 and p2 requires additional energy. (ii) Two extra transistors per transistor in N-logic increases the capacitance formed at the dynamic node and subsequently power consumption increases. Delay penalty of AND2 gate is due to the duplicated N-logic and increased capacitances at the gate inputs. Hence for wide fan-in PDN, use of this technique suffers from higher power and delay penalty. Domino techniques which enhance the noise immunity by pre-charging the internal node as well as by controlling the evaluation period are discussed as below [21].

Mendoza technique is shown in Figure 3, which increases the noise immunity by shortening the evaluation period as well as by pre-charging the internal nodes. Shorter evaluation period is achieved using Inverter Delayed Chain (IDL) logic which is used to generate the delayed clock which in turn drives the transistor M_N. Noise tolerance is also enhanced due to transistor M_P which is used to pre-charge node p2. In this technique, the delay circuitry needs to be designed to turn-off M_N approximately in the middle of evaluate phase; due to that, node p1 is virtually isolated from the impact of noise during rest of the evaluate phase.

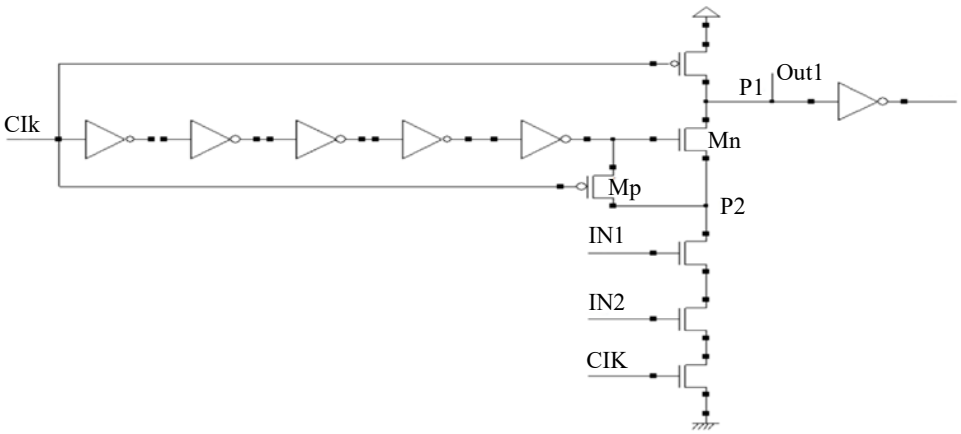

Figure 3. Mendoza technique.

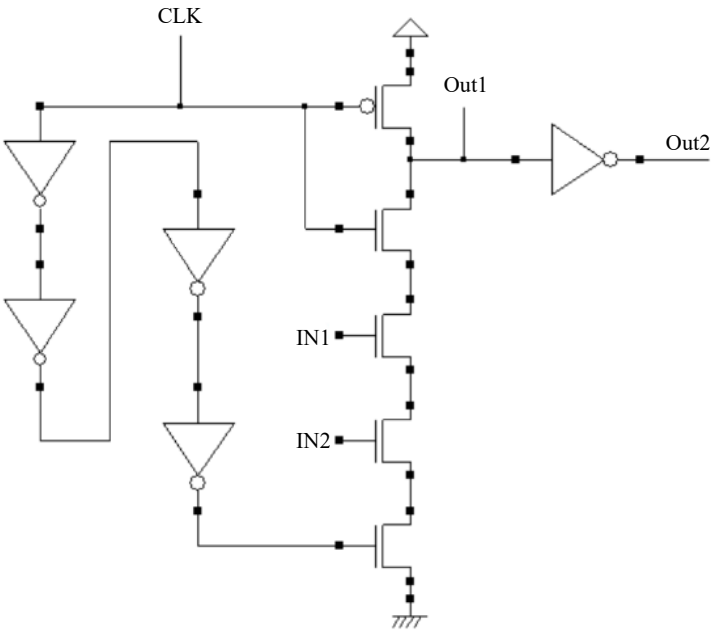

Figure 4. Proposed technique.

Moreover, noise tolerance is also increased when M_N is turned ON due to the presence of transistor M_P in the N-logic as it raised the voltage at node p2 up to V_{DD} during the pre-charge phase. However, this technique is not preferred for higher frequencies. Since in this technique, dynamic node discharging time is dependent upon time period during which transistor MN turns ON. For higher frequencies, this time period is not sufficient and requires to be increased. These can be done by increasing number of inverters in IDL chain as well as by increasing size of PDN transistors which results in to power consumption and delay penalty.

Like Mendoza technique, proposed technique enhances the noise tolerance by shortening the evaluation period [6]. However, circuit topology is different as compared to Mendoza technique in two respects. (i) Delayed clock drives the footer transistor instead of M_N transistor. (ii) nMOS is used as a pre-charging transistor instead of pMOS. However, further enhancement in the noise tolerance is achieved only by increasing the number of inverters in IDL chain which leads to significant power and area penalty like Mendoza technique [22].

Note that noise-tolerant techniques discussed above enhance the noise tolerance but at the cost of one or more design metric like power consumption, delay and silicon area. Hence, there is a demand to develop such a noise tolerant technique which enhances the noise immunity with minimum overhead in design metric. Moreover, Figure 4 shows the proposed technique of the system.

PROPOSED NOVEL TECHNIQUE

Our aim is to enhance the noise immunity of the proposed technique with the minor overheads [6]. In this section we initially describe the operation and limitation of the proposed technique with reference to noise immunity [6]. Later on, we represent the modification in the proposed technique in context of operation [6]. Section is concluded with the noise tolerance mechanism of the novel technique.

Operation of the Proposed Technique

Implementation and subsequently simulation of the circuit configuration have been performed in 90 nm technology using BSIM4 model and 1.2 V of VDD. Figure 5 represents the circuit configuration (AND2) with three internal nodes out1, out2 and out3. Operation of the circuit is divided into four phases (P1, P2, P3, P4) as shown in Figure 6.

P1

In this phase, on the lowering edge of the CLK signal, the circuit enters in to pre-charge phase and dynamic node is charged up to V_{DD}. However, DCLK is low in this phase such that M3 is off and as a result charge at the dynamic node is maintained.

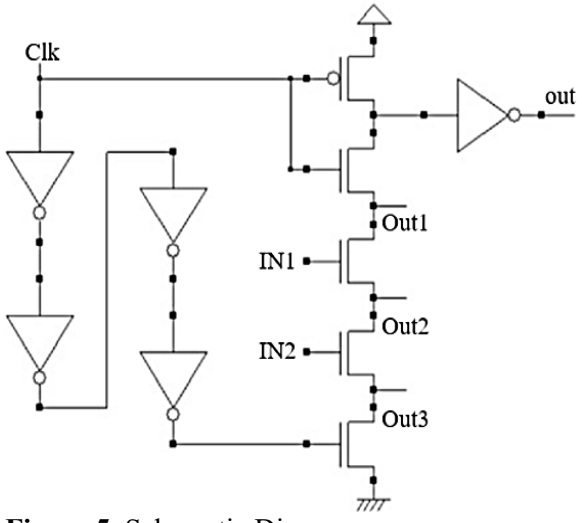

Figure 5. Schematic Diagram.

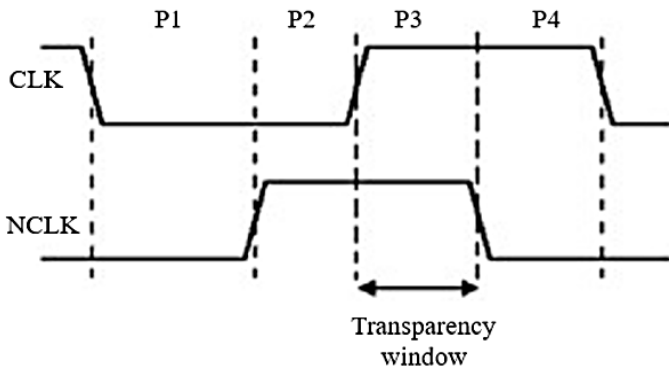

Figure 6. Operation.

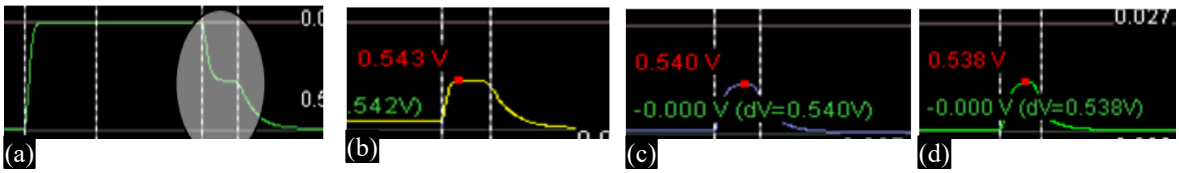

Figure 7. (a) Discharge at dynamic node, (b)–(d) Voltage levels at internal nodes out1, out2, out3 of PDN respectively.

P2

In the proposed technique [6], when CLK goes high, transistor M2 turns ON and evaluation phase begins. However, DCLK remains low in this stage, transistor M3 turns off so if PDN is ON either due to i/ps or noise pulses, charge level of capacitance of dynamic node is degraded as shown in Figure 7(a) due to charge sharing between dynamic node and internal nodes of PDN (parasitic capacitances). Hence, voltage level is increased at the internal nodes (out1, out2, out3) of PDN as shown in Figure 7(b–d).

Increased voltage level at the internal nodes directly leads to increased source voltages (V_{SBn}) of each transistor of PDN. Gate turn ON voltage must be greater than sum of source voltage and transistor threshold voltage (V_{TN}) when a transistor is turned ON. Higher V_{SBn} increases gate turn ON voltage. Additionally, due to body bias effect, V_{TN} of each transistor increases as per Eq. (1), when V_{SBn} increases, which is also helpful to improve Gate turn on voltage. In the evaluation phase, occurrence of a noise pulse requires larger magnitude as compared to Gate turn on voltage in order to turn ON the logic NMOS transistors.

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\emptyset_F|} - \sqrt{|2\emptyset_F|}\right) \quad (2)$$

Hence, gate voltage of each transistor of PDN plays a very important role in order to decide the noise immunity of circuit configuration in the case of external noise interference.

P3

In this phase, CLK and DCLK are high, transparency window is computed and the logic state of OUT node is dependent on the state of PDN. If PDN is ON, dynamic node as well as internal node are discharged and subsequently OUT go high. If PDN is OFF, dynamic node and internal node remains high and OUT goes low.

P4

CLK and DCLK are low and high respectively, transistor M1 and M3 are turned ON and transistor M2 turned off, due to that, charge of dynamic node does not escape.

However, the limitation of this technique is that the voltage level at the internal node of PDN is increased only up to 0.543 V in phase P2 due to charge sharing and subsequently noise immunity is marginally increasing of the circuit configuration. Note that the scope of further noise immunity

enhancement in circuit configuration is by obtaining higher voltage levels at the internal nodes of PDN. Literature represents the approach of pre-charging the internal nodes of PDN by accommodating additional transistors which is a useful approach in order to achieve higher voltage levels at internal nodes [8, 11, 23]. Likewise, in Bobba's method, one way is to connect the additional pre-charging transistors at each input node of PDN transistors (Figure 2). However, extra transistors in N-logic increases load capacitance of the gate input drivers which slow down the switching of the gates and also increase the area overhead [24, 25]. Likewise, in twin transistor technique (Figure 1), another possibility is using dynamic node driving pre-charge transistor and connecting its drain input to each input node of each PDN transistor which increases the capacitance formed at the dynamic node and subsequently power consumption and delay increases. Hence the number of pre-charging transistors and their positions in the circuit configuration is playing a very important role to enhance the noise immunity with minor overhead.

Operation of the Novel Technique

With aiming the enhancement in noise immunity with minor overhead, we have modified the proposed technique [6], such that in phase P2 the voltage level at the internal node of PDN is increased by incorporating only single pre-charging transistor MN as shown in Figure 8.

Due to addition of pre-charging transistor, operation of the proposed technique is modified and as explained below [6].

P1: Since the new transistor MN is situated between dynamic node and internal node, the voltage conditions at the dynamic node in this phase is same as existing technique. However, the voltage level at the internal node is additionally affected by the transistor MN as it pre-charges the internal node to higher voltage level of 0 to 0.8 V (VDD-Vtn), where Vtn is the threshold voltage of the transistor MN.

P2: When CLK goes high, transistor M2 turns ON and evaluation phase begins. However, in this phase, voltage at the internal nodes of PDN is higher as compared to proposed technique since they are pre-charged in phase P1 [6]. The voltage levels are observed as shown in Figure 8(a–d). This increased voltage levels increases VSBn (source to body) voltage of nMOS of PDN and subsequently Vtn of nMOS logic is increased as per Eq. (1). Hence, it is observed that as compared to proposed technique, i/p or noise pulses require higher magnitude to turn on the nMOS of PDN in the novel technique which subsequently enhanced the noise immunity.

Operation of phase P3 and P4 in the circuit configuration is similar to the proposed technique.

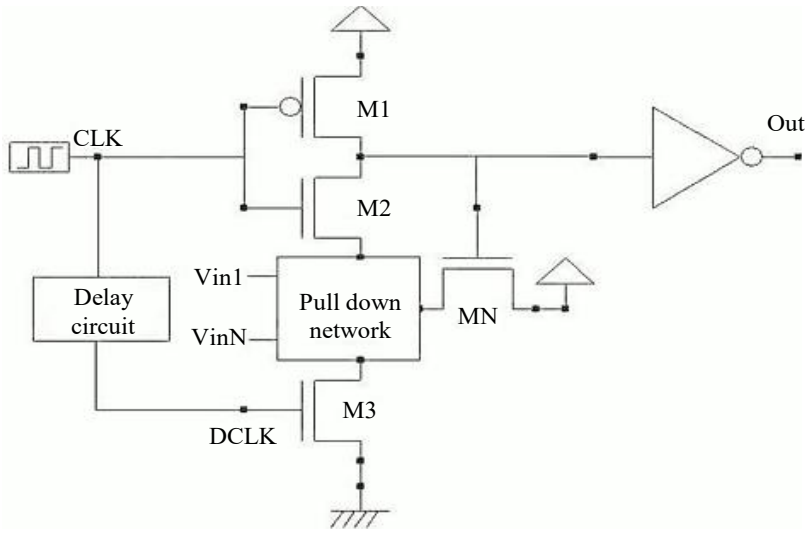

Figure 8. Schematic of Novel technique.

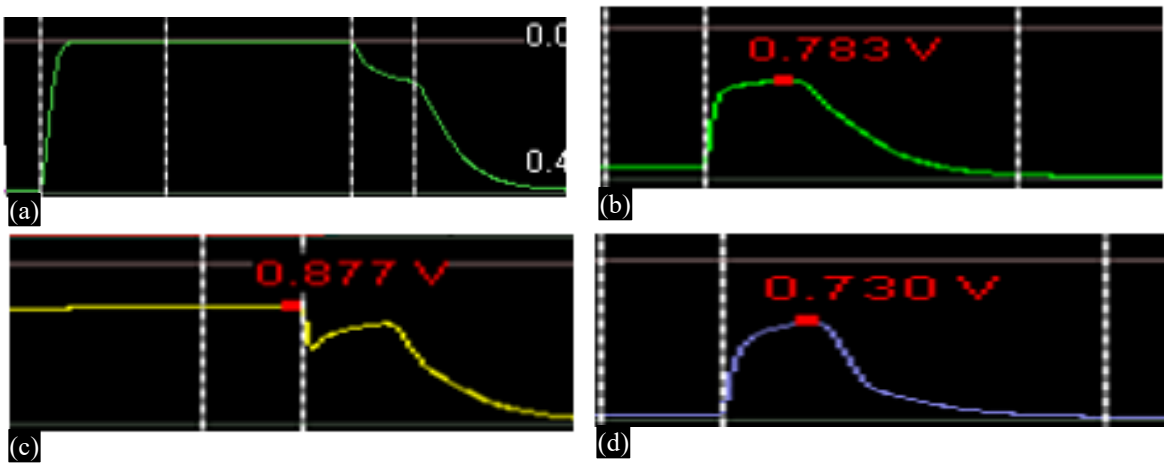

Figure 8. (a). Discharge at dynamic node, (b)–(d) Voltage levels at internal nodes of PDN.

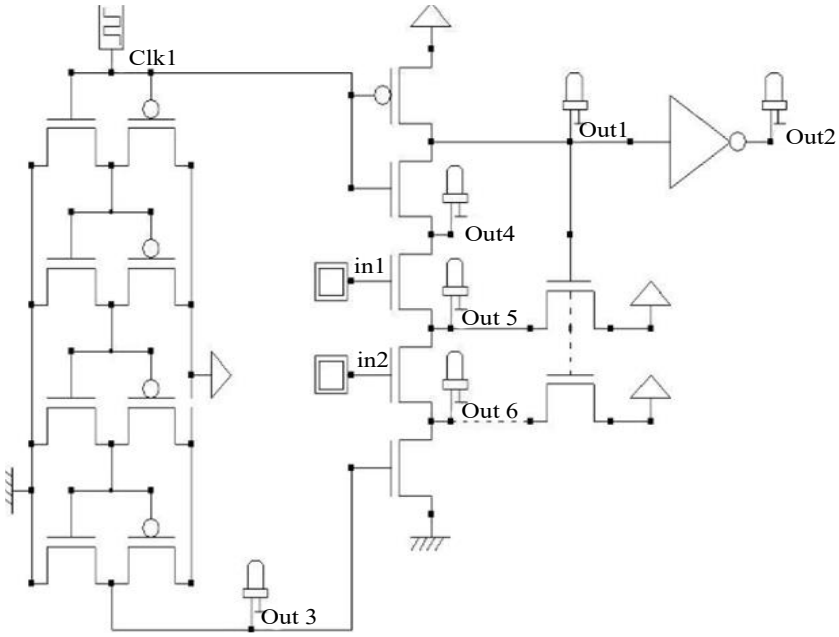

Figure 9. Node Selection of pre-charge transistor Mn.

Noise Tolerance Mechanism

Novel technique as shown in Figure 9 is having three internal nodes out4, out5 and out6 where dynamic node driving pre-charge transistor Mn might be connected. However, node out4 is top of PDN network, it cannot increase the Vtn of nMOS logic of PDN, as a result we have not considered the node.

i. *Node out6:* As shown in Figure 9, pre-charged nMOS transistor is connected at out6 terminal of circuit. Hence this node is pre-charged with the voltage V_{DD}-V_{TN} in the pre-charge phase (P1) and subsequently threshold voltage of both the NMOS1 and NMOS2 will increases and as a result noise tolerance is increased. However, in the phase P4, when CLK is low and DCLK is high, both M3 and MN transistors are simultaneously turned ON and as a result current flows from direct path of V_{DD} to GND which leads to high power dissipation.

ii. *Node out5:* As shown in Figure 9, pre-charge nMOS transistor is connected at out5 terminal of circuit. Hence this node is pre-charged with the voltage V_{DD}-V_{TN} in the pre-charge phase (P1) and subsequently threshold voltage of both the NMOS1 and NMOS2 will increases and subsequently noise tolerance is increased. Likewise, node out6, in phase P4, when CLK is low and DCLK is high, both M3 and MN transistors are turned ON but as the PDN is off no current flows from direct path of V_{DD} to GND and as a result power dissipation does not take place in P4.

From the above discussion, it seems that selection of node *out5* is an optimum choice compared to remaining nodes to enhance noise tolerance with minimum overhead in design metric.

SIMULATION ENVIRONMENT

The benchmark circuits are implemented using schematic modeling tool DSCH 3.1 to extract Verilog source, which is subsequently utilized by Microwind 3.1 tool to generate the layout file as shown in Figure 10 [25, 12]. Functionalities of the circuits are verified by applying various i/p's conditions to layout file and different system parameters like power, delay and noise immunity are analyzed with the help of same tool. We describe the behavior of AND2 and AND8 with reference to their implementation in this environment. Various techniques are employed and simulated for performance comparison in 90 nm technology with BSIM4 device model using following parameters (Table 1).

For noise immunity measurement, we have used the metric ANTE (Average Noise Threshold Energy) proposed in earlier studies [9, 8, 6]. The metric is defined as the average input noise energy that the circuit can sustain given by following expression.

$$ANTE=E(V^2_{noise}T_{noise}) \quad (3)$$

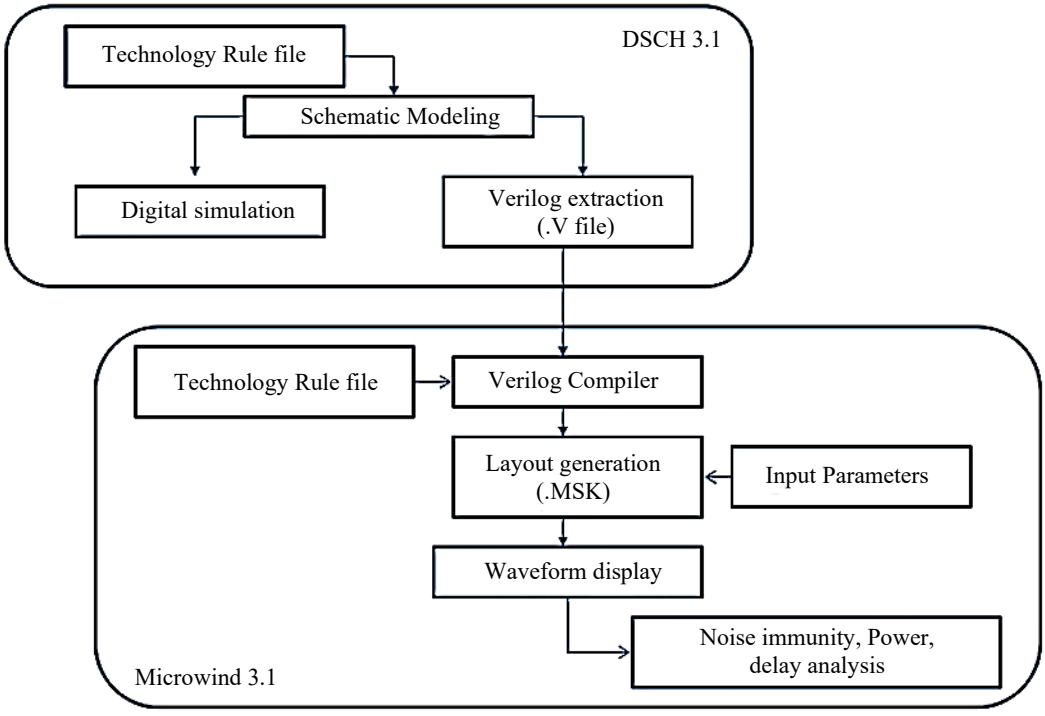

Figure 10. Simulation environment.

Table 1. Parameters used for the model.

Parameter	Specification
Technology	90 nm
V_{DD}	1.2 V
V_{tp}	0.32 V
V_{tn}	0.28 V
i/p Voltage	1.2 V
Temperature	27ºC
Noise Immunity	ANTE
Trade-off Parameter	ANTE/td and ANTE/Power
CLK Frequency	1 GHz

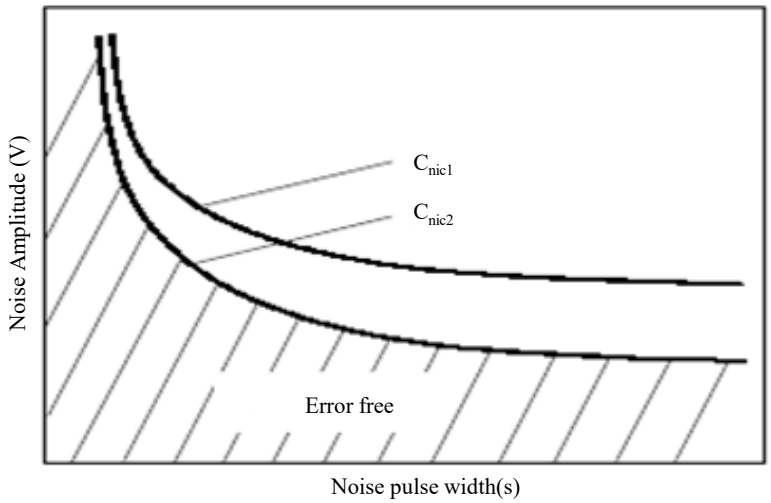

Figure 11. Noise Immunity Curve.

It seems from the expression that ANTE metric uses magnitude and duration (width) of noise pulse which may produces erroneous result. Since, an error to occur, noise pulse must have higher amplitude and long duration. Figure 11 represents the two noise immunity curve Cnic1 and Cnic2, the circuit whose noise immunity curve given by Cnic1 has better noise immunity (ANTE) as compared to Cnic2. However, ANTE metric only provides comparison in terms of noise immunity but it does not indicate the energy penalty in terms of design metric in order to get improvement in noise immunity. Hence, trade-off metrics, ANTE/t_d and ANTE/Power are also used in the study [9, 26, 27].

PERFORMANCE COMPARISON

In this section, we first present the performance evaluation-based analysis of the novel technique which helps us to judge appropriate internal node among all internal nodes to obtain enhanced noise immunity with minimum overhead in the design metric. Eventually, results of simulation-based experiments conducted over the circuit configuration of the published techniques like Mandoza, Bobba's and proposed technique with the novel technique are analyzed with respect to ANTE, power, delay, area, ANTE/td and ANTE/power [6]. The results are validated over small fan-in (AND2) and wide fan-in (AND8) circuit configuration in 90 nm technology. We have also suggested the approach to further enhance the noise immunity of the novel technique at the end of section. Note that for performance evaluation in terms of noise tolerance, we have considered the external/crosstalk noise. In the evaluation phase, we have applied the noise pulses to all the inputs of PDN due to that PDN momentarily turns ON and gates are switched from one state to another.

Performance Comparison at Internal Nodes of Novel Technique

Performance comparison in terms of ANTE, power and delay at various nodes of novel technique is presented in Figure 12. It seems that noise immunity (ANTE) is observed to be higher at node out5 as compared to all other nodes since at this node obtained voltage is reported higher (Figure 8(c)). Note that, power dissipation is significantly higher in the case of node out6, since, as discussed earlier (Figure 9), in the phase P4, when CLK is low and DCLK is high, both M3 and MN transistors are simultaneously turned ON, as a result current flows from direct path of V_{DD} to GND which leads to high power dissipation. From the discussion it concludes that out5 is the optimum choice among all internal nodes in terms of enhancement in noise immunity with minimum overhead in design metric. Hence, while representing performance comparison of novel technique with other techniques we have considered node out5 only.

Performance Comparison Using Small Fan-in

Figure 13(a–c) represents the performance comparison of existing technique with novel technique using AND2 as a bench mark circuit. From Figure 13 (b), it seems that Bobba's technique provides

better ANTE/Delay, ANTE/Power trade-off compared to other techniques with less area. For small fan-in (AND2), Bobba's technique provides 10.317x times, 9.416x times and 1.254x times better ANTE/Power and 3.525x times, 5.718x times and 2.565x times better ANTE/Delay compared to Mendoza, Proposed technique and Novel technique respectively [6]. It seems that for small fan-in circuit configuration, Bobba's is preferred choice.

Performance Comparison Using Wide Fan-in

We have attempted the performance comparison using wide fan-in (AND8) as a benchmark circuit. From Figure 14(a–c), it seems that trade-off factor ANTE/p (V^2/mw) and ANTE/td (V^2/ps) is found to be higher in the novel technique as compared to all other techniques. For wide fan-in (AND8), Novel technique provides 3.211x times, 2.1x times and 0.986x times better ANTE/Power and 2.068x times, 1.086x times and 1.288x times better ANTE/Delay compared to Mendoza, Bobba's and Proposed technique respectively [6].

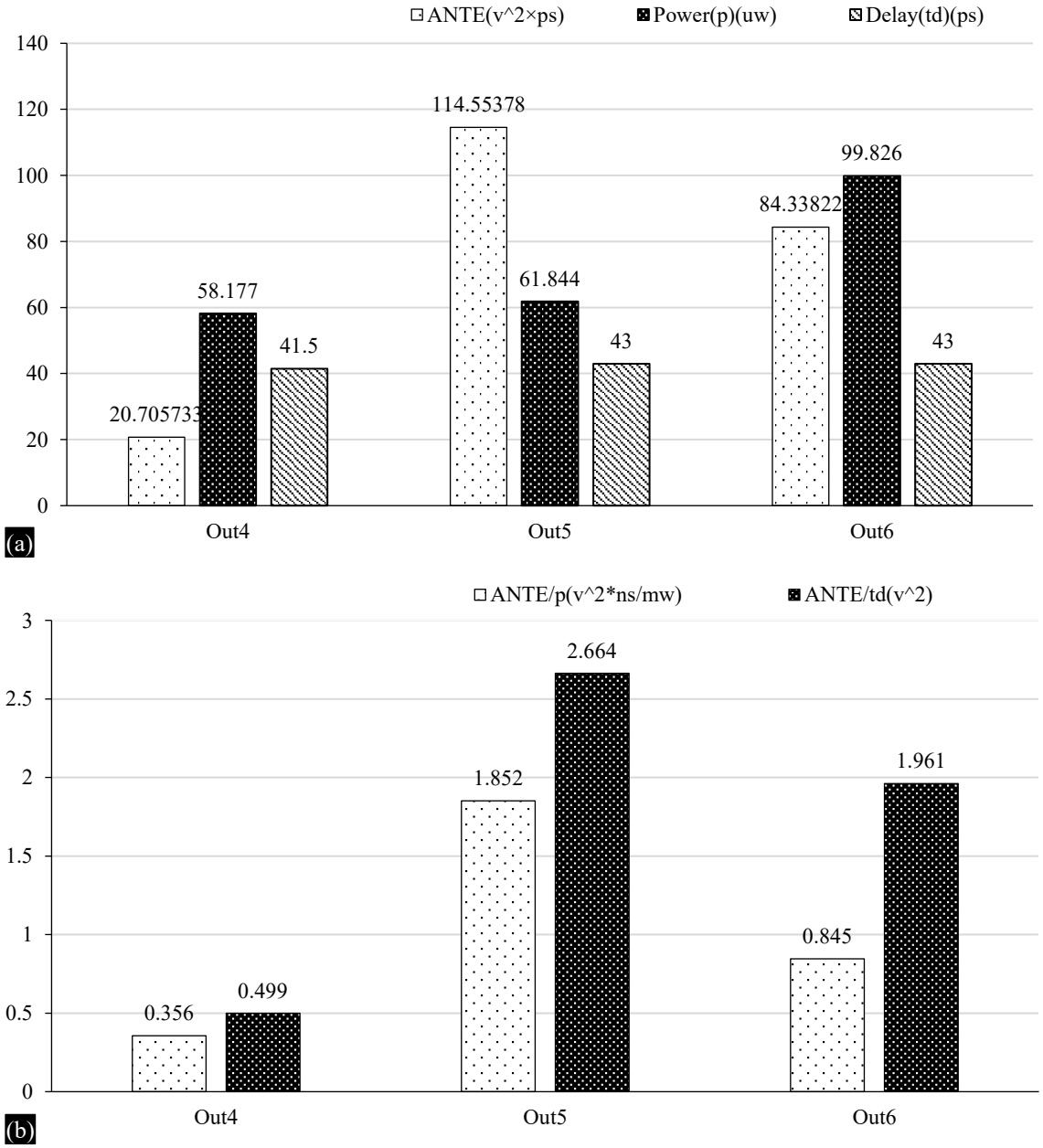

Figure 12. (a, b) Performance Comparison at internal nodes of novel technique.

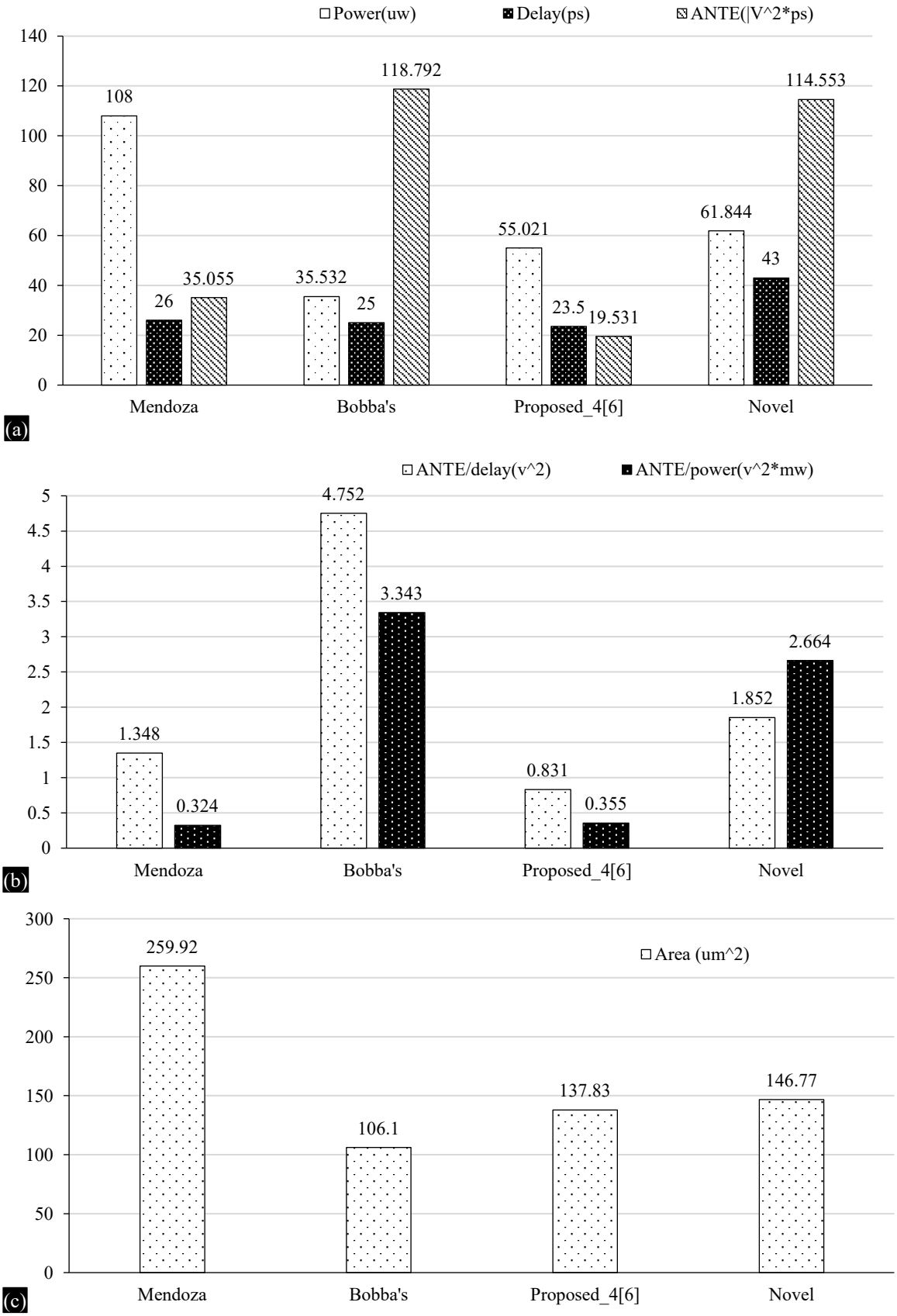

Figure 13. (a)–(c) Represents performance comparison using design metric, trade-off factors and area respectively of small fan-in circuit.

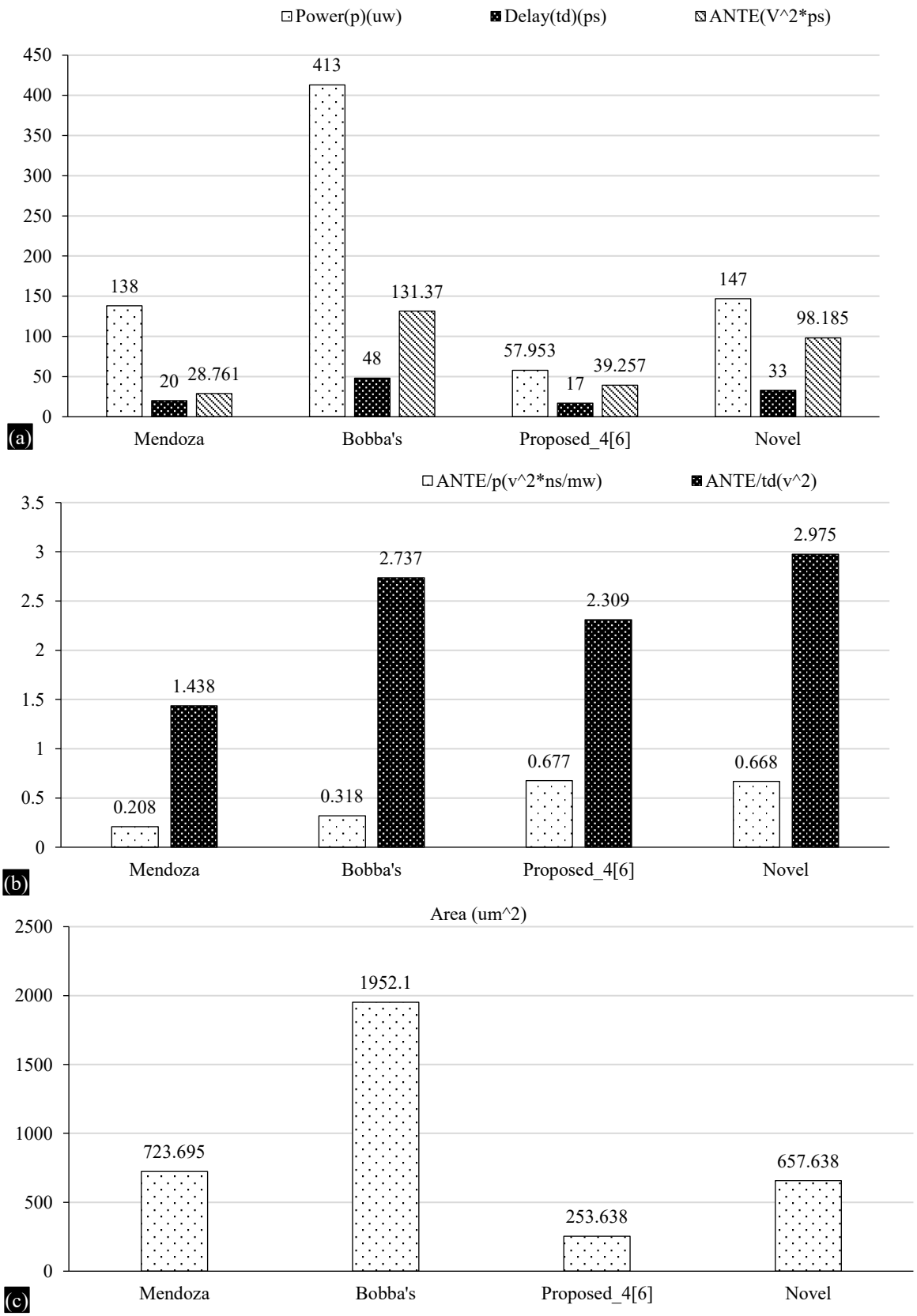

Figure 14. (a)–(c) Represents performance comparison using design metric, trade-off factors and area respectively of wide fan-in circuit. It seems that novel technique enhances the noise immunity (*ANTE*) with minimum overhead in design metric for the wide fan-in circuit configuration.

Approach to Enhance the Noise Immunity

In the novel technique, scope of enhancement in noise immunity by increasing the size of pre-charge transistor Mn is shown in Figure 15.

As the width of Mn increases, C_{GS} of Mn increases, due to that capacitance formed at node X increases, due to that its charge storing capacity (voltage) is increased and as a result noise immunity is further enhanced. Table 2 shows the variation in width vs. increases in the voltage at the node X.

Figure 16 shows the performance comparison in terms of ANTE, power and delay at various widths of pre-charging transistor Mn. From Figure 16 it seems that as the width of Mn increases, ANTE is increased (voltage formed at node X increases) but with that simultaneously design metrics i.e. power consumption and delay increase.

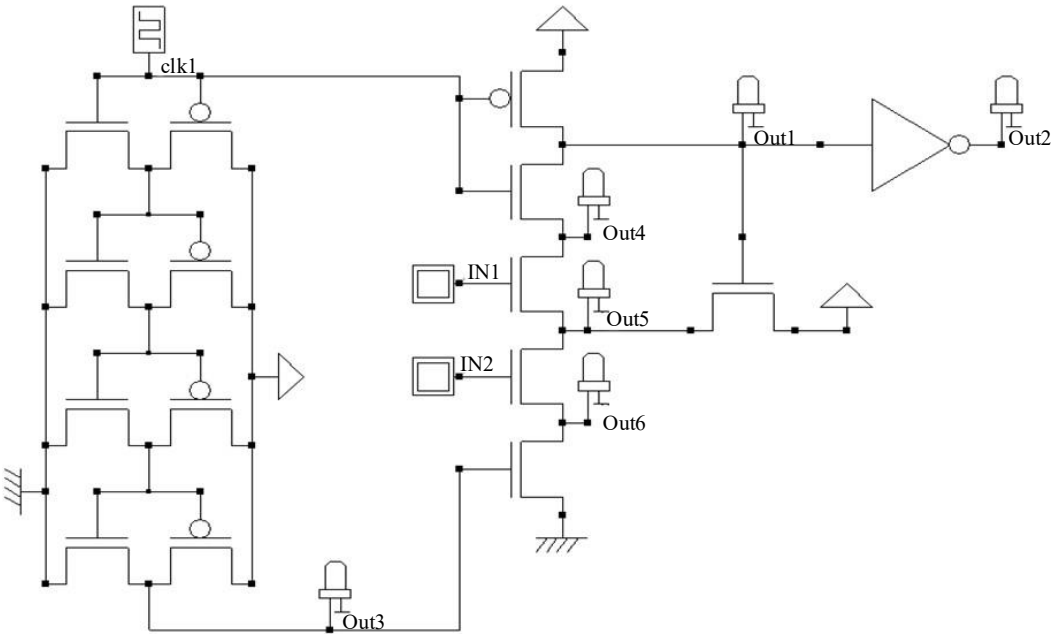

Figure 15. Increasing the width of Mn in novel technique.

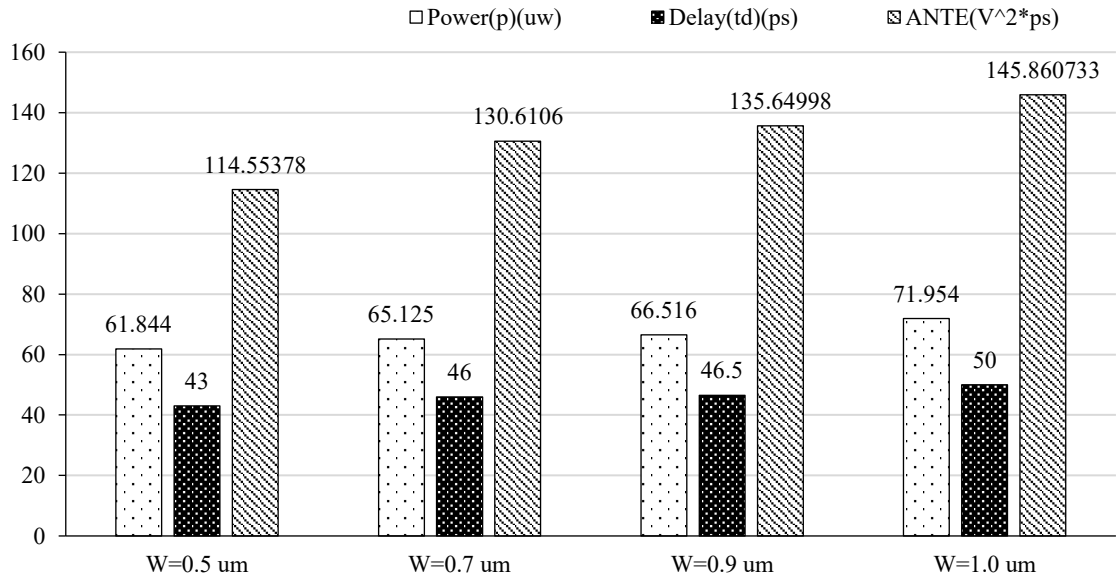

Figure 16. Performance Comparison at various width of Mn.

Table 2. Width vs. Increases in Voltage at node X.

Width of Mn	Voltage obtained at X
W_{Mn}=0.5 um	0.877 V
W_{Mn}=0.7 um	0.884 V
W_{Mn}=0.9 um	0.887 V
W_{Mn}=1.0 um	0.888 V

CONCLUSION

For wide fan-in (AND8) circuit configuration, Novel technique provides 3.211x times, 2.1x times and 0.986x times better ANTE/Power and 2.068x times, 1.086x times and 1.288x times better ANTE/Delay compared to Mendoza, Bobba's and Proposed_4 respectively. For small fan-in (AND2) circuit configuration, Bobba's technique provides 10.317x times, 9.416x times and 1.254x times better ANTE/Power and 3.525x times, 5.718x times and 2.565x times better ANTE/Delay compared to Mendoza, Proposed_4 and Novel technique respectively. Novel technique with width WMN=1.0 µm provides ANTE 1.273x times higher than of width WMN=0.5 µm at the cost of 1.163x times higher power consumption and 1.163x times higher delay.

- *For wide fan-in (AND8):* The Novel technique is superior in both ANTE/Power and ANTE/Delay metrics.
- *For small fan-in (AND2):* Bobba's technique outperforms others significantly in ANTE/Power and ANTE/Delay metrics.
- *Width Adjustment (WMN):* Increasing width improves ANTE but incurs higher power and delay penalties in the Novel technique.

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