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R-M and M-R Model for Interpreting Logic State of Memristor Aided NOR with Enhanced Noise Margin

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Abstract

Memristive crossbar arrays are one of the fascinating subjects in the field of nanoelectronics and memory devices. The arrangement of arrays consists of grid-like structure with rows and columns of memristors which are resistive devices that can preserve their resistance state even after power is turned OFF. They have now emerged as a promising alternative to traditional memory technologies due to their high density, non-volatility and low power consumption. This paper presents the technique of reading the state of memristor via two different models M-R model and R-M model in Memristor Aided Logic (MAGIC) NOR gate for prime and optimum noise margin. A comparative analysis of both the models are presented in which the M-R model is found to be more beneficial with 5% maximum voltage drop which is a bearable range for any voltage divider. Additionally, the study presents a thorough methodology for determining noise margins in order to assess the dependability and stability of logic circuits. The resilience of memristor-based logic devices in practical applications is determined by this analysis, which guarantees performance under a range of operating situations.

Keywords: Memristor, Magic NOR, Model, Noise Margin, Voltage Divider, Memory

INTRODUCTION

The advancement in technology has led the CMOS technology to face challenges in the nanoscale regime. The never-ending rise in demand for smart devices with high performance and integration facilities has forced the researchers to cater new technologies to fulfill the needs. Memristors are one such fundamental unit that can fulfill the demands in nanoscale regime. The unique characteristics of memristors like non volatility, fast switching speed, efficient, high density integration and reconfigurability has made it one of the significant members in the realization of advanced technology related devices. A memristor is a two terminal device that models a change in resistance based on the amount of charge that has flown through it in the past. The state of memristor can be depicted by its resistance value [1]. Magic (Memristive Aided loGIC) NOR is a particular implementation of a NOR gate that employs memristor devices to aid the logical operations. Figure 1 shows a NOR gate is a digital circuit whose output is HIGH only when all of its inputs are LOW [2, 3].

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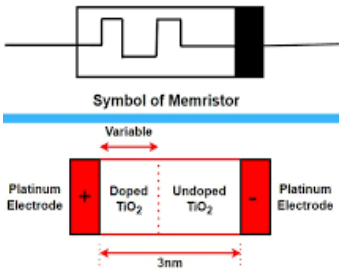
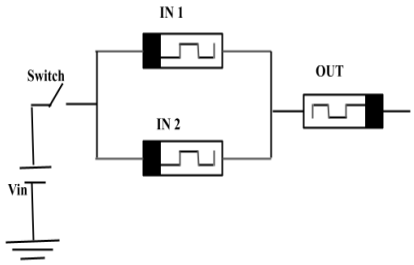
The noise margin is a significant postulation in logic circuits as it influences the robustness of circuit to external noise and variations in the signal levels. In digital circuits, the noise margin is the difference between the voltage levels of logic high and logic low states w.r.t unspecified voltage range in logic gate. It expresses the amount of noise or variation that can be present in the input signal while still certainly maintaining the legitimate logic level. The noise margin ensures that the logic circuit can suitably interpret the input signal and yield the correct output. High noise margin indicates that the

circuit can tolerate a higher level of noise without disturbing its functionality and low noise margin means that even the slightest variation or noise in the input signal can cause improper logic level interpretation and result in errors in the output [4–8].





IN1	IN2	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Figure 1. Memristor symbol, structure, Magic NOR gate and its truth table.

It plays an important role in supporting the reliability and stability of logic circuits by ensuring a safe margin against signal variation and noise selection of logic gates with high noise margin or by using noise rejection techniques circuits can be designed that are immune to external interference and environmental variation.

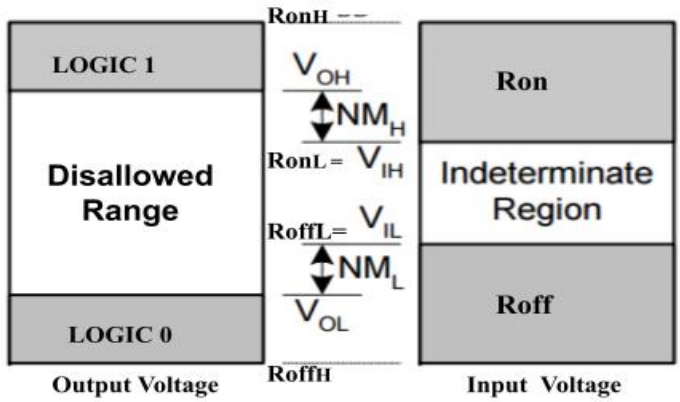


Figure 2. Noise Margin Representation.

There are two parts for measuring the noise margin selection of Ron and Roff depending on which series resistor value will be chosen and reading of output voltage as shown in figure 2.

The precision of memory reads in memristor memories can differ depending on several parts. First is the quality of the memristive device. Memristors are well known to have irregularity in their resistance levels and this variation can lead to variation in read accuracy. In addition to this, steadiness of resistance states in the long run can also impact the accuracy of memory reads. Secondly, the accuracy of memory reads also depends on the design and implementation of memory circuits which are involved in reading. The read circuitry should be able to precisely sense the states of memristor and transform it into corresponding data value. Any fallibility or noise in circuitry can result in error in read operation [9,10]. Third is the voltage and current levels that are used during read operation. The selection of current and voltage should be done carefully to make sure that memristor does not get pushed to some other state or level.

VOLTAGE DIVIDER METHOD

Out of reading and writing, reading operations need more attention as they are more prone to creating errors. So reading the stored information from memristive crossbar arrays is one of the important aspects of operations performed in memory devices based on memristors. One of the methods is using the

voltage divider rule. In this one of the known resistors is connected in series with the memristor to form a voltage divider configuration.

Voltage Divider on R-M Model

Memristors were first theorized in 1971 by Leon Chua who described a memristor as a two terminal electronic component and a fourth missing fundamental unit. It typically consists of thin solid state film wedged between two metal electrodes. This thin film is made in the combination of metal and oxide. The metal oxide materials used are titanium dioxide, hafnium oxide etc. In its initial state, the film is in a high resistance state but when a voltage is applied across it, the film undergoes structural change which leads to change in resistance.

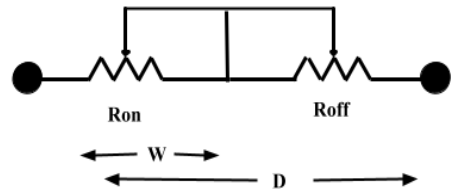


Figure 3. Memristor equivalent circuit.

Memristance of a memristor is given as

$$M = Ron\,W/D + Roff(1 - W/D \quad (1)$$

Where, W is the length associated with the change in flux, D is the whole length of memristor, Ron is the resistance of the state of the doped region as shown in figure 3. The dopants start moving on applying the voltage across the memristor thus causing change in flux whereas Roff is the resistance depicting the undoped region.

The R-M model is a configuration in which a known resistor is placed in series with a memristor or combination of memristors as in the case of MAGIC NOR.

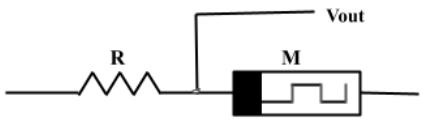


Figure 4. Structure of R-M model.

In the structure, it is clearly visible that the model has a resemblance with the voltage divider circuit which is given as

$$Vout = M/(M + R) \quad (2)$$

As memristors are a linear combination of Ron and Roff, their memristances can also be added in the same way as resistances are counted ie. if memristors are connected with opposite polarity, the combined resistance will be a constant value but twice of the individual memristance[11,12].The series combination of memristors can be represented as

$$M' = M1 + M2 + \ldots Mn \quad (3)$$

In the similar way memristances in parallel combination i.e memristors are connected with same polarity and can be calculated as

$$1/M' = (1/M1) + (1/M2)\ldots\ldots\ldots + (1/Mn)\ldots \quad (4)$$

So, MAGIC NOR configuration as seen from figure 4, two memristors are in parallel which are connected in series within a memristor. So their total memristance will be

$$Mparallel + Mseries = M/2 + M = 3M/2\ldots \quad (5)$$

The output obtained if MAGIC NOR is substituted in place of single memristor:

$$Vout = 2R/(3M + 2R) \ldots \quad (6)$$

Voltage Divider on M-R Model

This configuration of the M-R model consists of memristors first which are connected in a series with resistors. MAGIC NOR consists of a combination of memristors which are connected in series with a known resistor.

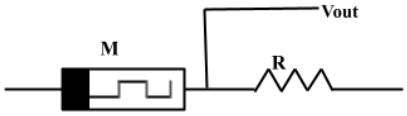


Figure 5. Structure of M-R Model.

In Figure 5, if M is replaced by a magic NOR circuit then M' will be calculated first (Effective Memristance) then will be connected to a known series resistor. Vout obtained will be

$$Vout = R/(R + M) \quad (7)$$

$$Vout\ NOR = 2R/(2R + 3M) \quad (8)$$

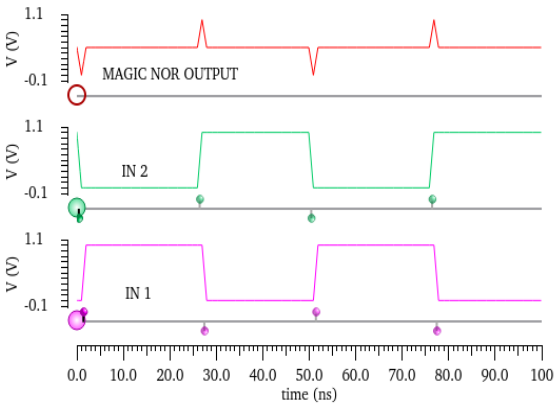


Figure 6. Magic NOR input/output

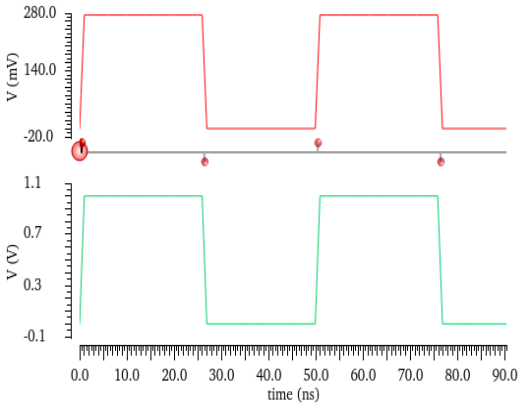


Figure 7. Voltage divider output M-R model

Figure 6 shows the Input/Output waveform of magic NOR gate which is showing the spikes only when both the inputs are off for very few ns time. Figure 7 shows the voltage divider output of a model in which only one memristor is placed in series with the one known resistor. Here it is seen that the maximum voltage drop is 5% as shown in table 1 and table 2

Table 1. Vin/Vout of M-R & R-M model.

Vin (V)	Vout (V) (M-R Model)	Vout (V) (R-M Model)
0.1	0.028	0.075
0.3	0.085	0.22
0.5	0.14	0.38
1	0.28	0.75
1.2	0.34	0.9
1.5	0.42	1.1

Table2. Voltage drop of M-R & R-M Model.

Vin	Vout (M-R Model)	Voltage Drop	Vout (R-M Model)	Voltage Drop
0.1	0.095	5%	0.005	95%
0.3	0.285	5%	0.015	95%
0.5	0.475	5%	0.025	95%
1	0.95	5%	0.05	95%
1.2	1.14	5%	0.06	95%
1.5	1.425	5%	0.075	95%

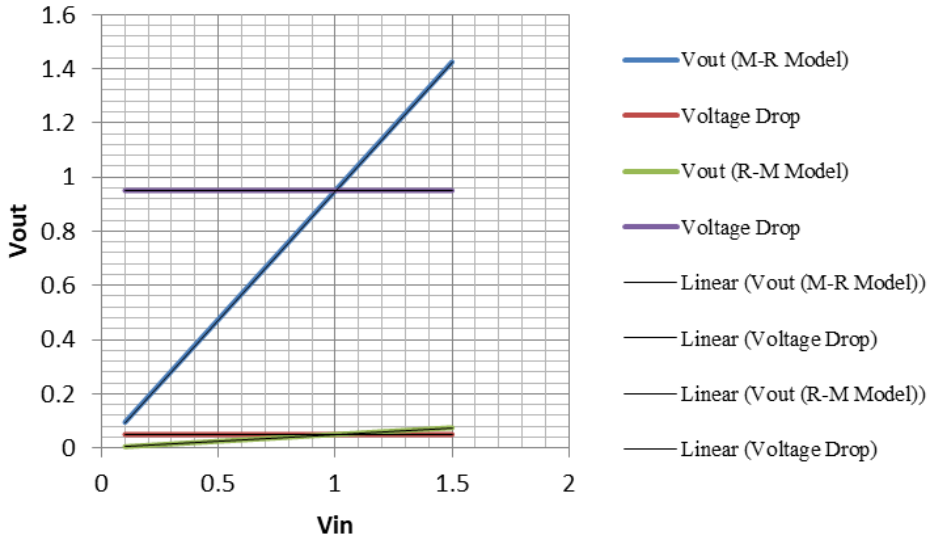


Figure 8. Voltage Drop representation of M-R and R-M model.

Excessive voltage drop will lead to improper functioning of equipment causing damage as there will be low power supply to device as shown in Figure 8.

STABILITY and RELIABILITY TESTER of MEMRISTIVE CIRCUIT

As mentioned earlier in this paper, to test the circuit for its reliability and stability Noise margin is the best parameter [13]. It plays a significant role in estimating the tolerable range of any device in which the circuit can work efficiently without any disturbance or data loss or without creating any error. From figure 2. Noise margin can be evaluated with its equivalent resistive state of memristors.

$$VNH = VOH\,Ron - VIHRon \tag{9}$$

$$V_{NL} = V_{IHRoff} - V_{OHRoff} \tag{10}$$

$$NM = V_{NH} - V_{NL} \tag{11}$$

Table 3. Noise Margin Calculation.

Vin	Vout at Ron	Vout at Roff	VNM
0.5	0.463	0.0161	0.447
0.7	0.648	0.0229	0.632
1	0.926	0.0322	0.894
1.2	1.111	0.0387	1.072

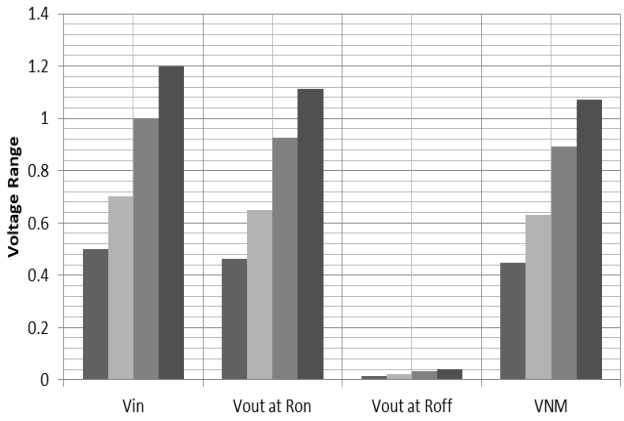


Figure 9. Noise margin after calculatingVout Ron and Roff\.

In the above table 3, it is clearly visible as the input voltage is increasing, Noise margin is also increasing. For the above table 3 calculations one of the significant things is to select optimal values of Ron and Roff. The resistor which is chosen in series with the M-R model plays an important role in deciding the value of Ron and Roff as shown in figure 9. It is generally taken as the geometric mean of Ron and Roff [14]. The value obtained should be such that below the optimal value memristor is in Roff state and vice- versa.

CONCLUSION

This paper focussed on the importance of reading of state. As out of reading and writing operations, reading is more vulnerable to create errors. Two models have been represented for reading of logic states based on voltage divider rule. This paper has indeed proven that the M-R model for reading the state of the memristive circuit is better as compared to the R-M model with 5% voltage drop which is found to be the maximum range for a good circuit. Memristor's performance for testing its reliability and stability has also been done in terms of noise margin which was found to be between 0.447 to 1.072V keeping the voltage scaling factor in mind.

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Declarations

1. *Ethical Approval:* This declaration is not applicable.
2. *Funding:* This declaration is not applicable.
3. *Availability of Data and material:* This declaration is not applicable.

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