STM JOURNALS

Journal of
VLSI Design Tools & Technology

ISSN: 2249-474X (Online)
ISSN: 2321-6492 (Print)
Volume 15, Issue 1, 2025
January–April
DOI (Journal): 10.37591/JoVDTT

https://journals.stmjournals.com/jovdtt

Review JoVDTT

Design and Implementation of Anti-Interference Low-Power Double-Edge Trigger Flip-Flop Based on C-Element

Shidesh S.[1,*], K.B. Ramesh[2]

Abstract

Double-edge triggered flip-flops (DETFFs) will use a lot more power when there are glitches and interference in the signal input. This work proposes an anti-interference low-power DETFF based on C-elements to efficiently lower the power consumption. This DETFF employs an enhanced C-element, which successfully filters input signal glitches, avoids redundant transitions within the DETFF, and lowers the transistor's charge and discharge frequencies. To lower its latency, the C-element has additionally incorporated pull-up and pull-down routes. In contrast to other DETFFs already in use, the DETFF suggested in this study only flips once on the edge clock, significantly lowering the number of duplicated transitions brought on by glitches thus efficiently lowering power usage. The suggested DETFF and ten more DETFFs are simulated in this work using HSPICE. The results demonstrate that the suggested DETFF has obtained high-performance indices in the areas of total power consumption, total power consumption with glitches and delays, and power delay products when compared to the other ten varieties of DETFFs. The suggested DETFF has reduced susceptibility to process, voltage, temperature, and negative bias temperature instability (NBTI) induced aging fluctuations, according to a thorough analysis of variance.

Keywords: Double-edge triggered flip-flop (DETFF), glitch, low-power, C-element, NBTI, power consumption, MUX

INTRODUCTION

With continuous progress in integrated circuit technologies, the scale of integrated circuits is constantly expanding. On the one hand, more advanced processes bring integrated circuit technologies to the deep submicron stage; on the other hand, the degree of integration increases with the number of transistors. These changes have made the problem of integrated circuit power consumption more prominent. In recent years, the rapid increase in portable consumer electronic equipment and circuit operating clock frequency has increased the need to reduce power consumption in circuit design. Therefore, low power consumption is a key challenge in modern integrated circuit design. For a digital integrated circuit, the power consumption of the sequential circuit accounts for a large proportion of the total power consumption. In the design of sequential circuits, the clock system is primarily composed of a clock tree circuit and sequential units. Power consumption in sequential circuits is the main source of all power consumption. As sequential elements in an integrated circuit, flip-flops are widely used in finite-state machine controllers, pipeline circuits, or storage elements, and their power consumption can account for 20%–

***Author for Correspondence**
Shidesh S.
E-mail: shideshs.ei23@rvce.edu.in

[1]Student, Department of Electronics and Instrumentation Engineering, R.V. College of Engineering, Mysore Road, Bengaluru, Karnataka, India
[2]Associate Professor, Department of Electronics and Instrumentation Engineering, R.V. College of Engineering, Mysore Road, Bengaluru, Karnataka, India

Received Date: January 16, 2025
Accepted Date: January 20, 2025
Published Date: January 28, 2025

Citation: Shidesh S., K.B. Ramesh. Design and Implementation of Anti-Interference Low-Power Double-Edge Trigger Flip-Flop Based on C-Element. Journal of VLSI Design Tools & Technology. 2025; 15(1): 36–44p.

45% of the total power consumption of the circuit. A low-power flip-flop designed as a basic component can provide significant advantages in reducing the total power consumption of integrated circuits [1].

EXISTING DETFF

Multiplexer-type DETFFs

Figure 1 shows a multiplexer-type DETFF LM1, which includes a multiplexer (MUX) and clock tree consisting of two inverters and two internal latches (LA1 and LA2). The input signal is *D*, and the output signal is *Q*. LM1 uses two latches and a multiplexer. The first and second latches the sample data when the clock signal CLK is high and low, respectively. The multiplexer will be in the logic value selection of the hold-mode latch for the output. The disadvantage of LM1 is that the state of the latch in the transparent mode changes with changes in the input signal, resulting in redundant transitions. When the input signal has glitches owing to various interferences, the latch in the transparent mode generates more redundant transitions, which increases the power consumption of the circuit [2]. The more glitches the input signal, the higher the power consumption overhead. Figure 2 shows the structure proposed in Ref. LM2 is composed of two latches, a clock tree composed of two inverters, and a multiplexer. Compared to LM1, LM2 uses two transistors instead of a transmission gate and an inverter in two latches. There are two main problems with the LM2. First, in the feedback path of the two latches of LM2, the input signal controls the transmission of the clock signal, causing the output load of the clock tree to be large and the overall power consumption to be relatively large. Second, LM2 encounters a level conflict problem. For example, when CLK is zero, CK1 is one, CK2 is zero, and the transmission gate TG1 is turned on. When *D* is 0, A1 switches to 0 and B1 switches to 1, causing transistor N1 to turn on [3]. Therefore, node A1 is simultaneously written with 0 and 1, causing level conflict. Similarly, when CLK and *D* are both one, another latch node A2 will also have a level conflict problem. This problem greatly increases the power consumption of LM2. Finally, LM2 encounters redundant transitions caused by glitches in the input signal, leading to excessive power consumption.

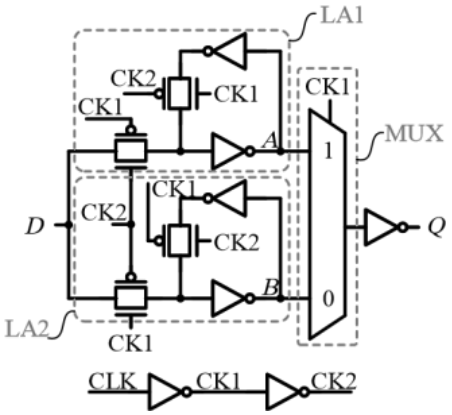

Figure 1. Structure of DETFF LM1.

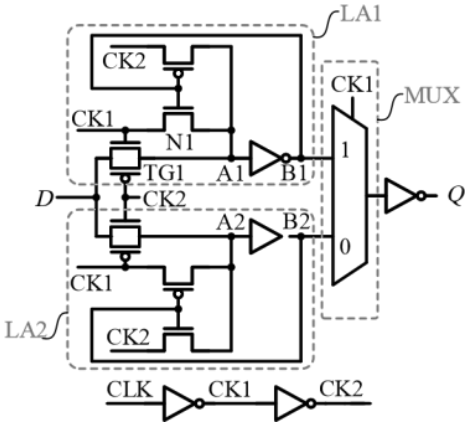

Figure 2. Structure of DETFF LM2.

PROPOSED METHODOLOGY

The working principle is illustrated in Figure 3. When the input signal *D* changes between clock edges, the output signal *Q* remains unchanged. Between the first falling edge and the first rising edge of the CLK, LA remains in the high-impedance state, the logic state is 1, and *B* is in state 1. At this time, the output *Q* is 1, *D* is flipped, *A* is flipped to state 0, *B* is kept in the high-impedance state, and the logic state is 1. Through the C-element, the output *Q* was still 1. When signal *D* remains unchanged, the clock signal does not flip anyway, and the output signal *Q* does not flip. Before the second falling edge of CLK, *D*, and *B* are 0, *A* is in a high-impedance state, the state is the previous 0, and the output *Q* is 0. After the second falling edge of the CLK, *D* remained at 0. Currently, *A* is 1, *B* is in a high-impedance state, and the state is the previous 0; therefore, the output *Q* remains at 0. The Q output will only flip to *D* when the clock edge arrives, and *Q* is different from *D* [4].

Table 1 shows the truth table of internal nodes *A* and *B* and output *Q*. The hold in Table 1 indicates that the output state *Q* maintains the previous clock level and the high-impedance state indicates that the latch is in the turn-off state.

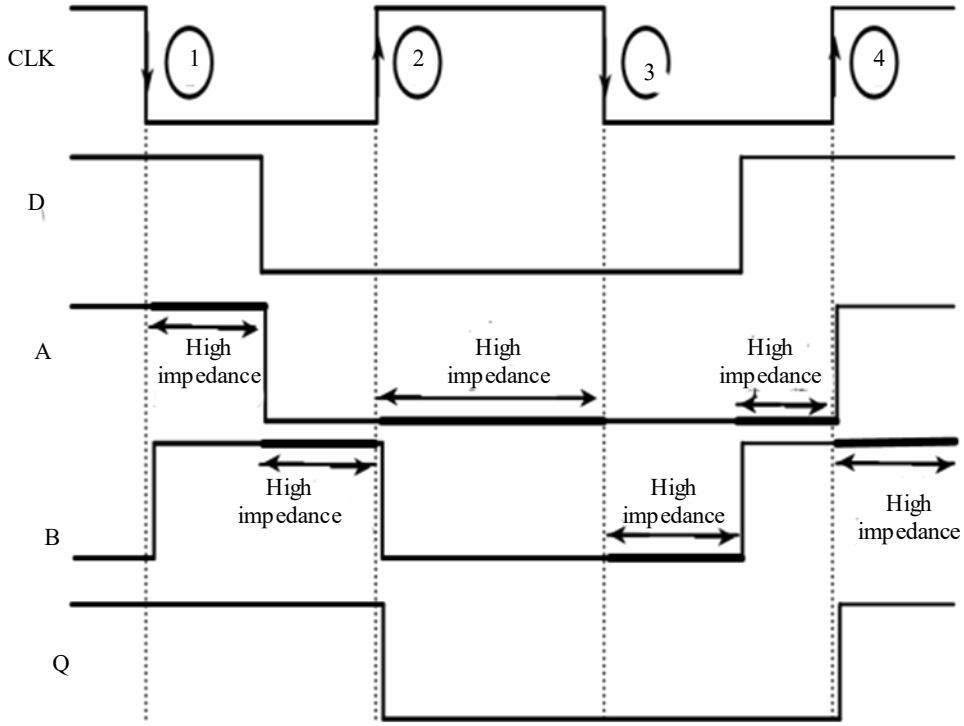

Figure 3. Working principal waveform.

Table 1. State truth table for nodes *A*, *B*, and *Q*.

A	B	Q
0	0	0
0	1	Hold
1	0	Hold
1	1	1
High impedance	1	Hold
High impedance	0	Hold
1	High impedance	Hold
0	High impedance	Hold

Signal D input was fed to LA and LB. Thus, regardless of whether the clock signal CLK is switched or not, at most, one of the output states of nodes *A* and *B* is in a high-impedance state. From the function of the C-element introduced earlier, we know that an input signal in a high-impedance state does not affect the output state. Currently, the output of the C-element is maintained. Only when the output states of latches LA and LB are the same is the output of the DETFF *Q* the same as the input signal *D* [5].

In this study, we simulated the proposed DETFF using the HSPICE platform. A Predictive Technology Model (PTM) 32 nm process was used. The power supply voltage is 0.9 V, temperature is 25°C, clock frequency is 250 MHz, and clock period is 4ns.

EXPECTED RESULTS

In Table 2, # *T* represents the number of transistors, TP represents the total power consumption of the circuit, tcq represents the delay from the clock signal CLK to the output signal *Q*, PDP represents the Power Delay Product of the circuit, which is an important composite index, tsetup represents the setup time of the flip-flop, thold represents the hold time of the flip-flop, CTP represents the clock tree power consumption of the circuit, G2 represents the total circuit power consumption when there are two glitches in a single clock cycle, and G4 represents the total power consumption with four glitches in a single clock cycle [6].

As shown in Table 2, the total power consumption of circuits LM2, EP1, and EP2 was relatively large. LM2 uses a transmission tube instead of a transmission gate and an inverter, and part of the clock signal is directly connected to the source of the transistor, resulting in greater power consumption. The level conflict problem of LM2 is also one of the reasons for its excessive power consumption. EP1 and EP2 are both explicit pulse-type DETFFs, and some of the circuits of their pulse generators will introduce large power consumption, causing the total power consumption of the circuit to be relatively large. Meanwhile, the total power consumption of the DETFF circuit proposed in this study was the lowest among the 11 types of flip-flops.

In terms of circuit delays, the delays of LM1 and the Solid-State Power Controller (SSPC) are the smallest, whereas the delays of C-element-type DETFFs, such as LG C and IP C, are larger [7]. This is because the design uses a C-element and its driving current is small. This condition causes an excessively high delay. Although the DETFF proposed in this paper also uses a C-element, its delay is much lower than that of other C-element type DETFFs because it uses an improved static C-element. A feedback loop increased the pull-up and pull-down capabilities of the C-element [8]. As a result, this feedback loop has a lower latency than a C-element with the same transistor size.

The SSPC was the lowest and the PDP of LM2 was the highest. The PDP of DETFF proposed in this study was the second lowest. However, the number of transistors used by the SSPC is 25% higher than that of the proposed flip-flop, and thus, the proposed DETFF has a better comprehensive performance. Because the clock load is large and some of the clock signals are directly connected to the transistor source, the power consumption of the clock tree of LM2 is excessively large. In EP1 and EP2, the clock tree formed by the pulse generator is more expensive and requires more resources. Therefore, the power consumption of the clock tree is too large. The flip-flops proposed in this paper use a C-element, which reduces the clock load and reduces the clock tree power consumption. Thus, the power consumption of the clock tree was acceptable. The comparison results are listed in Table 3, which also shows the proposed DETFF in the presence of glitches in the input signal [9]. The total power consumption of the circuit is better than that of all the comparative flip-flops, with an average increase of 43.62% and 51.28%, respectively. In summary, compared with contrast DETFFs, the DETFF proposed in this study has achieved greater advantages in terms of total power consumption, delay, PDP, and total power consumption with glitches in the input signal [10, 11].

Table 2. Comparison of the DETFF proposed in this paper.

DETFFL	# *T*	TP (W)	tcq (ps)	PDP (10^{18}J)
LM1	26	1.75	37.14	65.18
LM2	22	23.80	39.34	936.07
TCRFF	22	1.52	80.97	123.34
LM C	26	1.22	72.20	88.11
LG C	28	1.44	84.04	120.66
IPC	26	1.39	77.65	107.65
25.08	148.59	0.29	1.39	1.39
FNC	30	1.18	74.28	87.28
15.59	101.43	0.32	1.36	1.53
EP1	22	2.29	51.42	117.65
EP2	25	3.35	46.42	155.59
SSPC	40	1.21	37.28	45.28
Proposed	32	1.12	48.91	54.63

Table 3. Comparison of the relative cost of glitches caused by interference.

DETFF	G2 (%)	G4 (%)
LM1	48.71	58.02
LM2	94.72	94.73
TCRFF	45.86	58.41
LM C	28.23	43.05
LG C	38.45	48.95
IP	17.95	19.57
FN C	16.46	26.65
EP1	49.23	50.65
EP2	65.87	66.42
SSPC	30.71	46.38
Average	43.62	51.28

VARIANCE ANALYSIS

With the development of integrated circuit technology and continuous progress in technology, the impact (%) of process, voltage, and temperature (PVT) and negative bias temperature instability (NBTI)-induced aging variations on the reliability of nanoscale integrated circuits has become increasingly serious. A comparison of the relative costs of the glitches caused by interference is shown in Figure 3. This section evaluates the power consumption and delay performance of the DETFF under PVT- and NBTI-induced aging variations. We took the gate length as a relative variable, changing from 32 to 42 nm with a step size of 1 nm. The power consumption and delay variations of the DETFFs were obtained, as shown in Figures 4 and 5 [12]. In particular, because LM2 power consumption is larger than that of the other DETFFs, it uses the secondary axis on the right side. With an increase in gate length, the power consumption of the circuit shows a downward trend, whereas the delay steadily increases. LM C, LG C, IP C, and the other three C-element-type DETFFs gradually fail to function as the gate length increases, indicating that they are very sensitive to process variations [13]. Moreover, the DETFF proposed in this study can operate normally under process variations, showing good robustness, as shown in Figure 3.

In Figures 5 and 6, the voltage is increased from 0.75 to 1.25 V, with a step size of 0.05 V. Because LM2 power consumption is larger than that of other DETFFs, it uses the secondary axis on the right side of Figure 5. As shown in Figure 5, the power consumption of the circuit increases with voltage.

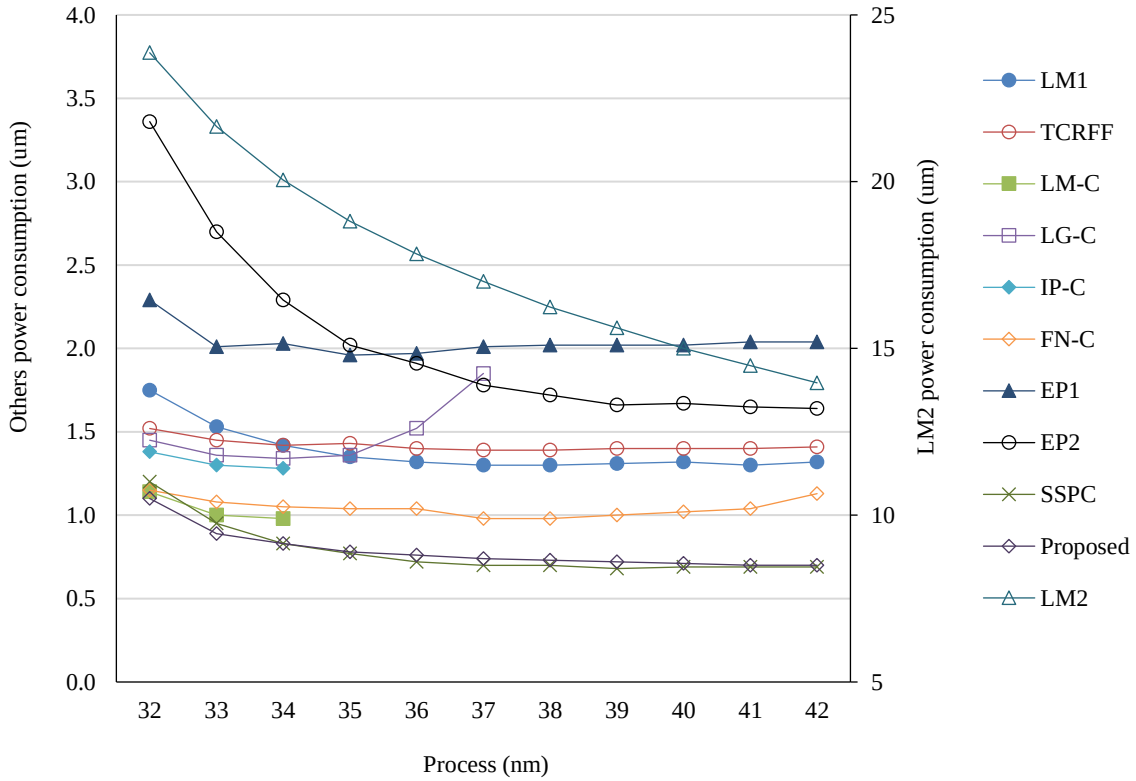

Figure 4. Effect of process variations on the power consumption of DETTF.

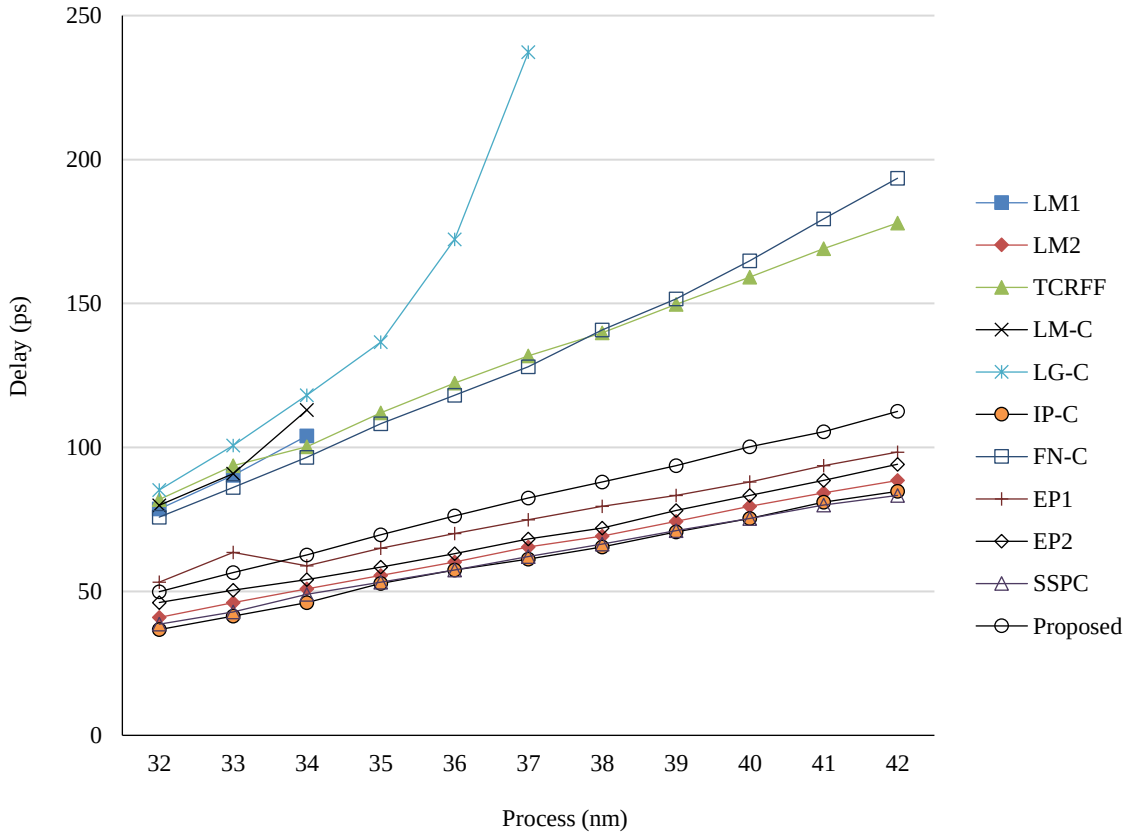

Figure 5. Effect of process variations on the delay of DETFF.

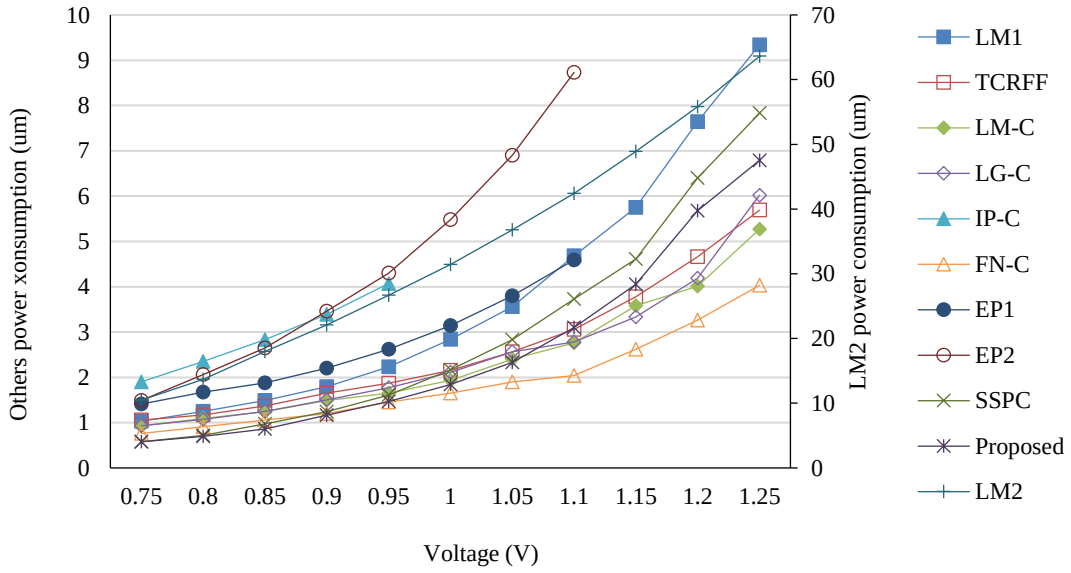

Figure 6. Effect of voltage variations on the power consumption of DETFF.

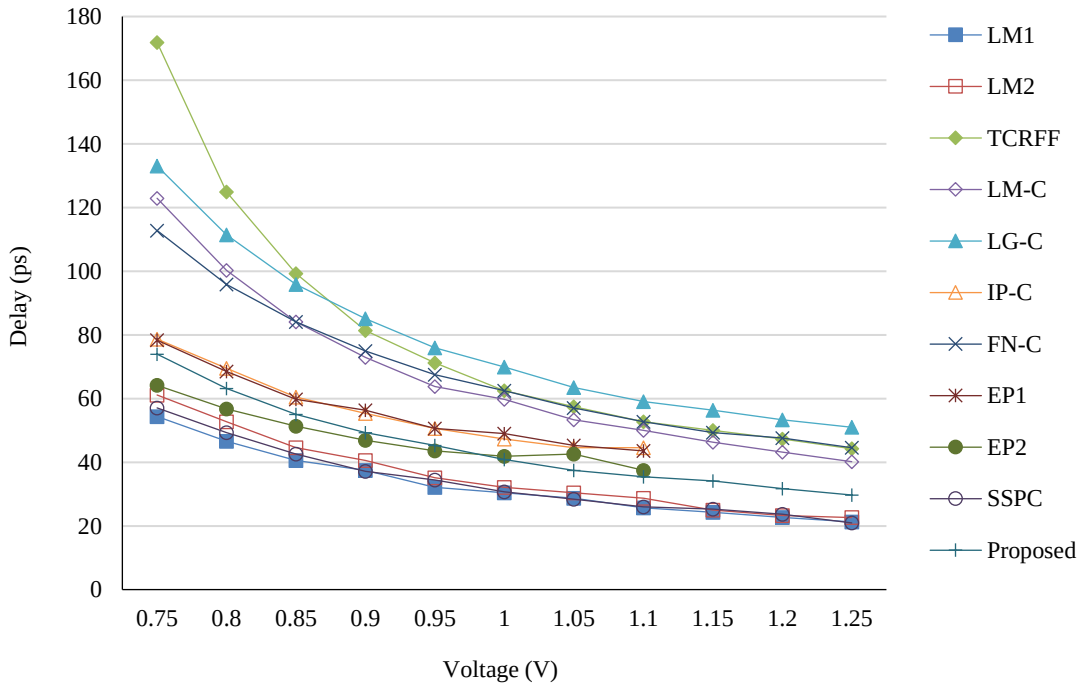

Figure 7. Effect of voltage variations on the delay of DETFF.

The power consumption is proportional to the square of the voltage. In Figure 6, the circuit delay continues to decrease as the voltage increases because the larger the supply voltage, the faster the conduction current, and the smaller the delay. Furthermore, IP C does not properly work at low voltages, such as 0.75 V, 0.8 V, and 0.85 V, whereas EP1 and EP2 do not work properly at high voltages, such as 1.15 V, 1.2 V, and 1.25 V. The DETFF proposed in this study can normally work under a voltage fluctuation of 0.75–1.25 V and is not sensitive to its variations. The effects of temperature variations on the performance of the DETFFs are shown in Figures 7 and 8, where the temperature ranges from 25 to 75°C with size steps of 10°C. In particular, because LM2 power consumption is larger than those of the other DETFFs, it uses the secondary axis on the right side of Figure 8, which also shows power consumption.

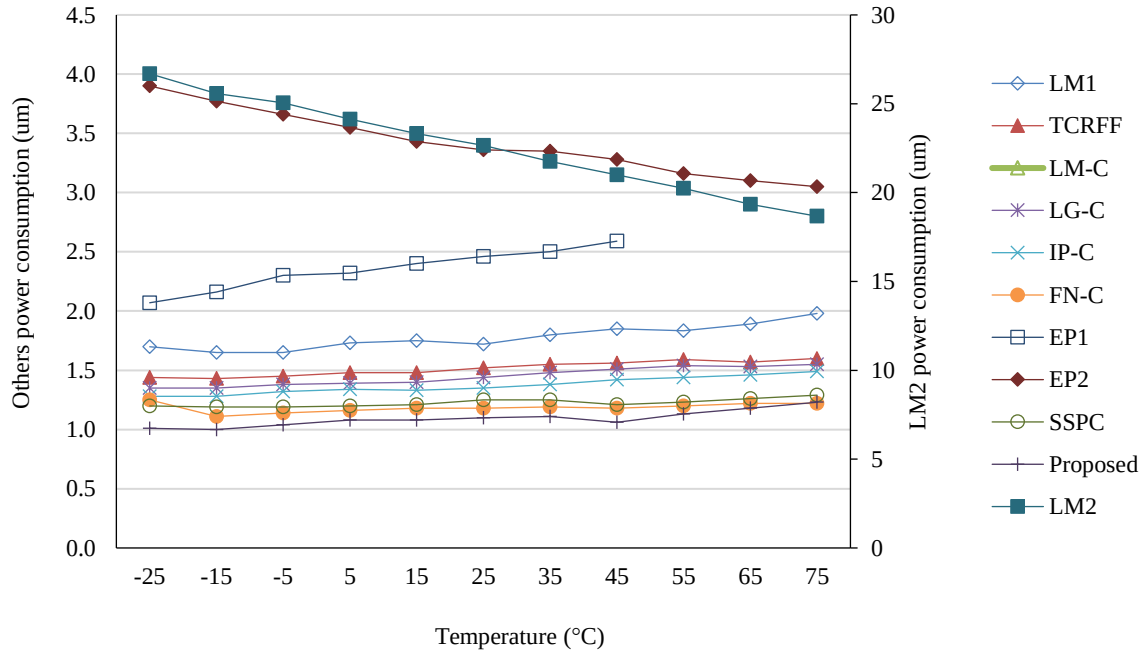

Figure 8. Effect of temperature variations on the power consumption of DETFF.

CONCLUSION

To effectively reduce the power consumption of DETFFs, this paper presents an anti-interference low-power DETFF based on a C-element. We used an improved static C-element to reduce the clock load and power consumption of the clock tree. The use of C-elements can effectively reduce the redundant transitions of the internal nodes of the circuit and further reduce the overall power consumption. Compared with previous DETFFs, the DETFF proposed in this study has great advantages in terms of total power consumption, clock tree power consumption, PDP, and anti-interference glitch-blocking capabilities, which have good comprehensive performance. The detailed variation analysis shows that it is not sensitive to variations such as PVT. Moreover, it can achieve better performance in the aging simulation and has high reliability.

REFERENCES

1. Yang B, Yu Z, Wei J. Design of low-power modern radar SoC based on ASIX. Tsinghua Sci Technol. 2014;19(2):168–73. doi:10.1109/TST.2014.6787370.
2. Hu S, Ji W, Wang Y. Feedback cache mechanism for dynamically reconfigurable VLIW processors. Tsinghua Sci Technol. 2017;22(3):303–16. doi:10.23919/TST.2017.7914202.
3. Dai Y, Shen J. An explicit-pulsed double-edge triggered JK flip-flop. 2009 International Conference on Wireless Communications & Signal Processing, Nanjing, China. 2009. p. 1–4. doi:10.1109/WCSP.2009.5371580.
4. Zhao P, McNeely J, Golconda P, Bayoumi MA, Barcenas RA, Kuang W. Low-power clock branch sharing double-edge triggered flip-flop. IEEE Trans Very Large Scale Integr (VLSI) Syst. 2007;15(3):338–45. doi:10.1109/TVLSI.2007.893623.
5. Kim C, Kang SM. A low-swing clock double-edge triggered flip-flop. IEEE J Solid-State Circuits. 2002;37(5):648–52. doi:10.1109/4.997859.
6. Nedovic N, Oklobdzija VG. Dual-edge triggered storage elements and clocking strategy for low-power systems. IEEE Trans Very Large Scale Integr (VLSI) Syst. 2005;13(5):577–90. doi:10.1109/TVLSI.2005.844302.
7. Rawat A, Kumar M. Low power CMOS based dual edge triggered flip flop using LECTOR C-element. 2024 International Conference on Computer, Electronics, Electrical Engineering & their Applications (IC2E3), Srinagar Garhwal, Uttarakhand, India, 2024. p. 1–6. doi:10.1109/IC2E362166.2024.10827394.

8. Huang Z, Zhong W, Duan L, Zhang Y, Liang H, Wang J, Song T, Lu Y. Low-power anti-glitch double-edge triggered flip-flop based on robust C-elements. J Circuits Syst Comput. 2022;31(13):2250231. doi:10.1142/S0218126622502310.
9. Gopika EP, Anand AB, Shajin S, Angel Prabha P, Brinda P, Sreenidhi H, Rajeev P, Baby Sreeja SD. Efficient design and analysis of dual-edge triggered flip-flop for advanced VLSI systems. 2024 10th International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India, 2024. p. 306-310. doi:10.1109/ICACCS60874.2024.10717092.
10. Raj MP, Kavithaa G. Dynamic signal driving strategy based high speed and low powered dual edge triggered flip flop design used memory applications. Microprocessors and Microsystems. 2019;71:102879. doi:10.1016/j.micpro.2019.102879.
11. Tulasi SK, Inthiyaz S, Prasad GRK, Kumar MS. Comparative analysis of C-element and D-element double edge triggered flip flop for power efficient VLSI applications. AIP Conf Proc. 2024 Jan 22;2512(1):020076. doi:10.1063/5.0112001.
12. Murugesan P, Rajeev SP. Power efficiency evaluation of dual edge triggered flip-flops - A comparative analysis. 2024 7th International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India. 2024. pp. 112–6. doi:10.1109/ICDCS59278.2024.10560917.
13. Rahiminejad M, Saneei M. Low-power pulsed hybrid flip-flop based on a C-element. AEU Int J Electron Commun. 2014;68(9):907–13. doi:10.1016/j.aeue.2014.04.012.

