STM JOURNALS

Recent Trends in
Electronics & Communication Systems

ISSN: 2393-8757
Volume 12, Issue 1, 2025
January–April
DOI (Journal): 10.37591/RTECS

https://journals.stmjournals.com/rtecs

Research RTECS

Noise-Resilient QPSK Modem for Reliable Communication for Green Communication

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Abstract

The channel noise severely degraded the performance of the communication system and that also limits the maximum data transmission rate. Hence, it is required to design a demodulator in a receiver that overcomes the effect of noise in the received signal, reconstructs un-corrupted information signal, and improves data rate. In quadrature phase-shift keying (QPSK), noise affects the phase of the modulated signal and that causes errors in the information signal. This study tackles this crucial issue in the field of communication systems by presenting a noise-free technique for QPSK demodulation. The proposed algorithm compares the received noisy signal with stored sampled values of an ideal signal having signal-to-noise ratios (SNR) of 15 dB to 35 dB that detects the phase of the modulated signal and eventually reconstructs noise-free information signal. The algorithm's performance is thoroughly evaluated, and thorough bit error rate (BER) measurements at different SNR show how successful it is. The proposed QPSK Modem is validated using the open rapid open analog design (ROAD) electronic design automation (EDA) tool with Sky water SKY130HD process design kit (pdk) and *found a maximum operating frequency of 533MHz.*

Keywords: QPSK, digital modulation, MODEM, AWGN, Verilog

INTRODUCTION

Software-defined radio (SDR) is an evergreen technology used with FPGA or programmable System on Chip (Soc) owing to its best features such as flexibility, cost efficiency, and easy upgradation towards future technologies. By employing advanced digital modulation techniques in SDR devices, the system can be either bandwidth- or power-efficient. Various types of digital modulation techniques have been developed, such as amplitude shift keying (ASK), frequency shift keying (FSK), and Phase Shift Keying (PSK). Because PSK is a power-efficient technique, variants of PSKs are used to make it bandwidth efficient, that is, quadrature PSK (QPSK), 8PSK, etc. In these techniques, a greater number of bits are transmitted in the same bandwidth.

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Received Date: December 12, 2024
Accepted Date: December 16, 2024
Published Date: December 25, 2024

Citation: Vagadiya Harsh, Pallavi Darji, Vinay Thumar. Noise-Resilient QPSK Modem for Reliable Communication for Green Communication. Recent Trends in Electronics & Communication Systems. 2025; 12(1): 36–46p.

In real-time, the transmission channel cannot be noiseless. Some types of noise are present on the channel, such as Additive White Gaussian Noise (AWGN), and Brown Noise. This noise affects the communication signal and creates errors. In modulation schemes such as Binary Phase Shift Keying (BPSK) and quadrature phase-shift keying (QPSK), because of noise, the signal will result in a corrupt signal, and the receiver will not obtain the actual data that had been transmitted by the receiver.

According to channel impairment under different conditions, different modulation techniques, such as QPSK, 8PSK, and 16QAM, should be utilized to maintain a sufficient signal-to-noise ratio within a

system. SDR comprises hardware and software in which appropriate modulation techniques have been chosen to optimize the performance of communication systems. It is necessary to implement each technique with minimal hardware and work at a low-power level [1].

QPSK modulation demodulation (MODEM) is used in various applications, such as Cable TV, WiMAX, WLAN, and Satellite communication. A comparator-based method was employed for the demodulation of the QPSK signal, and its test was performed on an Field-Programmable Gate Array (FPGA) board for the best performance. In the 8PSK demodulator, higher performance was achieved with lower FPGA resources. The author implemented a QPSK modulator/demodulator utilizing an SDR with FPGA devices of the ZYNQ family using VHDL and took advantage of available Acorn RISC Machine (ARM) processors in the Xilinx family to improve system performance for a network interface. An efficient QPSK MODEM system was implemented for SDR applications and optimized for speed, area, and power with and without AWGN and Root Raised Cosine (RRC) filters. The system was realized on a Spartan VI FPGA board and found to have low-power and 20% improvement in speed with a reduction in latency compared to other methods [2]. The author proposed a simple approach for the modulation of Quadrature Phase Shift Keying (QPSK). He obtained a digitized carrier wave for QPSK modulation and phase shifting using a 4:1 multiplexer according to the data bits. The design was implemented on a Spartan 3E Xilinx FPGA using Verilog hardware description language.

This paper presents a QPSK modem designed for AWGN channel. Employing the Box-Muller method, the authors generated random noise that was added independently to the in-phase (I) and quadrature phase (Q) channels. Notably, a Raised Cosine filter is applied to smooth the signal and mitigate the inter-symbol interference effects. This comprehensive approach ensures the robust performance of the modem in the presence of channel-induced disturbances, offering a systematic solution for reliable communication in challenging environments [3].

This study focuses on the implementation of QPSK MODEM for error-free reception. This QPSK MODEM was tested on the Open ROAD tool to obtain the final Graphic Data System (GDS) file, which can be considered the final chip.

METHODOLOGY

Career Generation

A high-frequency carrier signal is required to modulate and demodulate low-frequency information signals. RAM-based logic was used to generate this high-frequency sine-wave signal, as shown in Figure 1. For this, 32 different 8-bit values were stored, which were generated through the following MATLAB commands.

T=0 : π/16 : 2π and int(32)=(sint(t)* 1000/28)
fc = clk frequency/64

QPSK Modulation

In the QPSK modulation technique, the digital information signal is partitioned into two distinct segments: In-phase data bits (I-bits) and quadrature phase data bits (Q-bits). These bits are grouped into pairs, forming symbols, where each symbol comprises one I-bit (even) and one Q-bit (odd). This configuration results in four possible symbol combinations: 00, 01, 10, and 11. To transmit these symbols, the carrier signal undergoes a phase shift of 90° based on the incoming symbols, as detailed in Table 1. These principles are visually represented in Figure 2, which employs a decoder and 4:1 multiplexer [4].

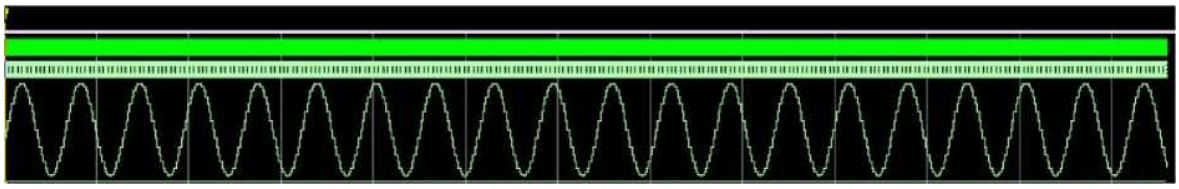


Figure 1. Carrer generation.

The multiplexer's inputs correspond to four high-frequency carrier signals that are phase-shifted by − (90°) with respect to each other [5]. The phase of the carrier signal assumes one of four equidistant values, such as [pi/2, pi, 3pi/2, 2pi] or [pi/4, 3pi/4, 5pi/4, 7pi/4], resulting in two common variants of QPSK: conventional QPSK and ^QPSK, In Figure 3, the modulated QPSK output signal is presented, defined by equations.

s1(t) = ((2E/T)^1/2) (sin(2*pi*fc*t)+ (2i*pi/2))

or

1(t) = ((2E/T)^1/2) (sin(2*pi*fc*t)+ ((2i-1)*pi/4))

Where, i = 1,2,3,4, E is the transmitted signal energy per symbol, T is the symbol duration, \(f_c}\) is the carrier frequency, and t is in the range of \(0\leq t\leq T\).

T= 0: pi/16: 2pi
Fc = clk_frequency/64

The implementation of the conventional QPSK modulation was realized through Verilog HDL coding, and comprehensive simulations were conducted to validate the system. Figure 3 offers an insightful representation of hardware realization, as visualized through Altera Quartus-II. In parallel, Figure 4 presents the modulated QPSK waveform, an outcome of the meticulous simulation performed using the ModelSim simulator. It is worth noting that the requisite phase shifts corresponding to the four-symbol combinations (00, 01, 11, and 10) were precisely engineered to meet the specified operational requirements. This underscores the successful implementation and robust functionality of conventional QPSK modulation schemes.

Table 1. Incoming symbols.

Symbol	00	01	11	10
Phase Corresponding to Symbol	0°	90°	180°	270°

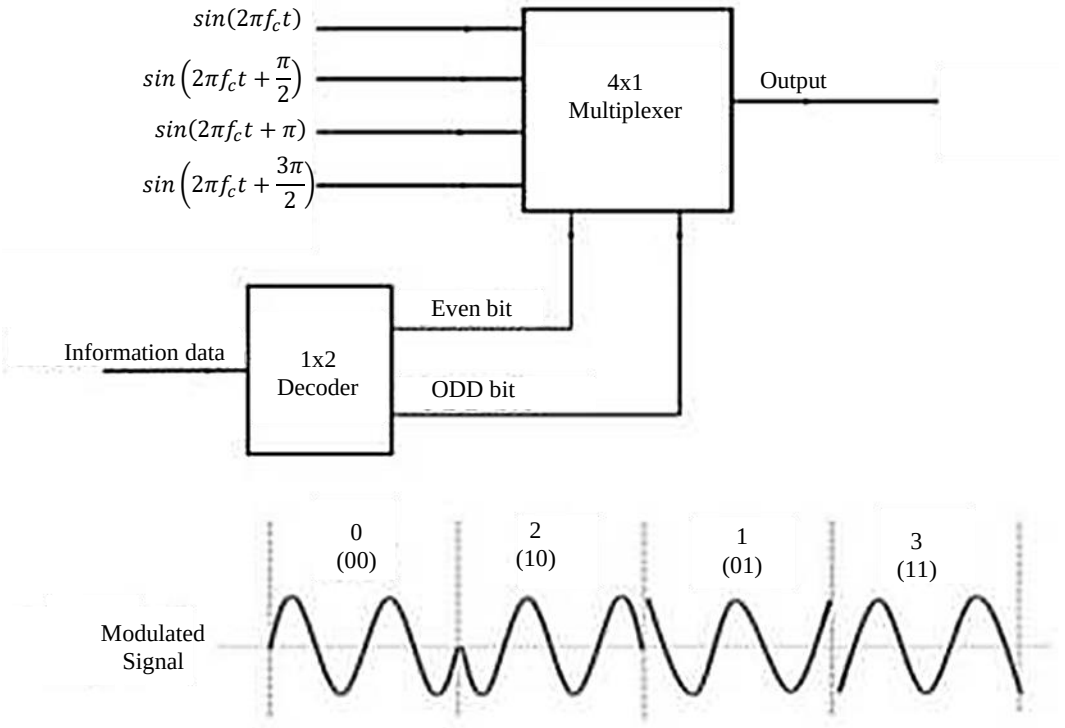


Figure 2. Working flow of the modulator.

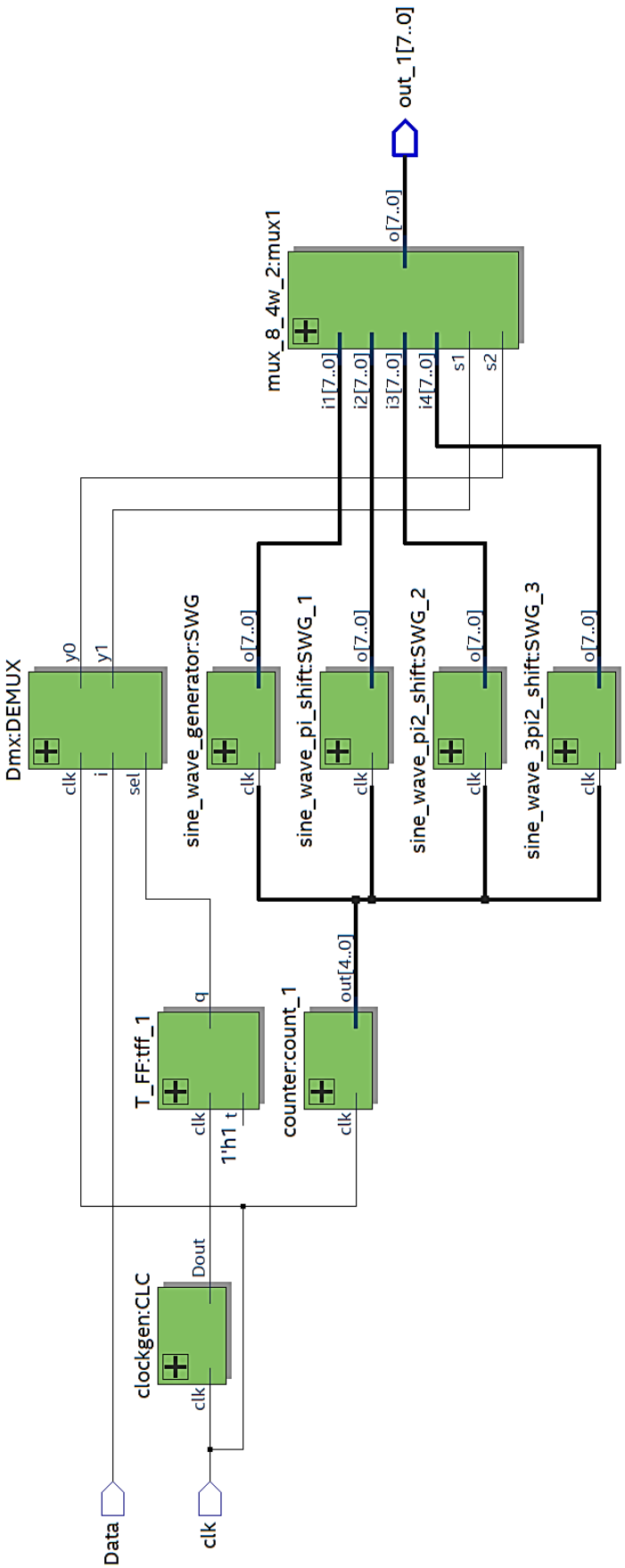


Figure 3. Register Transfer Level (RTL) view of the modulator.

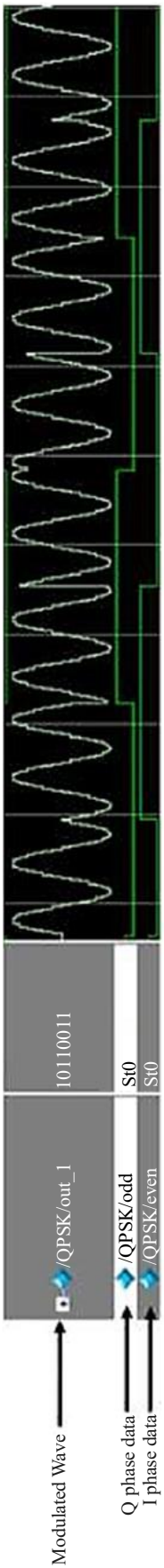


Figure 4. Modulated waveforms.

QPSK Demodulation

To recover the original information from the receiver, a crucial step involves QPSK demodulation. This process requires the multiplication of the received QPSK-modulated signal with specific carrier signals, referred to as its basis functions. In the context of QPSK, two primary basis functions are utilized for this purpose: Q1 = ((1/tb)^1/2) sin (2*pi*fc*t) and Q2 = ((1/tb)^1/2) cos (2*pi*fc*t) Each basis function is strategically employed to disentangle a pair of symbols.

Practical implementation involves the multiplication of the received signal with the respective basis functions using specialized multipliers, as illustrated in Figure 5. The phase detector plays a pivotal role in determining the received symbol [6]. The outcomes of this phase detection, corresponding to odd and even bits, were subsequently merged using a multiplexer. This orchestrated process ultimately leads to the retrieval of the original information signal, which is a critical step, as depicted in Figure 6. The combination of these operations forms an integral part of the QPSK demodulation, enabling faithful reconstruction of the transmitted data.

The QPSK demodulator was meticulously implemented using Verilog HDL, and its functionality was thoroughly assessed. Figure 5 provides a visual representation of the RTL view, offering insight into the underlying modules and their interconnections [7]. This demodulator encompasses various stages, commencing with the generation of carrier signals, followed by multiplier modules that play a pivotal role in the demodulation process. The subsequent modules are dedicated to symbol detection, facilitating the extraction of even and odd bits and culminating in the successful retrieval of the original information signal. This visualization underscores the systematic extraction of the original signal from the received QPSK-modulated signal, primarily achieved through the in-phase and quadrature phase signals acquired after the multiplier modules. It is worth noting that this demodulation process introduces some delays owing to the inherent characteristics of the multiplier and multiplexing operations, as observed in the signal waveform. This delay is a fundamental aspect of the demodulation process and is critical for faithful signal reconstruction.

PROPOSED NOISE-PROOF QPSK DEMODULATOR

In the demodulation process of a QPSK modem, the signal passes through a sequence of steps. Initially, it is sampled using an ADC, followed by multiplication with basic functions to separate the in-phase and quadrature components. A digital filtering stage was employed to enhance the signal quality and mitigate the noise. The final step in this process is phase detection, which ultimately unveils the transmitted symbol [8]. However, the use of digital filters introduces additional computational complexity involving operations such as multiplication and addition. Striking the correct balance between signal fidelity and system complexity is crucial for efficient and reliable communication.

The previous simulation of the QPSK modem was conducted under the simplifying assumption that the communication channel is devoid of noise and that the system operates in a coherent fashion. However, such ideal conditions are rarely encountered in practice [9]. Communication channels are invariably affected by various types of noise, such as additive, black, pink, and flicker noise, all of which can significantly degrade the quality of the received signal \cite{b19}. Therefore, the signal reaching the receiver's input is inherently noisy, and it is imperative to account for these noise sources when designing and evaluating communication systems. This discrepancy between the pristine theoretical model and real-world noisy channel conditions underscores the need for robust and effective signal-processing techniques to ensure reliable data transmission in the presence of such impairments.

To extract the original information signal from the noisy modulated signal, a noise-free QPSK demodulator is proposed. The phase detection module is shown in Figure 5 was modified, as shown in Figure 8. The noisy modulated signal is amplified and converted into a digital signal using an analog-to-digital converter (ADC). The sample digital signal from the ADC was available at the input of the demodulator.

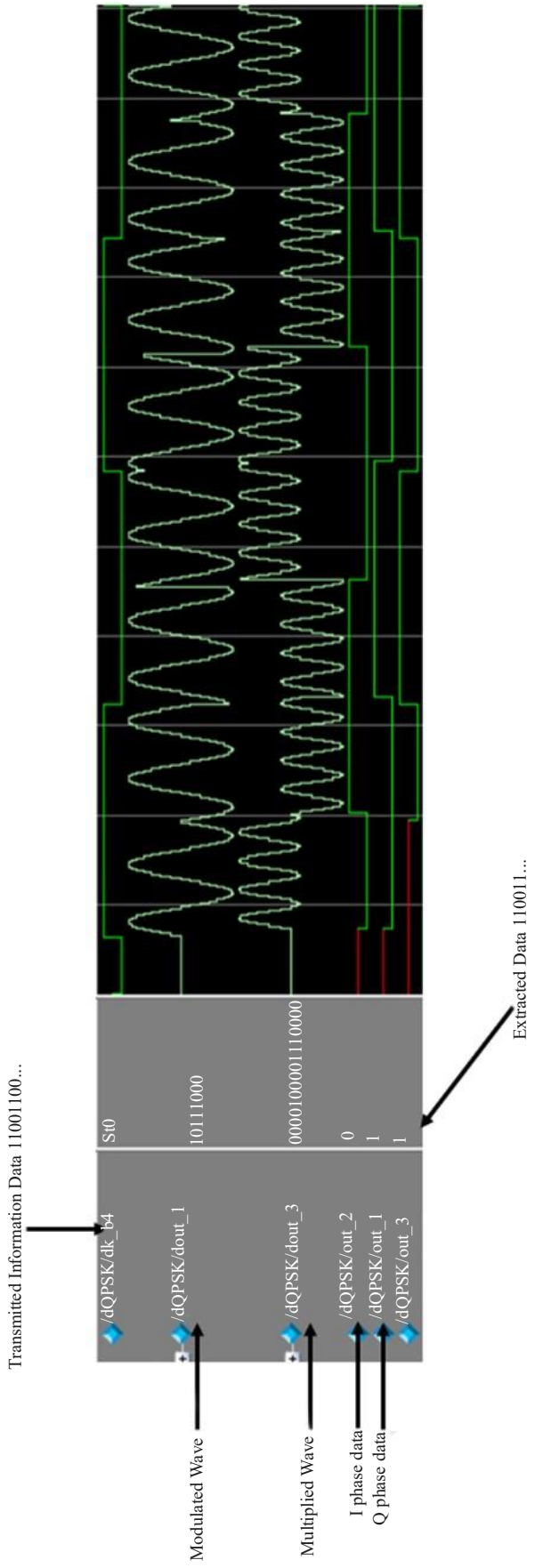


Figure 5. Register Transfer Level (RTL) view of demodulator.

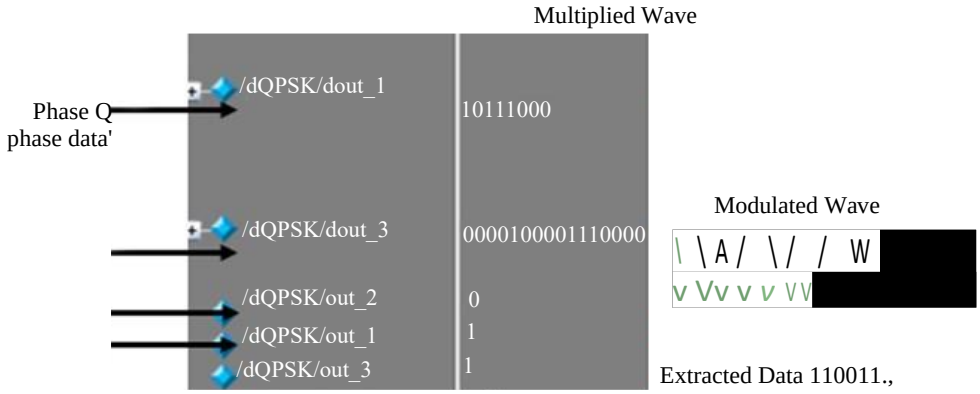


Figure 6. Simulation results of QPSK demodulation.

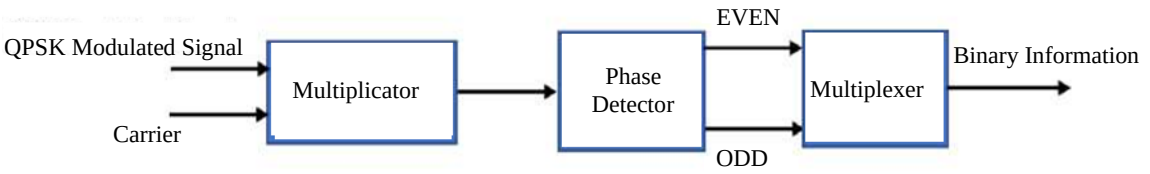


Figure 7. Working flow of demodulator.

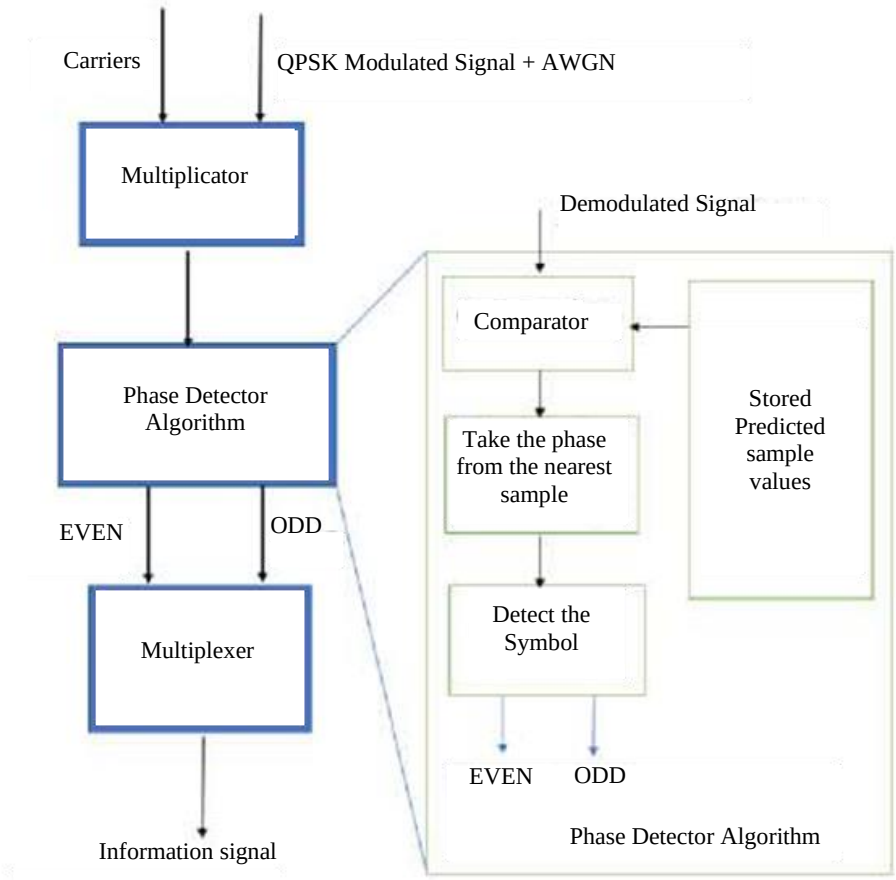


Figure 8. Working flow of the proposed demodulator.

The multiplicative module multiplies the sampled signal with a carrier signal for demodulation, as shown in Figure 8. The output of this module was compared with the predicted noise signal samples

stored in memory. From the comparison, it takes the phase of the nearest predicted sample value and identifies the phase symbol, as per Table 1. Odd and even bit streams are generated from these symbol signals and applied to the multiplexer module to extract the original information signal [10].

In a demodulator system, the first critical component is the ADC. The noise was introduced into the signal during the transmission through the channel. As the analog signal is sampled by the ADC, noise becomes an intrinsic part of the signal. To illustrate, let us consider a scenario where an 8-bit ADC is employed, and the signal is expressed in millivolts. This implies that noise in the microvolt range may be effectively filtered out during the sampling process. However, noise in the millivolt range can potentially introduce errors in the signal.

In Section 3, we delve into carrier generation in Subsection A of the discussion. This section explores the concept of noise-free channels, in which we can reliably obtain samples of the carrier waveform and calculate the differences between consecutive samples.

In general, wireless channels with signal-to-noise ratios (SNR) in the range of 15–35 dB are considered to be favorable for communication. Within this range, we introduced noise of specific magnitudes into the modulated signal, which was then sampled at the demodulator. This process enabled us to obtain the sample values of the signal with a defined SNR.

For instance, when a signal arrives at the demodulator with a signal voltage of 37.33 millivolts, it can be approximated as 38 millivolts. Numerous noise possibilities exist within the signal, summing up to a total voltage of 38 mV. However, other parameters, such as the data rate, previous sample values, and subsequent sample values, come into play. These parameters aided in determining the most appropriate sample for the signal under consideration. This meticulous analysis helps ensure the accurate reception and decoding of transmitted information, even in the presence of noise.

This noise-modulated signal is shown in Figure 9. It looks like a modulated wave only, but its peaks and average value change after the addition of noise. The BER was calculated using numbered all equation.

$$BER = (1/t)/Tb$$

Where,

t = time when the error occurs and

T_b = Period of the 1-bit information signal.

An RTL view of the noise prototype QPSK demodulator is shown in Figure 10. It shows more utilization of resources on FPGA compared to conventional QPSK demodulators because of the requirement to store samples of the carrier signal with different DC values to recover the information signal from the noisy modulated signal.

Figure 11 illustrates the bit error rate (BER) performance across various SNR. The data reveals that the performance of the NP-QPSK demodulator aligns with predefined requirements, as documented in reference [10]. Note that Radio Frequency (RF) amplifiers are positioned upstream of the modulation block. In this configuration, when a signal contains noise, the amplifiers amplify the noise components. Conversely, in the absence of noise, the signal exhibits minimal power.

Figure 9. Noisy signals.

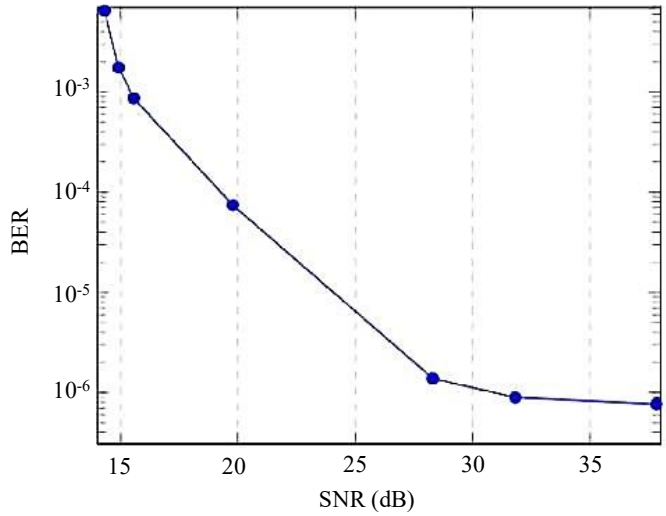
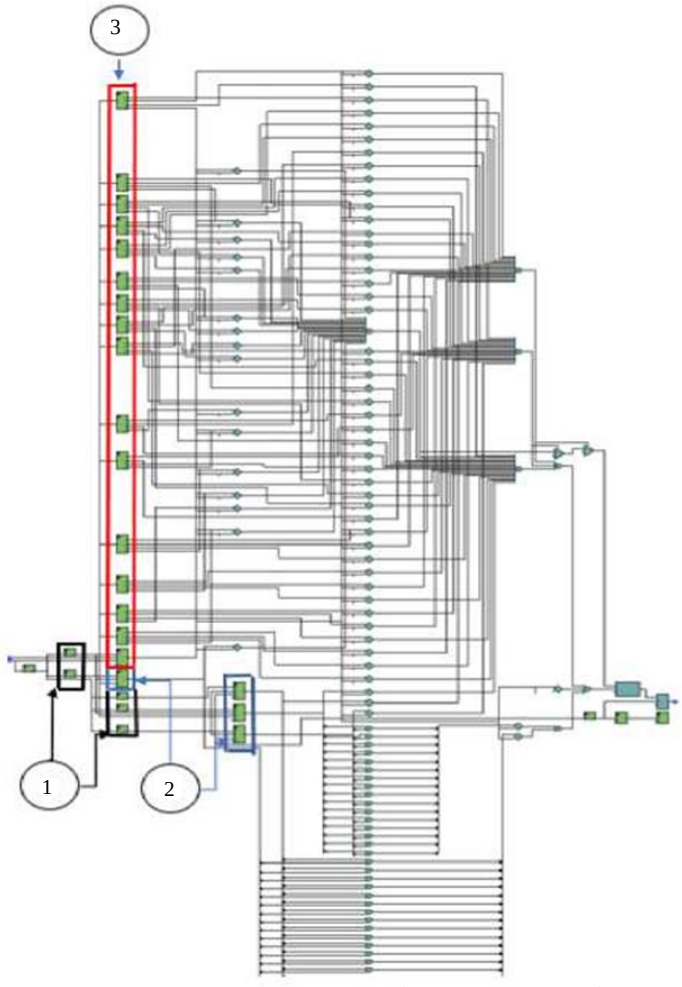


Figure 10. SNR vs BER Graph.



1. Modules that are generating carriers for the demodulation of signal.
2. Multiplier blocks for demodulator.
3. Modules that have samples for noise detection.

Figure 11. RTL view of the proposed demodulator.

As shown in Figure 11, the maximum error rate was observed at an SNR of 15. This SNR level corresponds to the highest signal power, equivalent to the signal power plus the noise component, which

Table 2. Different system analysis.

Technology	System	fmax (MHz)
SKY130HD	QPSK M	587
	QPSK DM	554
	NP-QPSK DM	533

accounts for approximately 20 percent of the signal power. This observation underscores the interplay between signal power and noise, and how variations in the SNR affect the overall performance of the system. The performance parameters, as detailed in Table 2, were meticulously evaluated using the Open ROAD open-source electronic design automation (EDA) tool, employing sky130hd technology to ascertain the system's suitability for high-frequency operations. The results highlight a distinct order in operating frequencies, with the QPSK modulator exhibiting the highest operating frequency, followed by the conventional demodulator and noise-proof demodulator.

This observed hierarchy in the operating frequencies is primarily attributed to the complexity of the system design. Notably, the noise-proof QPSK demodulator emerges as the most intricate among the three and consequently operates at a comparatively lower frequency. In contrast, the QPSK modulator, which is characterized by its relative simplicity, achieves the highest operating frequency. This distinction underscores the intricate balance between design intricacy and operational performance, with the QPSK modulator emerging as the most adept at high-frequency operations.

CONCLUSION

The successful implementation of the Conventional QPSK MODEM demonstrated its ability to reliably recover information bits at the demodulator end, ensuring the integrity of the transmitted data. In contrast, the proposed noise-proof (NP) QPSK demodulator, which is effective in enhancing the demodulation performance in noisy conditions through parallel noise sample comparisons, necessitates a larger hardware footprint, consequently limiting the operating frequency. Notably, noise-proof QPSK MODEM exhibits commendable BER performance in the presence of AWGN. Both Conventional and Noise-Proof MODEMs were validated for high-frequency operation using the Open ROAD open-source EDA tool in conjunction with the sky130HD process design kit (pdk). The discernible difference in the maximum operating frequency between the Conventional and Noise-Proof demodulators is primarily attributed to the sampled matching algorithm, and the introduction of a digital filter in the noise-proof demodulator would likely exacerbate these disparities because of its increased computational complexity. This work not only advances the understanding of QPSK modulation and demodulation but also highlights the intricate balance between design complexity and high-frequency performance.

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