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Performance Analysis of Schmitt Trigger Circuit for Noise-free Chips

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Abstract

At lower nodes of complementary metal-oxide semiconductor (CMOS) technology, noise within a chip increases due to a drastic increment in interconnects within a given area. To improve the noise immunity of a chip, a Schmitt trigger circuit is used as a buffer instead of a simple CMOS inverter at various intervals along the metal interconnect. The use of a Schmitt trigger circuit not only makes the chip noise immune but also increases the speed of operation. Different typologies of Schmitt trigger circuits, such as 4T, 6T, and 6T with body-bias, are studied, implemented, and analyzed based on speed, area, power, and hysteresis. Since there is a trade-off between these parameters, the power-delay product (PDP) is determined, and the best one will be chosen as per the requirement. The Schmitt trigger circuit is also used in IO pads surrounding the chip and in a bidirectional bus as a tristate buffer in a communication system. The 4T Schmitt trigger is found to be 82% lower PDP compared to the conventional 6T Schmitt trigger circuit. Modern electronics have become more susceptible to noise due to the shrinking of components and the growing complexity of integrated circuits. This can cause irregular behavior and a deterioration in signal integrity. One common remedy for noise-related problems is the Schmitt trigger circuit. By supplying hysteresis, it guarantees steady signal processing and eliminates undesired noise in digital systems. Schmitt trigger circuit design, functionality, and performance are examined in this article, with a focus on their use in the production of noise-free semiconductors.

Keywords: CMOS, Schmitt trigger, power, hysteresis, propagation delay, noise, buffer

INTRODUCTION

The Schmitt trigger, a crucial component in electronic circuits, is significant owing to its unique characteristics, namely, power efficiency, noise immunity, and high-speed operation. Power efficiency is paramount in modern electronics, and the Schmitt trigger excels in this aspect by consuming minimal power during its operation, thereby contributing to energy-efficient designs. Noise immunity, which is another critical attribute, refers to the ability of a circuit to reject or tolerate external interference. The Schmitt trigger's hysteresis feature ensures robust noise immunity, enhancing the reliability of electronic systems in noisy environments. Furthermore, the high-speed operation of the Schmitt trigger is invaluable in applications demanding rapid response times. Its ability to switch states quickly makes it suitable for applications in which signal transitions need to be detected promptly, ensuring efficient and accurate processing of electronic signals. Whether employed in digital communication, signal processing, or control systems, the Schmitt trigger's combination of power efficiency, noise immunity, and high-speed performance makes it a versatile and indispensable

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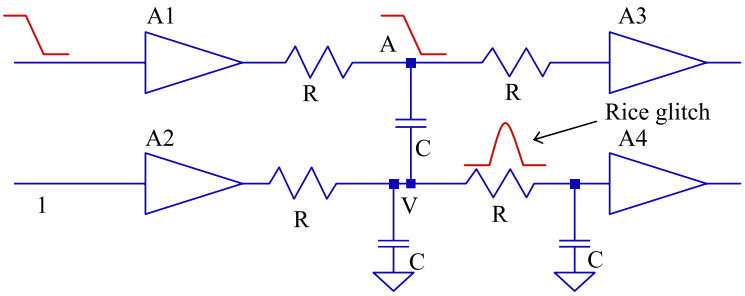

Figure 1. Occurrence of glitch.

component in modern electronics and plays a pivotal role in the reliable and efficient functioning of electronic circuits across various applications.

Furthermore, shrinking transistor sizes increases the number of transistors within a chip area, while simultaneously leading to a progressive increase in interconnect lines. This increase in metal interconnect lines also raises the occurrence of crosstalk, which may result in signal-level fluctuations. Figure 1 illustrates a glitch caused by the crosstalk between the two metal lines. This shows that the two metal interconnects, with buffers A1 and A3, and A2 and A4, respectively, run in parallel, while the metal lines are depicted with the equivalent RC circuit [1–4]. Owing to the capacitance formed between the metal lines, as depicted in Figure 1, the signal couples from point A to point V, generating a glitch at the input of A4, potentially flipping its signal level. This could compromise the signal transmission through the interconnect, leading to chip failure. To address this issue, buffers or inverters with Schmitt triggers can be employed to prevent unnecessary transitions caused by glitches [5].

In this study, various CMOS-based Schmitt trigger (ST) circuit designs were implemented and evaluated using the LTSpice simulator with 180 nm CMOS technology. The implementation of 4T, 6T conventional, and 6T with body bias Schmitt trigger circuits is detailed in Section II. The simulation and corresponding results, along with discussions, are presented in Section III. Section IV provides a comparison of the performance parameters for these circuits, and conclusions are drawn in Section V.

IMPLEMENTATION

A conventional 6T Schmitt trigger [2] comprises two inverters and two output transistors, as shown in Figure 2. It is composed of two sub-sections, section 1 and section 2, where section 1 represents the PMOS circuitry consisting of three PMOS transistors M1. M2 and M5, which are responsible for the generation of the lower threshold switching voltage V_L; Section 2 represents the NMOS circuitry consisting of three NMOS transistors M3, M4, and M6, which are responsible for the generation of the upper threshold switching voltage V_U [6–10]. The hysteresis voltage, V_H, is the difference between V_U and V_L. The higher the voltage, the better the noise immunity. The PMOS M6 and NMOS M5 transistors relate to the output to provide positive feedback for eliminating unwanted noise signals from the output when the changes in the amplitude of the input signal are not more than the switching threshold voltage difference.

A 4T Schmitt Trigger circuit with a reduced number of transistors, as shown in Figure 3, was implemented to improve the performance parameters. It is composed of four transistors: M1, M2, M3, and M4; out of which transistor M4 was used to provide positive feedback. As this modified circuit has a smaller number of transistors in the P-section, the overall delay and power dissipation of the circuit were reduced compared to the conventional CMOS Schmitt trigger circuit.

The third Schmitt trigger circuit with body bias variation [2] was implemented as shown in Figure 4. The circuit is composed of two sub-sections, that is, section-1 and section-2, where section-1 is composed of two transistors $M1,_P$ and $M1,_N$, and section-2 is composed of two inverter circuits ($M2,_P$, $M2,_N$, $M3,_P$, $M2,_N$), in which the body bias voltages of $M2,_P$, $M2,_N$ is are controlled for adjusting

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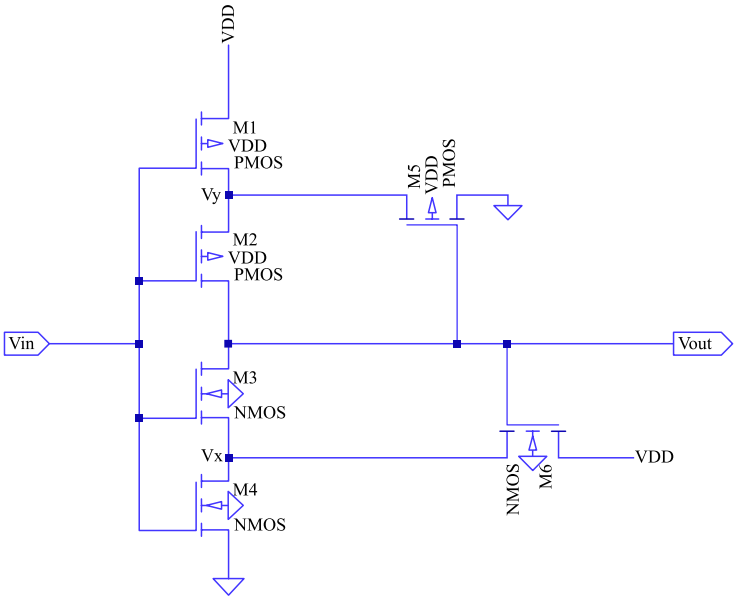

Figure 2. Conventional 6T Schmitt trigger.

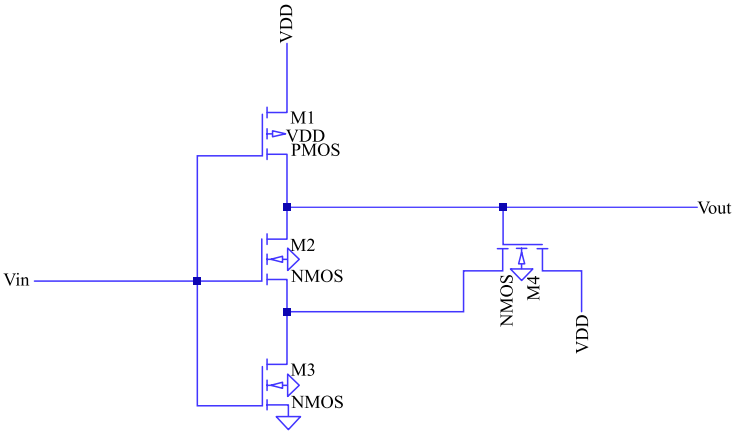

Figure 3. 4T Schmitt trigger.

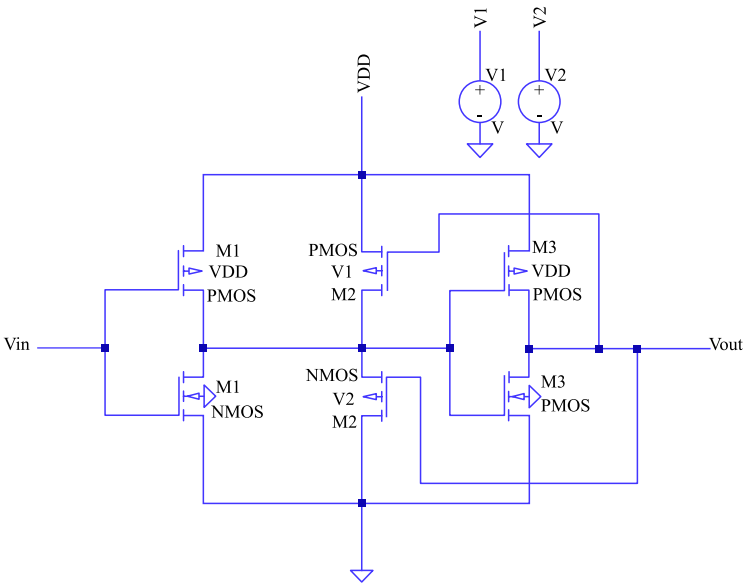

Figure 4. 6T body bias Schmitt trigger.

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the threshold voltage V_L and V_U of the circuit and controlling the switching of the output in order to minimize the propagation delay of the circuit. In addition, by controlling the body bias voltage, the width of the hysteresis loop is adjusted, making it suitable for applications requiring variable noise immunity.

The operation of the body-biased Schmitt trigger is as follows. As the implemented circuit behaves as a buffer, when the voltage at the input terminal is low, that is, when V_m is low, the voltage at the output terminal also decreases, that is, V_{out} is also low; thus, the CMOS transistors M1,n, M3, and n operate in the cut-off region and the transistors M1,p, M^ operate in the saturation region. However, when the input is transitioning from low to high, transistor M1, n is turned on and the voltage at the intermediate node decreases as it is dropped down to the ground through transistor M1,n.

The voltage at the node is used to control the switching at the output terminal, that is, V_{out}, because the voltage V2 at the body terminal of M3,p is used to set out the threshold voltage of M3,p; thus, it helps in switching the output with a smaller propagation delay. When transistor Mi,n is in the saturation region, the current through transistor Mi,n is equal to the current through transistors M1,p, and M3,p. Similarly, when the voltage at the input terminal is high, that is, when the input increases, the voltage at the output terminal is also changed to a voltage level equivalent to the voltage at the input terminal, that is, the output also increases, because of which transistors Mi,p, M3, and p operate in the cut-off region and Mi,n, M3, and n operate in the saturation region. However, when the input is changed from high to low, transistor M1, p is turned on and the voltage at the node increases as it is dropped up to VDD through transistor Mi,p. The voltage at the node is used to control the switching at the output terminal, that is, V_{out}, as the voltage V3 at the body terminal of M2, n is used to set out the threshold voltage of M2,n, thus helping switch the output with a smaller propagation delay. When transistor Mi,p is in the saturation region, the current through transistor M1,p is equal to that through transistors M1,n and M3,n. It is observed that body bias voltages are used to control the switching action of the output voltage, thus changing the delay of the circuit. As in this case, the body-biasing voltages are chosen such that we obtain the minimum possible value of the delay. In addition, by controlling the voltages at the body terminal of transistors M2,p, and M2,n, the width of the hysteresis loop is adjusted, thus making it suitable for applications requiring variable noise immunity. Optimizing these factors allows designers to balance the speed, power consumption, and reliability for tailored circuit operation across different conditions and applications.

Design for Hysteresis Voltage V_H

To obtain the desired hysteresis voltage, the aspect ratio for each transistor was selected such that it operates in the saturation region. In a conventional 6T Schmitt trigger circuit transistors M1, M2, M3, and M4 in Figure 2 behave as simple inverters. When the input voltage (V_{in}) is low, the upper PMOS transistors conduct, allowing a path for the supply voltage (VDD) to reach the output, resulting in a high output. Conversely, when V_m is high, the lower NMOS transistors conduct, providing a discharge path, leading to a low output.

When transistors M2 and M5 are added, they help control things. When V_{in} (input voltage) is low, the output is high. Subsequently, M5 kicks in, ensuring that the upper circuit remains strong. This pushes the inverter's performance slightly to the right, as shown in Figure 5 (top-left curve). Similarly, if V_{in} is high, making the output low, M2 steps to keep the lower circuit strong, pushing the performance slightly to the left. This back-and-forth creates a loop (like a curve) that is important for keeping things stable and free from interference, as shown in Figure 5 (bottom curve).

When V_{in} switches from low to high, Mi conducts, and the potential difference between V_{in} and node Vx changes. At that instant, because the output is high, transistor M5 is saturated. Hence, the saturation current equation is utilized to equate the currents flowing through Mi and M5, which provides a design equation for the Vth upper transition point. Similarly, when V_{in} decreases, causing V_Y to increase and M4 to turn on, the output changes from low to high. The saturation current equations for M4 and M2 are equated to determine the Vtl-Lower transition point.

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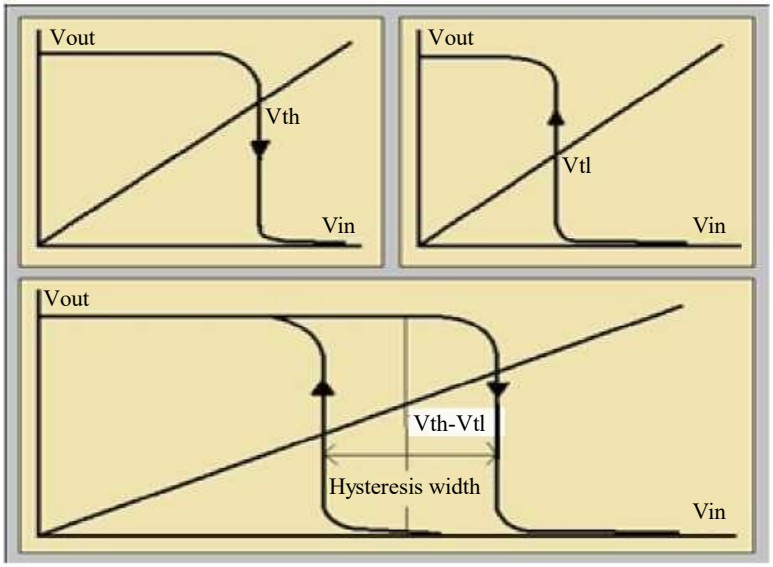

Figure 5. Hysteresis loop of inverter.

$$\frac{k1}{2}(Vin - Vthn)^2 = \frac{k5}{2}(Vdd - Vx - Vthn)^2$$

$$\frac{k4}{2}(Vdd - Vin - Vthp)^2 = \frac{k6}{2}(Vy - Vthp)^2$$

By solving these equations, the threshold voltages, Vth and Vtl, were calculated, providing critical parameters for understanding the behavior of the circuit and ensuring the desired hysteresis width.

$$V_{th} = Vdd + Vthn\left(\frac{\sqrt{\frac{k1}{k5}}}{1+\sqrt{\frac{k1}{k5}}}\right)$$

$$V_{tl} = \frac{\left(\sqrt{\frac{k4}{k6}}\right)(Vdd - Vthp)}{1+\sqrt{\frac{k4}{k6}}}$$

$$V_H = V_{th} - V_{tl}$$

Where, k is the trans-conduction parameter of the MOSFET, and the relationship between the individual k for the NMOS and PMOS transistors is given by

$$Kr = \frac{Kn}{Kp} = \frac{\mu nCox\left(\frac{w}{l}\right)n}{\mu pCox\left(\frac{w}{l}\right)p}$$

Where, *Kn* and *Kp* are the trans-conductance of NMOS and PMOS transistors respectively.

Using the above equations, the W/L ratio for the conventional 6T Schmitt trigger circuit was obtained for 180 nm CMOS technology, and a threshold voltage VH of 0.6 V. Table 1 shows the sizing of transistors used in Figure 2.

- *Pn* and *pp* are the electron mobilities of NMOS and PMOS transistors respectively.
- *Cox* is the oxide capacitance.

Where (Y) *n* and (Y) *p* are the width-to-length ratios of the NMOS and PMOS transistors, respectively.

Table 1. Sizing transistors in 6T conventional Schmitt trigger.

Parameters	Mi (PMOS)	M2 (PMOS)	M3 (NMOS)	M4 (NMOS)	M5 (PMOS)	M6 (NMOS)
Width	200 nm	200 nm	200 nm	200 nm	200 nm	200 nm
Length	600 nm	600 nm	900 nm	900 nm	1200 nm	1800 nm

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SIMULATION RESULTS

Conventional 6T, 6T body bias, and 4T circuits were simulated using an LT Spice simulator with 180 nm technology. A transient analysis of these three circuits was performed, and the obtained output results are shown in Figure 6. This shows that the conventional 6T and 4T Schmitt trigger circuits act as inverters, as shown in Figure 6(a), because V_{out} is inverted of the input signal V_{in}, whereas in 6T body bias, the Schmitt trigger circuit V_{out} is the same as V_{in}, the high voltage level for the positive half cycle, and low for the negative half cycle, as shown in Figure 6(b).

Hysteresis Width Analysis

The obtained hysteresis voltage V_H for these three ST circuits have been shown in Figure 7 and listed in Table 2. It is found that 4T ST has minimum V_H while it is more and adjustable in 6T-body bias ST. In 6T body bias ST, V_H can be easily controlled by body bias voltages.

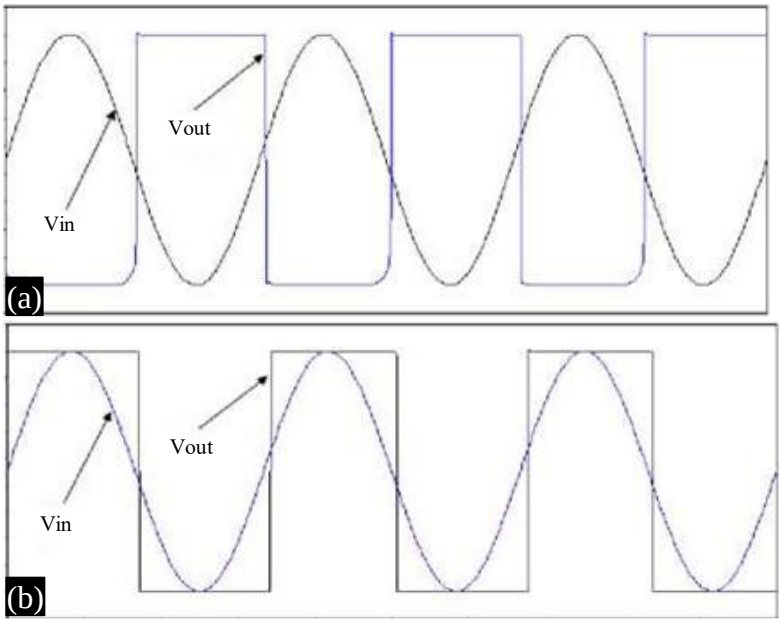
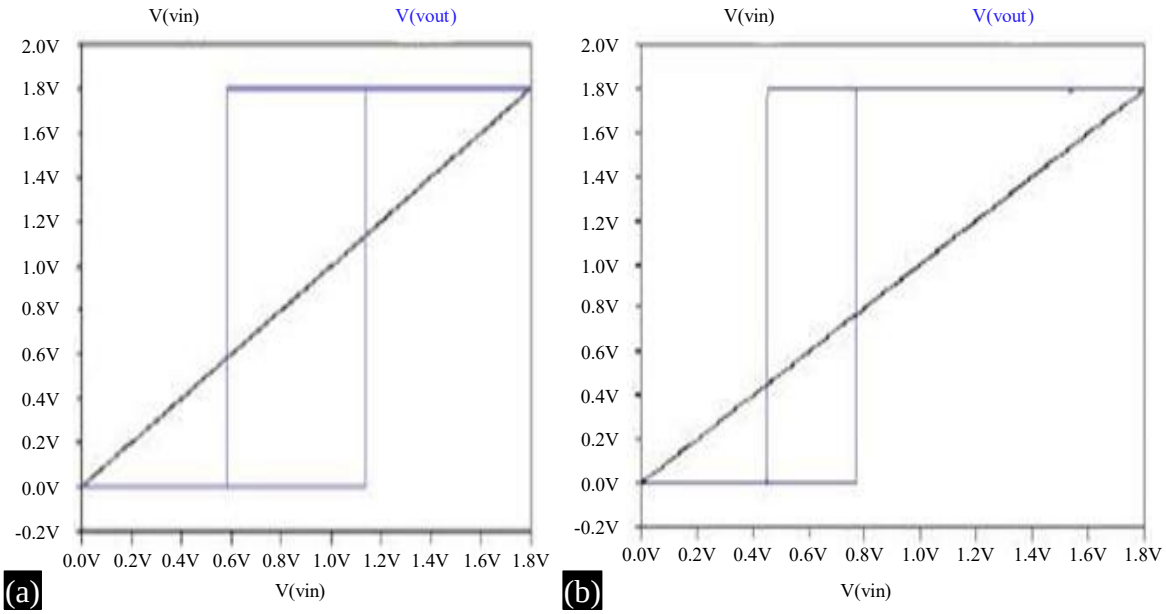


Figure 6. Transient analysis of Schmitt trigger, (a) 6T and 4T Schmitt trigger, (b) 6T Body Bias Schmitt trigger.



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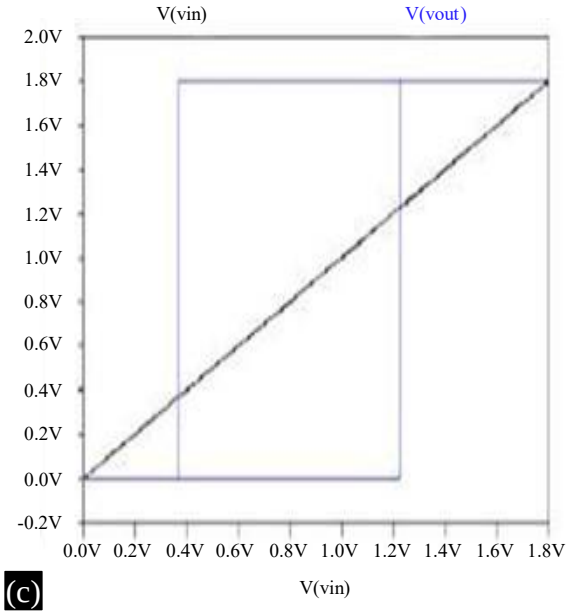


Figure 7. Hysteresis width of Schmitt trigger circuit, (a) Conventional 6T-ST, (b) 4T-ST, (c) 6T-Body bias-ST.

Table 2. Performance parameters of Schmitt trigger circuits.

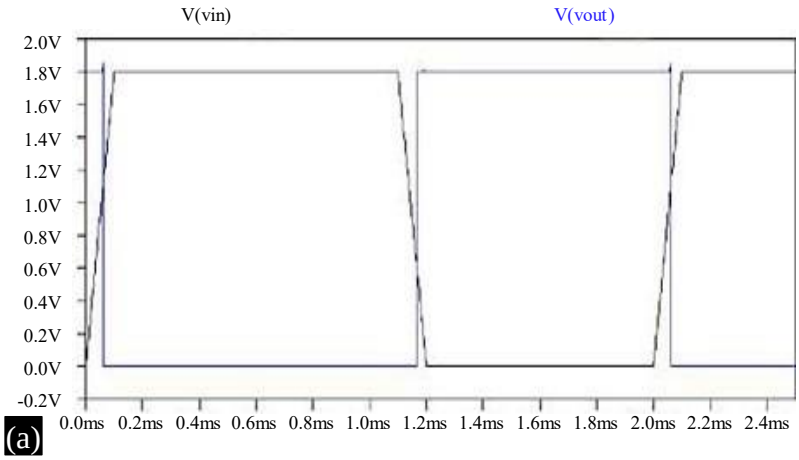
Type of Schmitt trigger	Hysteresis width	Propagation delay	Power consumption
4T	290.45772 mV	0.159 ns	8.4031 pW
6T	639.56555 mV	0.412 ns	17.736 pW
6T Body Bias	977.26218 mV	0.269 ns	7.2321 pW

Propagation Delay Analysis

Propagation delay (PD) was measured at 50% of the input and output signal transitions, and Figure 8 shows its measurement. The corresponding values for each topology are listed in Table 2. It was found that the 6T conventional has a higher PD than the others owing to the presence of more transistors at the output node.

Power Dissipation Analysis

The main advantage of CMOS-based circuits is minimum static power dissipation because, for a given square-wave signal, only the NMOS or PMOS transistor will be turned on, but the dynamic power dissipation depends on the switching activity, as shown in Figure 9. The higher the operation frequency,



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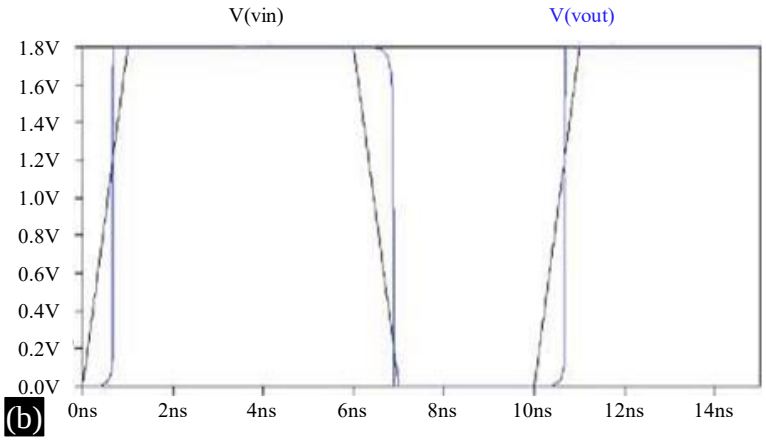

Figure 8. Propagation delay, (a) 6T and 4T Schmitt trigger, (b) 6T Body bias Schmitt trigger.

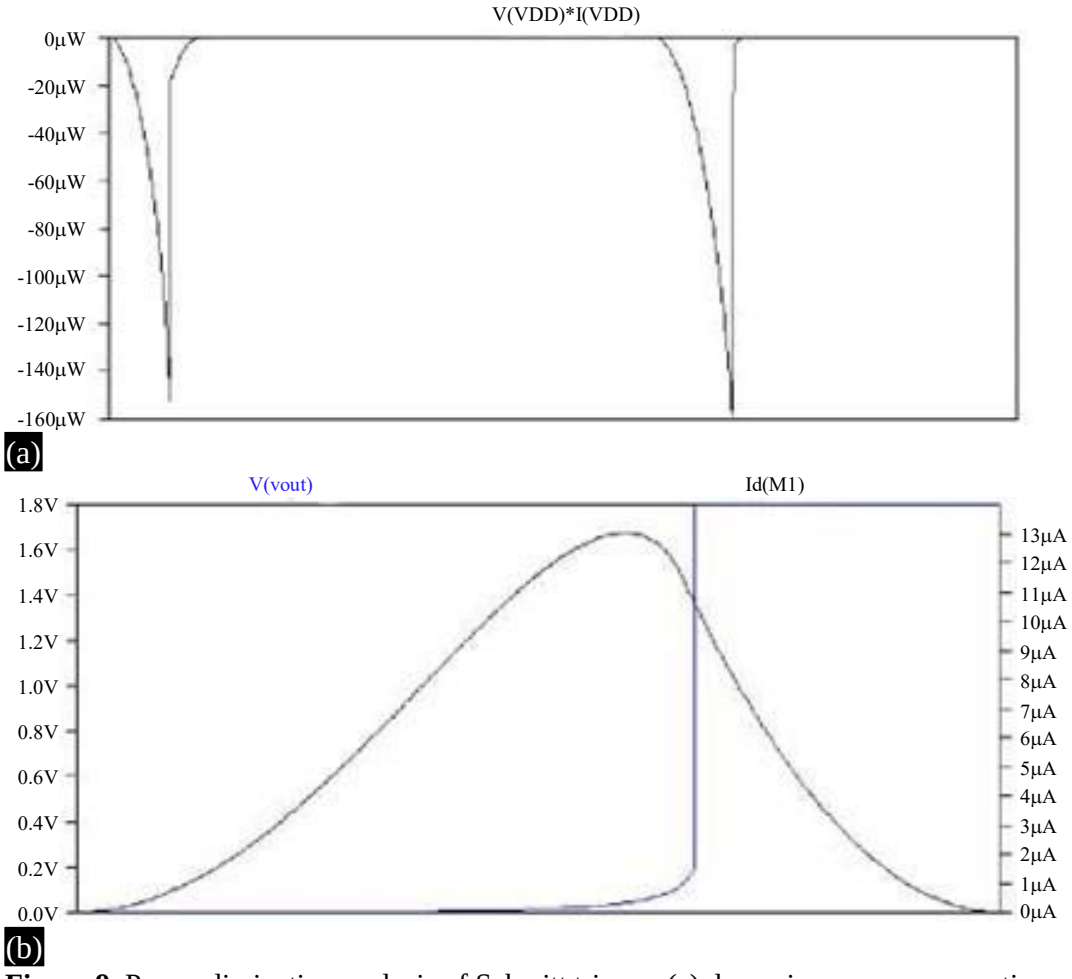

Figure 9. Power dissipation analysis of Schmitt trigger, (a) dynamic power consumption, (b) static power consumption.

the higher the dynamic power dissipation. The total power (P_{Total}) is given by the sum of the static power (P_{Static}) and dynamic power (Pn^mO.) expressed by the equation:

$$P_{Total} = P_{Dynamic} + P_{Static}$$

••• *Total Power = Pst + Pdy = 9.73pW + 8.50 pW = 8.50 pW*

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The power is given by the product of the voltage and current. Figure 9(a) shows the multiplication of V(VDD)*I(VDD) for a 100 MHz square wave signal, and its average gives a dynamic power dissipation of 8.50 pW. Figure 9(b) shows a static power dissipation of 9.73 pW. The power dissipation calculation was performed for these three typologies and is presented in Table 2.

Comparison with Prior Work

The carried-out work is compared with other available topologies and tabulated in Table 3. For fare comparison. The power-delay product (PDP) was evaluated. This serves as a crucial figure of merit in circuits, as measured by the energy consumed per switching event. In any circuit, a low-PDP is desirable, as it indicates efficiency. Table 3 presents the 4T Schmitt trigger circuit that significantly minimizes this metric in comparison with the traditional circuit. This observation underscores the potential advantages of the 4T ST circuit in terms of energy efficiency and overall performance.

Table 3. Comparison with prior work.

Schmitt trigger	Hysteresis width (mV)	Propagation delay (ns)	Total power consumption (pW)	Power-delay product (fJ)
4T	290.46	0.159	8.40	1.34
6T	639.57	0.412	17.74	7.31
6T Body Bias	977.26	0.269	7.23	1.94
$6T^2$	660.34	--	57.5	--
$6T^3$	487	0.960	11.05	10.61

CONCLUSION AND FUTURE SCOPE

Various topologies of the Schmitt trigger circuit, such as 4T, conventional 6T, and 6T with body bias, have been evaluated because of their wide application as buffers at the chip level. The hysteresis voltage of the Schmitt trigger circuit with a body bias can be easily adjusted by changing the bias voltage. Different noise levels may occur at various places within a chip, and this capability facilitates the design of buffers with different voltage hysteresis (V_H) suitable for different noise environments. The simulation results also indicate that the 4T Schmitt trigger circuit exhibits an 82% lower PDP than the conventional 6T Schmitt trigger circuit. However, its low hysteresis voltage limits its applicability to different levels.

These topologies can be used as tristate buffers to evaluate the performance of bidirectional voltage level shifters, voltage-controlled oscillators, peak detector circuits, frequency synthesis in communication systems, pulse width modulation (PWM) control, and time delay circuits.

REFERENCES

1. Kumar KVLP, Prabhakar VSV, Bhavani MD, Geetha K, Venkatesh M, Hari Kishore K. Design and analysis of CMOS Schmitt trigger. Int J Innov Technol Explor Eng. 2019 May;8(7S):106–9.
2. Khanna B, Gupta R. Design, implementation and analysis of different models of CMOS Schmitt trigger. Int Conf Intell Circ Syst ICICS. 2018;63–8. DOI: 10.1109/ICICS.2018.00025.
3. Kumawat K, Ajnar DS, Jain PK. Design and analysis of noise immune high-speed and leakage-tolerant Schmitt trigger using 180nm CMOS technology. IEEE Madras Sect Conf MASCON. 2021;1–5. DOI: 10.1109/MASCON51689.2021.9563581.
4. Goka KR, Saini LM. Comparative analysis of CMOS Schmitt triggers. 2023 3rd Int Conf Mob Netw Wirel Commun ICMNWC. 2023;1–5. DOI: 10.1109/ICMNWC60182.2023.10435839.
5. Pasini Melek LA, da Silva AL, Schneider MC, Galup-Montoro C. Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation. IEEE Trans Circ Syst I. 2017;64:869–78. DOI: 10.1109/TCSI.2016.2631726.
6. Elmezayen MR, Hu W, Maghraby AM, Abougindia IT, Ay SU. Accurate analysis and design of integrated single input Schmitt trigger circuits. J Low Power Electron Appl. 2020;10:21. DOI: 10.3390/jlpea10030021.

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7. Joseph JS, Shukla R, Niranjan V. Performance evaluation of low voltage Schmitt triggers using variable threshold techniques. 4th Int Conf Reliab Infocom Technol Optim ICRITO. 2015;1–5. DOI: 10.1109/ICRITO.2015.7359347.
8. Saini S, Veeramachaneni S, Kumar AM, Srinivas MB. Schmitt trigger as an alternative to buffer insertion for delay and power reduction in VLSI interconnects. TENCON IEEE Reg 10 Conf. 2009;1–5. DOI: 10.1109/TENCON.2009.5396104.
9. Niranjan V, Gupta M. An analytical model of the bulk-DTMOS transistor. J Electron Devices. 2010;8:329–38.
10. Kulkarni JP, Kim K, Roy K. A 160-mV robust Schmitt trigger based subthreshold SRAM. IEEE J Solid-State Circ. 2007;42:2303–13. DOI: 10.1109/JSSC.2007.897148.

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