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High-Performance Multi-Valued Logic (MVL) Gate Design Using FinFET

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Abstract

Complementary metal-oxide-semiconductor scaling faces challenges such as leakage, power dissipation, and short-channel effects. Multi-valued logic (MVL) offers higher information density and reduced interconnections. This work presents a fin field-effect transistor (FinFET)-based MVL gate design that improves electrostatic control, switching speed, and reliability. Simulation results confirm reduced leakage power and enhanced performance compared to conventional logic. The proposed architecture demonstrates scalability for advanced technology nodes. It also shows potential for low-power applications in portable and high-performance systems. Moreover, the design provides enhanced noise immunity and reduced signal distortion, both of which are essential for stable functioning in high-density integrated circuits. Furthermore, the suggested MVL framework aids in diminishing interconnect complexity, leading to layouts that make efficient use of area and enhancements in routing efficiency. Moreover, by optimizing the power-delay product, a well-balanced compromise between speed and energy consumption can be achieved, rendering the design highly appropriate for next-generation electronic systems. Overall, FinFET-based MVL gates provide an effective, scalable, and energy-conscious approach for future very large-scale integration (VLSI) designs that tackle the basic restrictions of conventional CMOS technology while facilitating compact and high-speed circuit implementations. Moreover, the design enhances noise immunity, minimizes signal distortion, optimizes power-delay performance, improves circuit stability, and facilitates efficient, scalable, and reliable nanoscale VLSI implementations.

Keywords: Multi-valued logic (MVL), FinFET, digital circuits, VLSI design, low-power circuits

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INTRODUCTION

The demand for low-power, high-performance digital circuits continues to grow, especially in portable and battery-operated systems. Figure 1 shows the schematic design of a fin field-effect transistor (FinFET)-based AND gate. With the increasing complexity of modern semiconductor designs, one of the primary challenges is achieving power reduction and performance optimization without compromising essential functionalities. Figure 2 shows the layout design of the FinFET-based AND Gate.

Although conventional binary logic circuits are widely used, they suffer from high interconnection complexity, power inefficiencies, and scaling limitations. Figure 3 shows the Simulation Results of the FinFET-based AND gate [1–3].

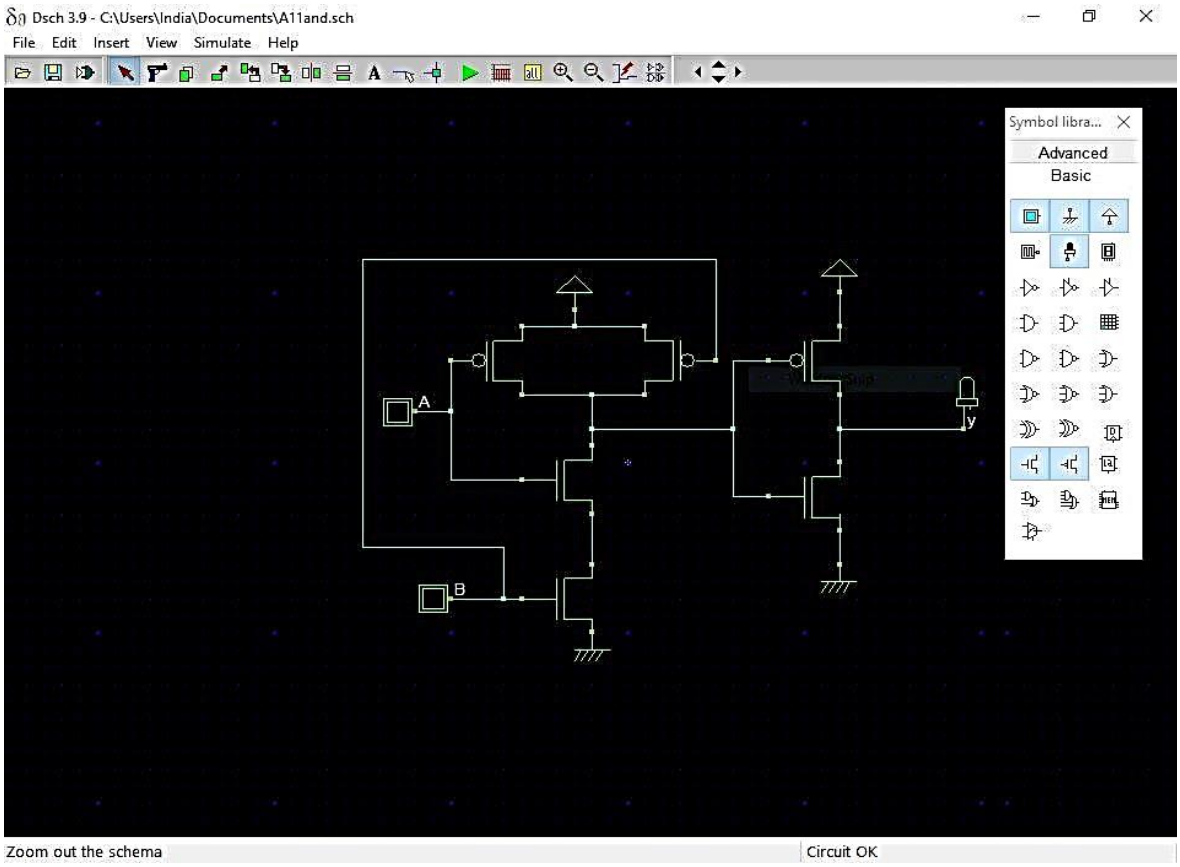

Figure 1. Schematic design of FinFET-based AND gate.

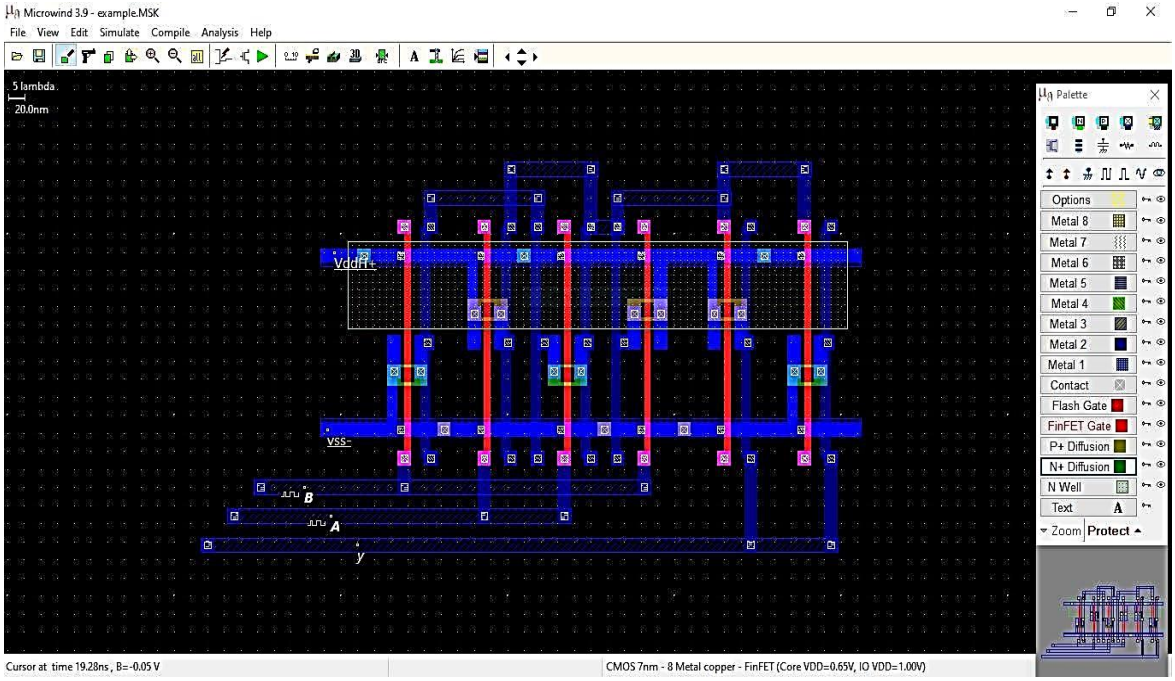

Figure 2. Layout design of FinFET-based AND gate.

To address these challenges, multi-valued logic multiple-valued logic (MVL) , which operates with three discrete states, provides an opportunity to optimize the circuit design and minimize the hardware overhead.

Figure 4 shows the schematic design of a FinFET-based OR gate. By leveraging FinFET technology, multiple-valued logic (MVL) gates can significantly reduce the transistor count while enhancing the switching efficiency, noise immunity, and computational speed. Figure 5 shows the layout design of the FinFET-based OR gate. This approach facilitates the development of energy-efficient very large-scale integration (VLSI) circuits that are suitable for next-generation processors, AI applications, and signal processing
units [4, 5].

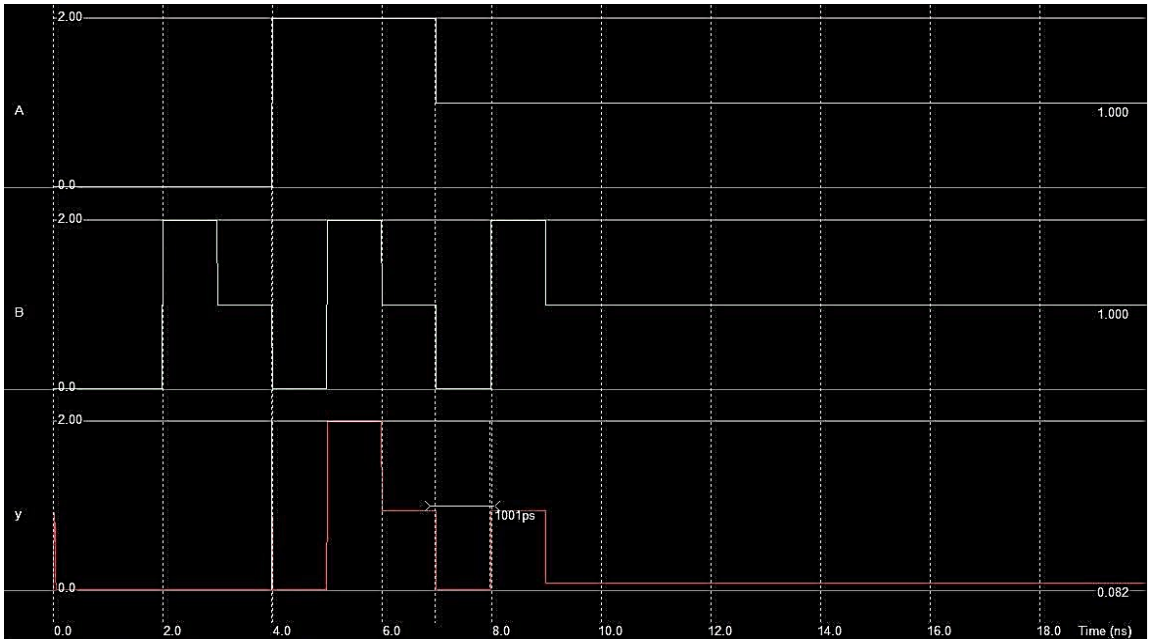

Figure 3. Simulation results of FinFET-based AND gate.

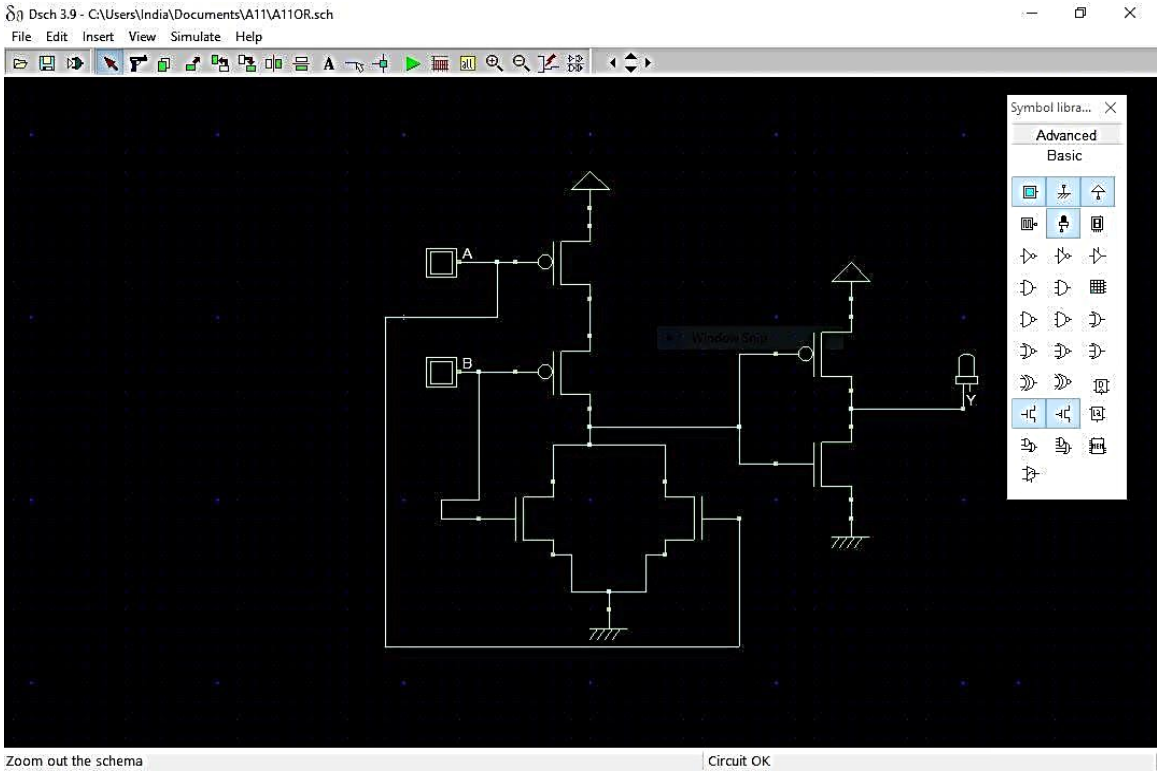

Figure 4. Schematic design of FinFET-based OR gate.

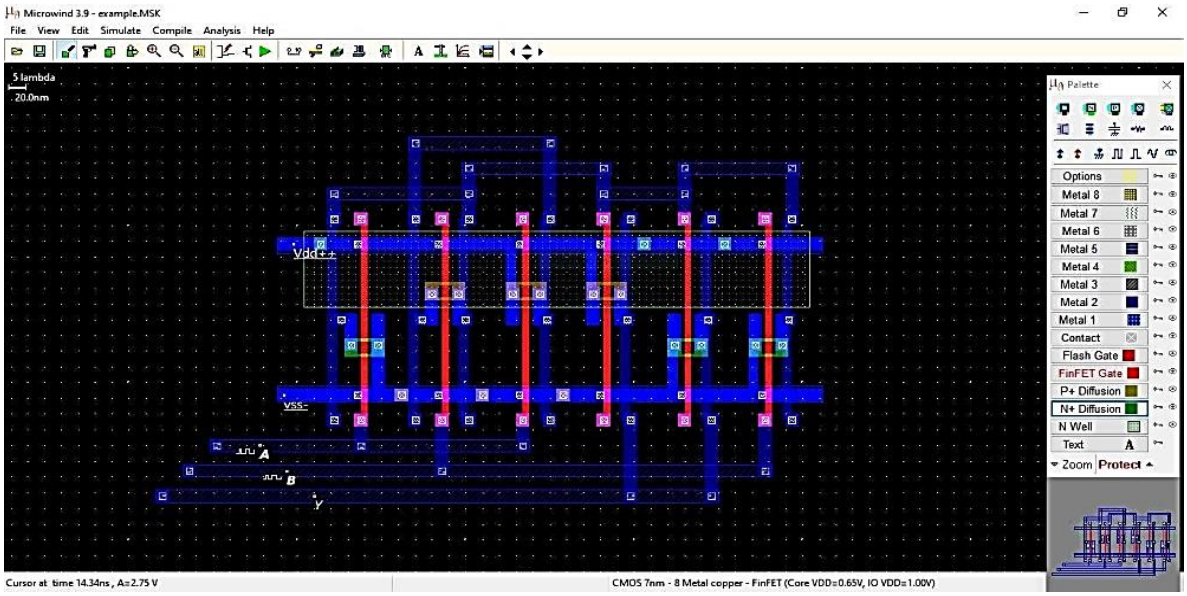

Figure 5. Layout design of FinFET-based OR gate.

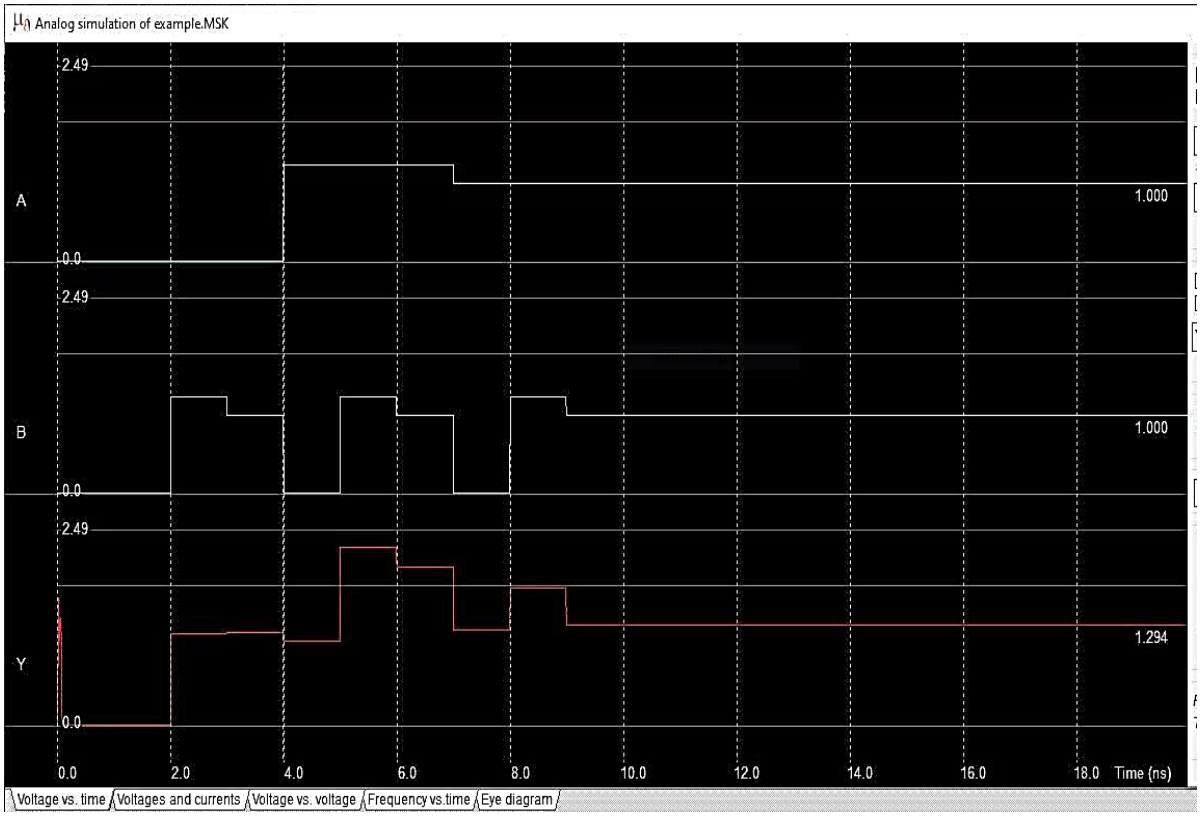

Figure 6. Simulation results of FinFET-based OR gate.

Significance of FinFET-based MVL logic gates reduced circuit complexity minimizes transistor count for optimized chip designs. Figure 6 shows the simulation results of the FinFET-based OR gate. Low-power consumption is significant energy savings compared to traditional CMOS. Enhanced noise immunity improves the overall circuit stability in dynamic environments. Efficient data processing facilitates compact and high-speed computation. Scalability for future technologies supports the transition to MVL systems in advanced microprocessor architectures. Figure 7 shows the schematic design of a FinFET-based NOT gate [6–8].

Applications: This novel FinFET-based MVL logic gate architecture holds great potential for low-power computing systems, next-generation AI processors, and VLSI. Figure 8 shows the layout design of the FinFET-based OR gate [9, 10].

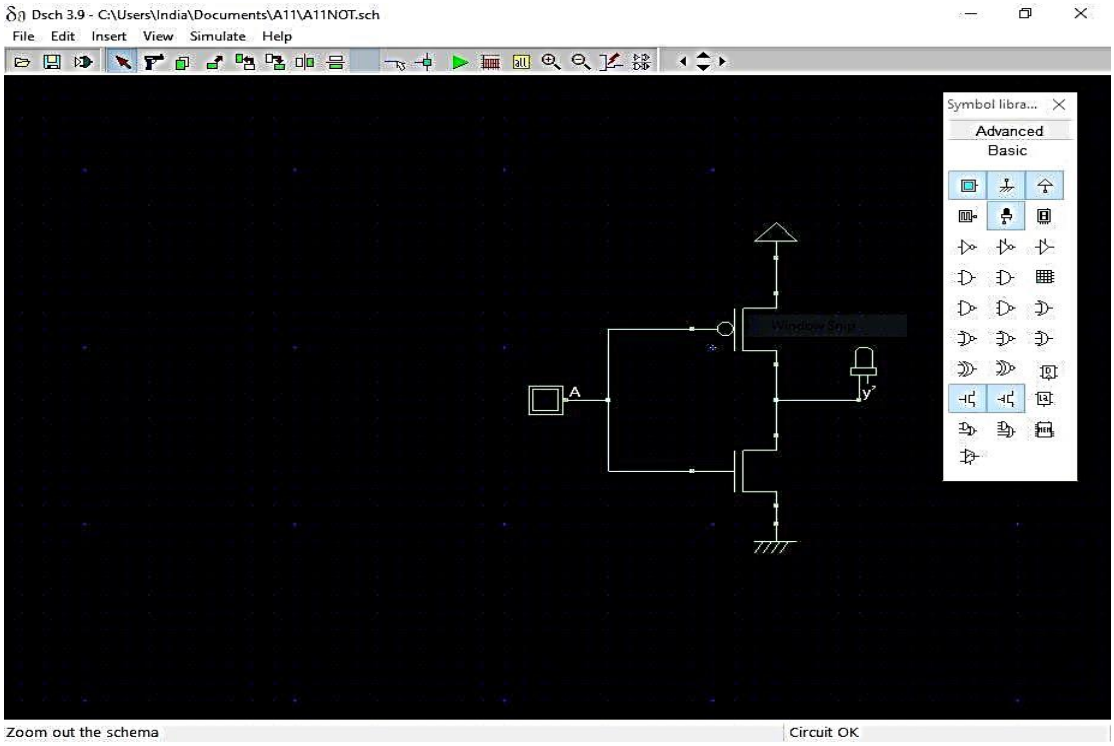

Figure 7. Schematic design of FinFET-based NOT gate.

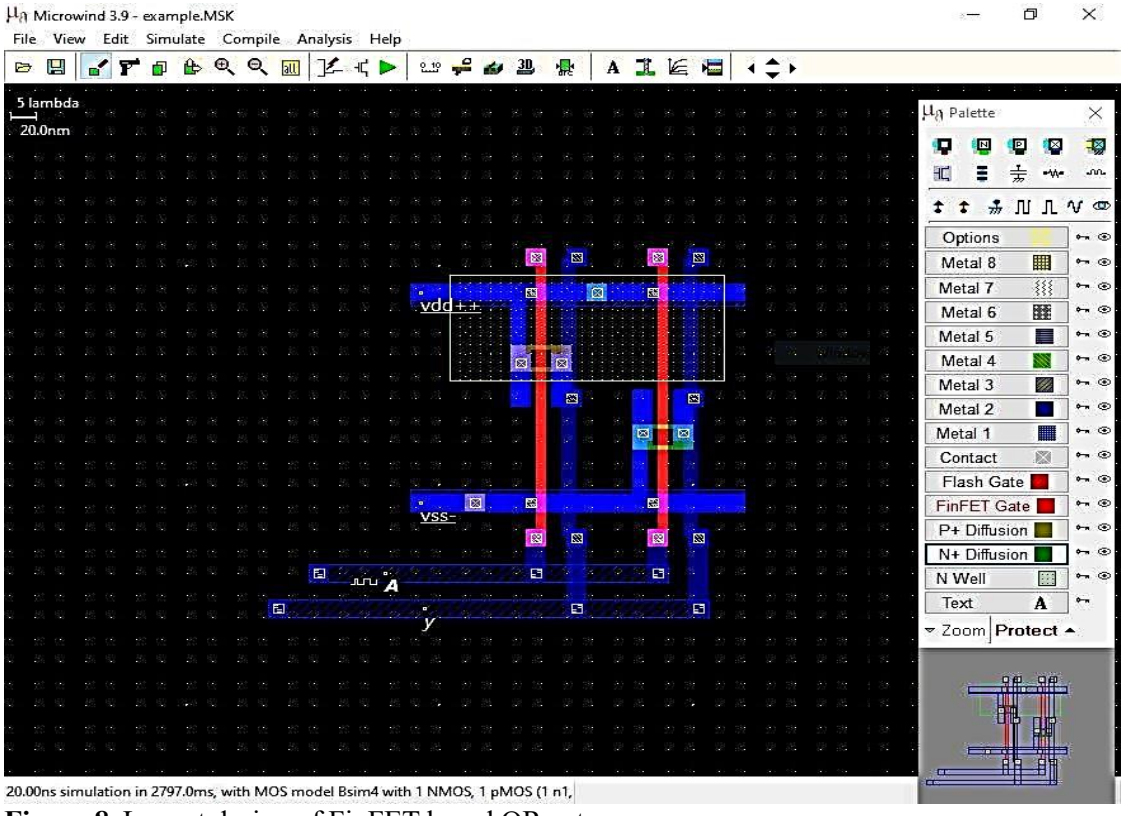

Figure 8. Layout design of FinFET-based OR gate.

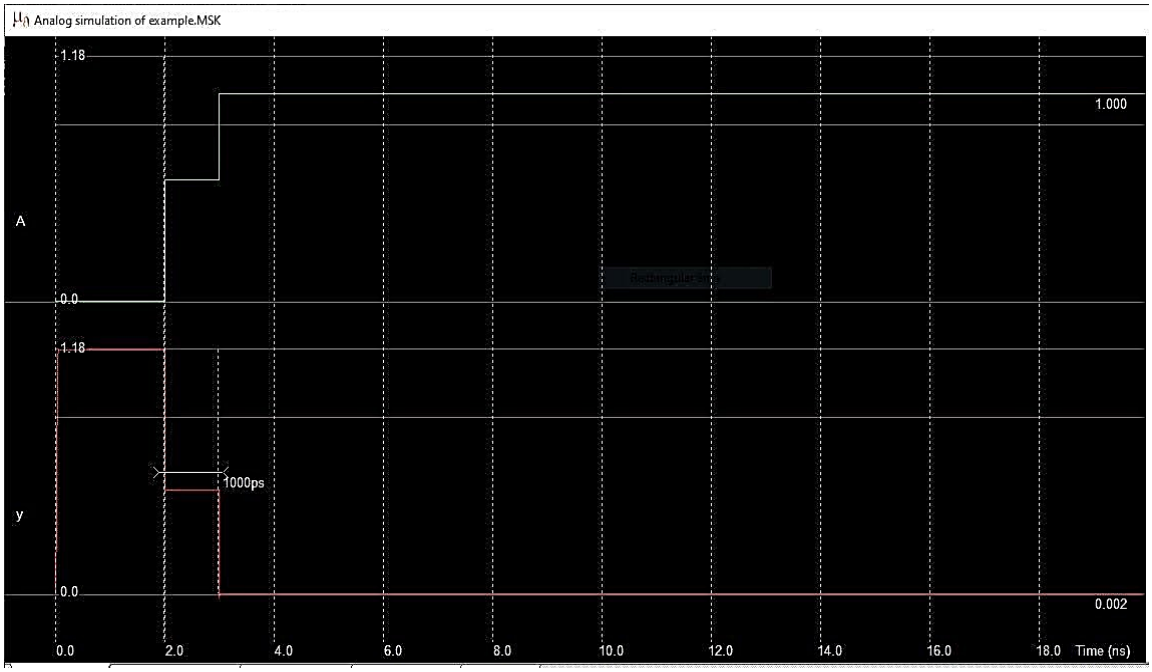

Figure 9. Simulation results of FinFET-based OR gate.

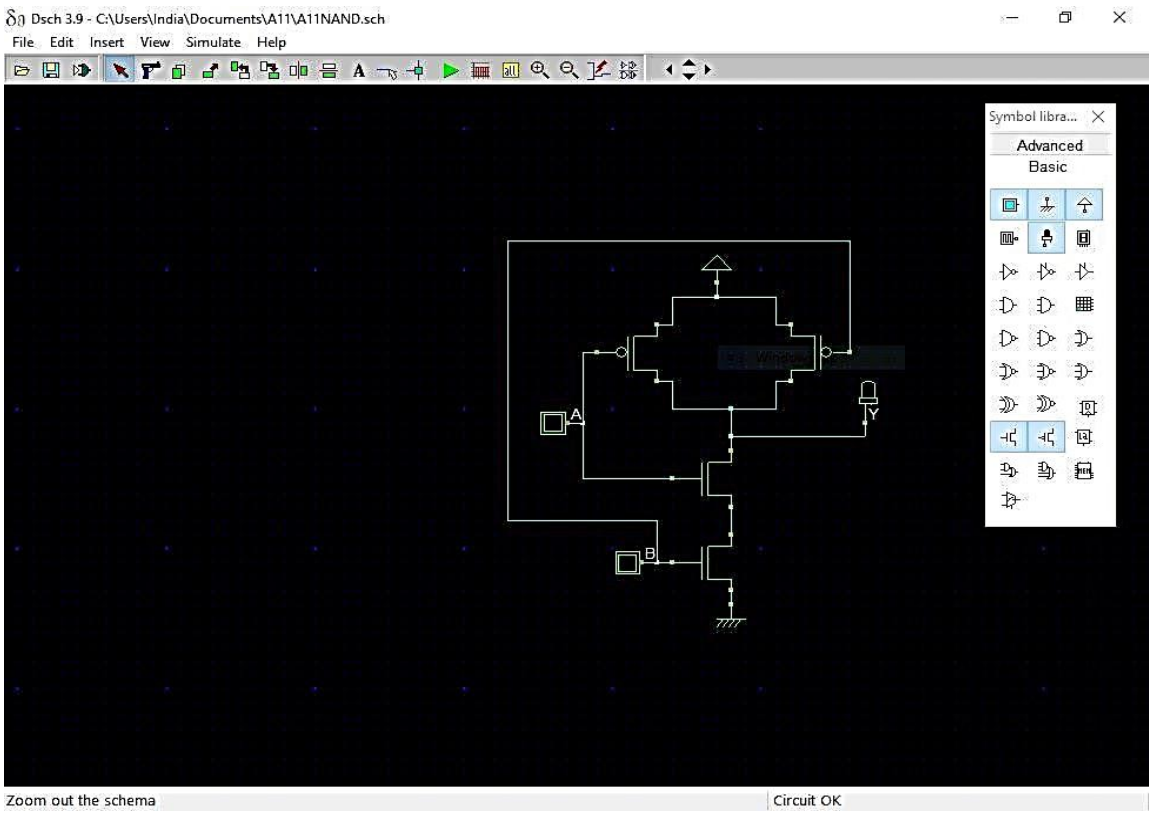

Figure 10. Schematic design of FinFET-based NAND gate.

Signal processing units, battery-efficient digital devices, and advanced telecommunication hardware. Figure 9 shows the simulation results of the FinFET-based OR gate. As digital systems evolve, integrating power-efficient, scalable, and noise-immune components into semiconductor circuits becomes a crucial step toward enhancing processing efficiency and minimizing overall power consumption. Figure 10 shows the schematic design of a FinFET-based NAND gate.

LITERATURE REVIEW

In the mid-1990s, significant advancements in transistor technology were initiated to address the limitations of conventional planar CMOS designs, particularly for digital circuit implementation in sequential and combinational logic systems. Early research explored optimization techniques for logic circuits to achieve improved power efficiency, area reduction, and noise immunity. However, as technology scaled to sub-32 nm regimes, traditional CMOS designs faced severe challenges due to short-channel effects and increased leakage currents, creating a demand for more advanced transistor architectures. In response, the introduction of FinFET technology marked a significant breakthrough in digital circuit design. FinFET devices, with their 3D structure and multi-gate configuration, provide better electrostatic control over the channel, reduced leakage currents, and enhanced scalability.

These properties make FinFETs a promising choice for advanced digital circuit designs, especially in the implementation of Multi-valued logic (MVL) systems. MVL logic gates, which form a subset of MVL, operate on three distinct logic levels (0,1, and 2) and offer advantages such as reduced transistor count, minimized interconnect complexity, and improved data density. In recent years, the integration of FinFET technology into MVL logic gate designs has garnered significant attention. By leveraging multi-threshold voltage levels and optimizing the transistor configurations, FinFET-based MVL logic gates have shown substantial improvements in power efficiency, delay performance, and noise immunity. The ability to achieve these improvements without significantly increasing circuit complexity makes this approach highly attractive for modern VLSI systems, particularly in applications like low-power internet of things (IoT) devices, AI processors, and portable systems.

METHODOLOGY

The proposed work focuses on the design and implementation of MVL gates using FinFET technology to achieve improved performance, reduced power consumption, and enhanced scalability. Figure 11 shows a schematic of FinFET-Based MVL logic gates (NOT and NAND). The methodology begins with an analysis of the limitations of conventional CMOS-based logic circuits, such as leakage current, short-channel effects, and reduced reliability at nanoscale dimensions. Figure 12 shows the circuit diagram of FinFET-based MVL logic. To overcome these issues, FinFET technology is selected due to its superior electrostatic control and reduced leakage characteristics.

Initially, the MVL system is defined by selecting multiple discrete voltage levels to represent different logical states. Figure 13 shows the layout design of a FinFET-based NAND gate. Proper voltage thresholds were established to ensure reliable switching and sufficient noise margins between the logic levels. The FinFET device structure was then modelled to understand its electrical behavior under various operating conditions. Figure 14 shows the schematic design of a FinFET-based NOR gate.

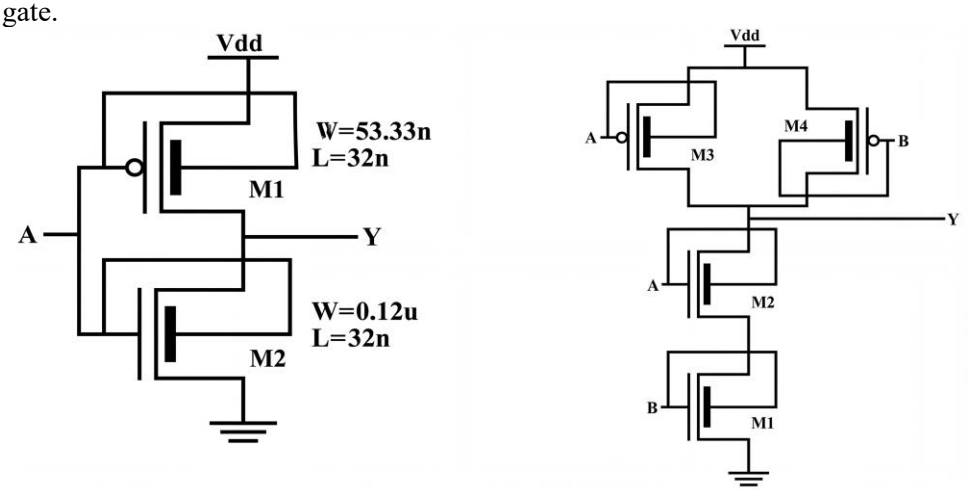

Figure 11. Schematic of FinFET-based MVL logic gates (NOT and NAND)

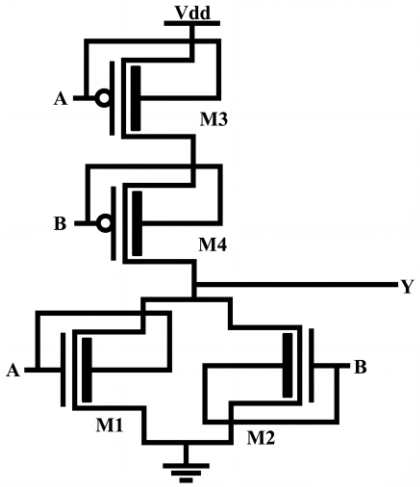

Figure 12. Circuit diagram of FinFET-based MVL logic gates.

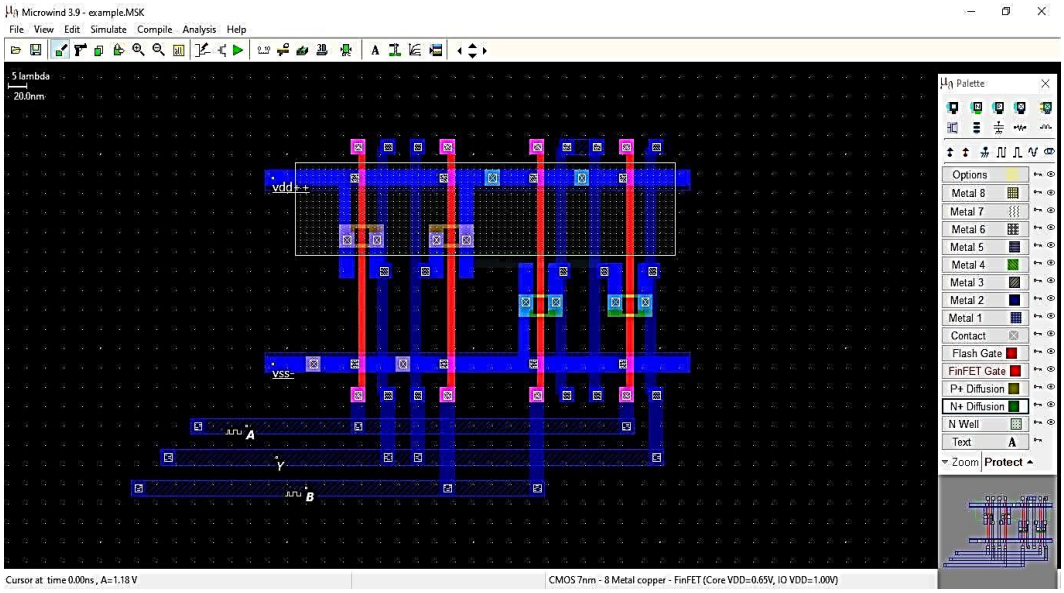

Figure 13. Layout design of FinFET-based NAND gate.

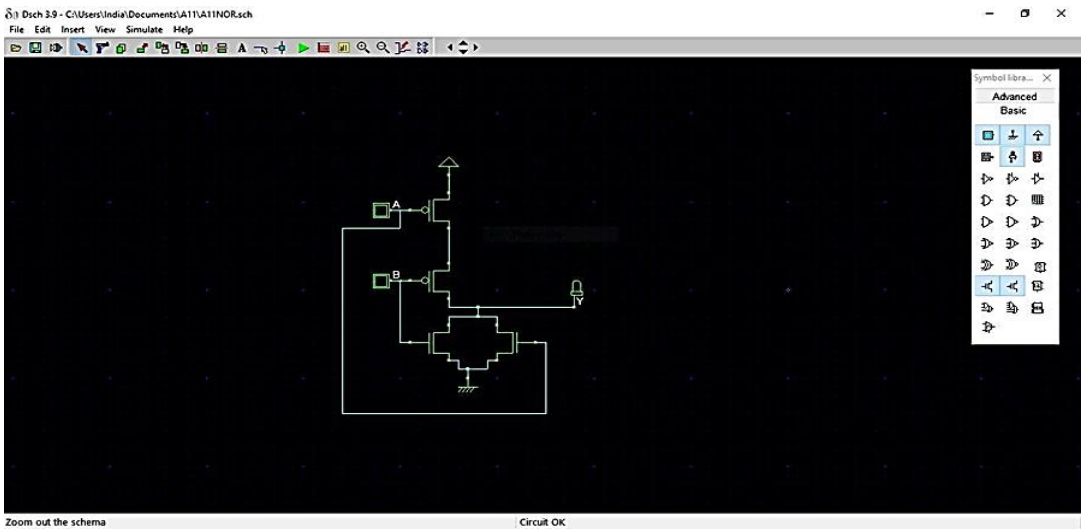

Figure 14. Schematic design of FinFET-based NOR gate.

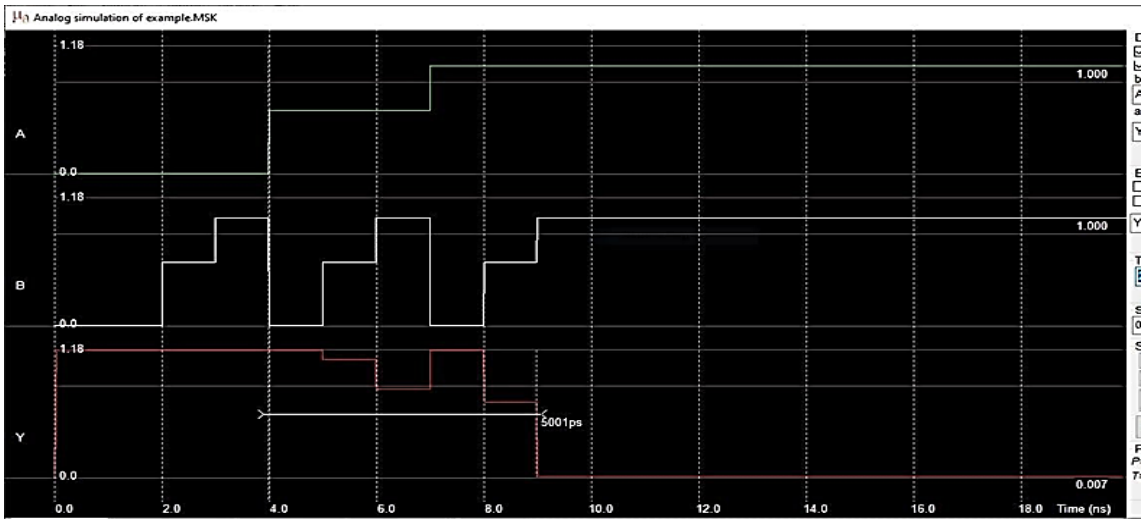

Figure 15. Simulation results of FinFET-based NAND gate.

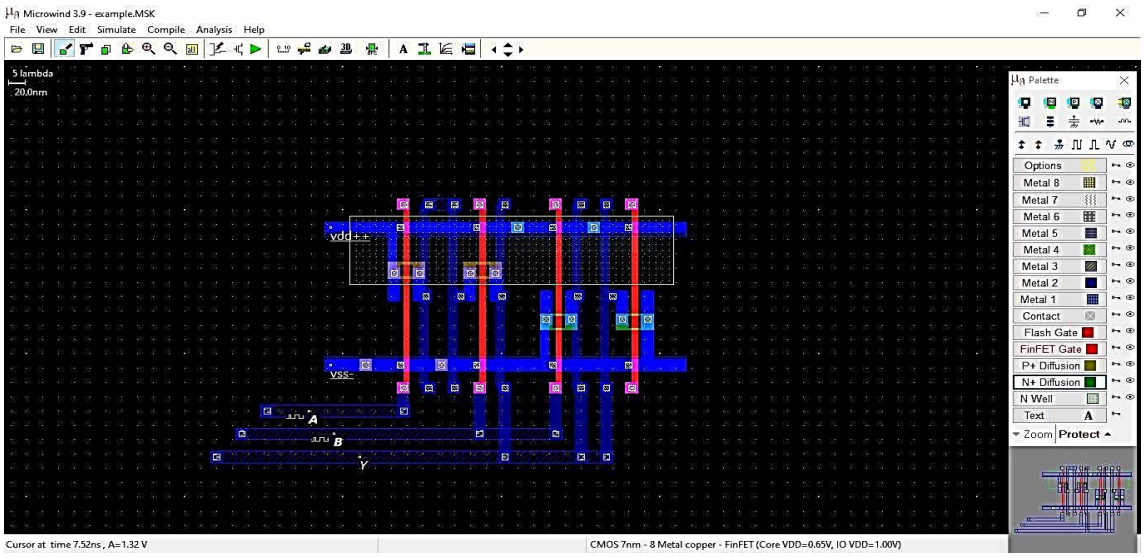

Figure 16. Layout design of FinFET-based NOR gate.

Based on this, MVL gates, such as inverters, NAND, and NOR, are designed using FinFET transistors. The circuit configuration was carefully arranged to support multiple logic levels while maintaining stability and minimizing power dissipation. Figure 15 shows the simulation results of FinFET-based NAND. The designed circuits were simulated using Tanner electronic design automation (EDA) tools to verify their functionality and performance. Key parameters, such as propagation delay, power consumption, and switching speed, were analyzed. The output waveforms were observed to confirm the correct logic-level transitions. Figure 16 shows the layout design of a FinFET-based NOR gate.

In this work, MVL logic levels are defined using three distinct voltage levels, namely 0 V, 0.45 V, and 0.9 V, representing logic states 0, 1, and 2, respectively. A FinFET device structure is utilized to maintain stable transitions between these levels and ensure reliable operation.

MVL gates, such as NOT, NAND, and NOR, are designed using FinFET transistors. The circuit configuration was optimized to reduce the transistor count, minimize the power consumption, and improve the switching speed. The design ensures proper voltage-level separation and noise immunity. Figure 17 shows the simulation results of a FinFET-based NOR gate.

Advanced FinFET-Based MVL Logic Gates

The proposed designs for FinFET-based MVL logic gates prioritize minimizing the number of transistors while optimizing the circuit performance in terms of power, area, and speed. These MVL logic gates utilize FinFET technology to effectively address key challenges in traditional logic circuits, such as leakage currents, short-channel effects, and scalability issues. Leveraging FinFET's wraparound gate architecture, the design achieves precise control over the fin-shaped channel, enabling efficient operation at three distinct voltage levels (e.g., 0, 1, and 2) required for MVL logic. In addition, the suggested design boosts the switching efficiency and lowers the dynamic power usage via optimized threshold voltage management. Additionally, it enhances signal integrity and noise margins, guaranteeing dependable multilevel functioning. This architecture enables a higher integration density and is compatible with cutting-edge fabrication technologies for next-generation VLSI systems.

The FinFET-based T-NOT, ST-NAND, and ST-NOR gates demonstrated significant improvements over the conventional MOSFET-based MVL logic designs. Figure 18(a) and (b) show the MVL logic NAND and NOR gates, and (b) the MVL logic NOR gate. Their compact structure reduces the transistor

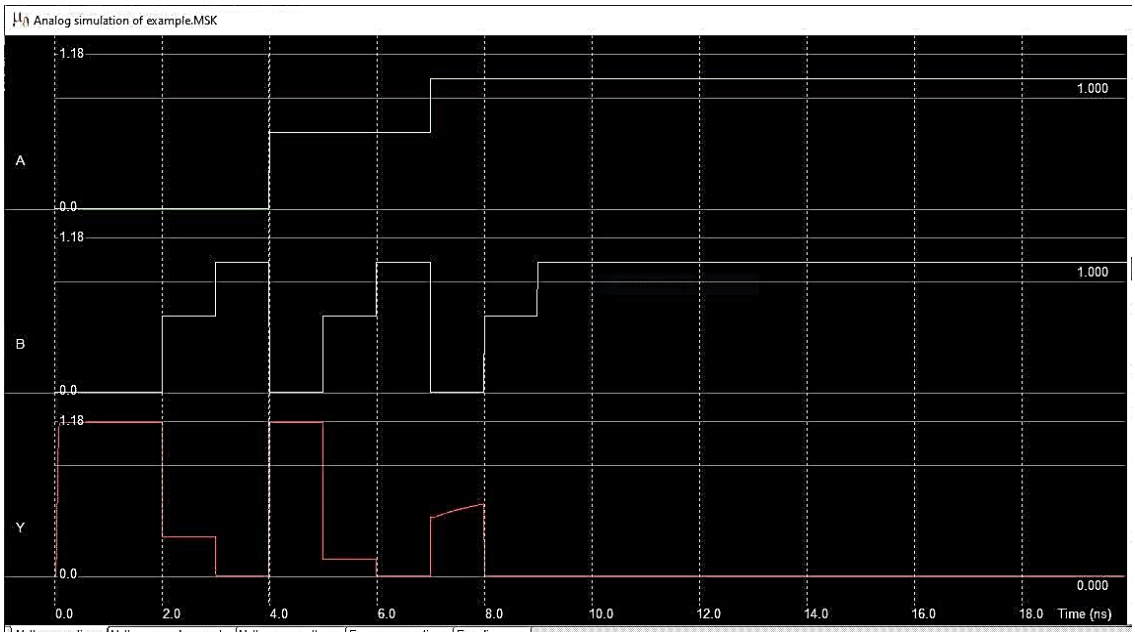

Figure 17. Simulation results of FinFET-based NOR gate.

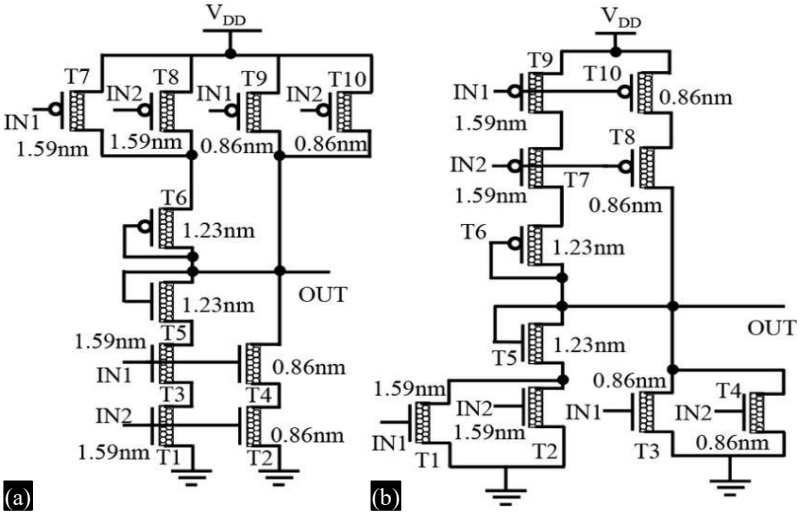

Figure 18. (a) MVL logic NAND gate, (b) MVL logic NOR gate.

Table 1. CMOS versus FinFET (7 nm) logic gate performance comparison.

Gate type	Technology	Power consumption	Area	Delay	Number of transistors
AND gate	CMOS	32.078 µW	6.9 µm²	2.4 ns	14
	FinFET (7 nm)	25.424 µW	0.3 µm²	600 ps	8
OR gate	CMOS	39.151 µW	7.4 µm²	2.5 ns	14
	FinFET (7 nm)	31.934 µW	0.4 µm²	620 ps	8
NOT gate	CMOS	44.673 µW	2.6 µm²	2.1 ns	4
	FinFET (7 nm)	24.403 µW	0.1 µm²	500 ps	2
NAND gate	CMOS	5.727 µW	4.5 µm²	2.8 ns	16
	FinFET (7 nm)	502 nW	0.2 µm²	650 ps	10
NOR gate	CMOS	1.160 µW	4.5 µm²	3.0 ns	16
	FinFET (7 nm)	470 nW	0.2 µm²	680 ps	10

count, optimizing the area usage while maintaining high-speed performance. The enhanced electrostatic control provided by FinFET ensures reliability and stability, even under stringent power constraints.

These MVL logic gates are specifically designed for energy-efficient and scalable VLSI applications, offering reduced power consumption and faster switching speeds. By carefully tuning the threshold voltages of FinFET devices, the gates achieve high accuracy in logic operations, making them well-suited for modern digital systems like IoT devices and portable electronics.

PERFORMANCE ANALYSIS

The performance of the proposed MVL gate design is evaluated based on several parameters:

Power Consumption

Power consumption is an important factor in modern digital circuit design. FinFET technology reduces the leakage current, resulting in lower static power consumption.

Propagation Delay

Propagation delay represents the time required for a signal to propagate from the input to the output. The proposed FinFET-based MVL gate exhibits an improved switching speed compared to traditional CMOS circuits.

Area Efficiency

MVL circuits reduce the number of required interconnections, which helps reduce the chip area and improve the integration density. Table 1 shows a comparison of the CMOS and FinFET (7 nm) logic gate performances.

CONCLUSION

By analyzing the electrical characteristics, conventional MVL logic gate designs face challenges such as short-channel effects, including barrier lowering due to increased drain voltage, impact ionization, and ion scattering. These challenges are more pronounced in traditional transistor technologies, limiting their scalability, reliability, and energy efficiency.

In the proposed FinFET-based MVL logic gate designs, these limitations are effectively addressed by leveraging an advanced double-gate FinFET architecture. This structure significantly reduces parasitic capacitance, ensuring enhanced immunity to short-channel effects. Experimental analyses highlight several advantages of the double-gate configuration over traditional single-gate designs, including:

- *Improved drain current output:* The double-gate structure enables a more robust and efficient current flow.
- *Minimal gate misalignments:* Precise design and simulation mitigate minor gate misalignments to ensure consistent performance.

The simulation results reveal that the proposed designs showcase remarkable advancements in terms of:

- *Energy efficiency:* FinFET-based MVL logic gates dramatically reduce power consumption, making them ideal for low-power applications.
- *Speed optimization:* Enhanced switching speeds support real-time processing in advanced digital systems.
- *Scalability:* The compact and energy-efficient layout enables integration into high-density VLSI systems with a small footprint.

The adoption of FinFET technology in MVL logic gate designs establishes new benchmarks in power efficiency and high-speed performance, addressing critical challenges in modern circuit design. By combining energy-saving features and scalability, these novel designs prove to be optimal solutions for next-generation applications such as IoT devices, AI platforms, and high-speed communication systems.

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