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High-speed Data Converter Architectures: Latched Comparator Design & Performance Comparison

Banoth Krishna[1,*], Sandeep Singh Gill[2], Amod Kumar[3]

Abstract

This paper focuses on the design and optimization of latch comparators for high-speed data converter applications. The performance of different comparator architectures is compared in terms of speed, power consumption, and noise performance. The proposed latch comparator architecture uses a preamplifier to boost gain and sensitivity, and a latch to store the output signal. The latch comparator design is optimized for low power consumption and high speed, and is implemented using 180 nm CMOS technology. The circuits are simulated using cadence virtuoso simulators with a 1.8 V supply DC voltage and a clock frequency of approximately 500 MHz. The responses of the circuits are analyzed and plotted, and the static and dynamic characteristics of different types of comparators are compared, highlighting their advantages and disadvantages. Simulation results show that the proposed latch comparator architecture has better performance compared to other comparator architectures, with lower power consumption and higher speed. The paper also discusses the trade-offs between power consumption, speed, and noise performance, and provides guidelines for selecting the appropriate comparator architecture for high-speed data converter applications.

Keywords: High speed comparator, Latch comparator, Double tail comparator, High speed ADC

INTRODUCTION

Comparators play a crucial role in electronic IC applications, particularly in data converters for comparing two different signals. During the conversion process, the signal is first sampled and then sent through several comparators to obtain the digital equivalent of the analog signal values. A comparator's design requires minimal power consumption [1], a low offset voltage, low noise, high speed, and a better slew rate. To achieve these specifications, dynamic comparator topologies are considered. Dynamic comparators are suitable for high speed, low power dissipation, and zero static power consumption. Two back-to-back inverters are used to provide the positive feedback circuit [2]., which converts a small voltage difference to full scale output digital levels. Such comparators are used in different applications, such as zero crossing detector, peak detector, and switching power regulators." Referring to Figure 1, when VinP is higher than VinN, the output is at logic 1, and when VinP is lower than VinN, the output is at logic 0.

***Author for Correspondence**
Banoth Krishna
E-mail: krish552011@gmail.com

[1]Research Scholar, Department of Electrical Engineering, National Institute of Technical Teachers Training and Research, Chandigarh, Punjab, India
[2]Professor, Department of Electrical Engineering, National Institute of Technical Teachers Training and Research, Chandigarh, Punjab, India
[3]Professor and Head, Department of Electrical Engineering, National Institute of Technical Teachers Training and Research, Chandigarh, Punjab, India

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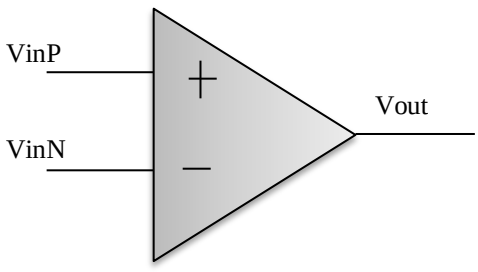

Figure 1. Comparator symbol.

Ideally, a binary signal has two states, a lower state called 0-state and a higher state called 1-state. The transition region between these states is the region from 0-level to 1-level, as described by Babayan-Mashhadi et al. (2013) [3].

DYNAMIC LATCHED COMPARATOR ARCHITECTURES

The comparator architecture consists of three blocks:

- Preamplifier,
- Latch Block,
- Buffer Block.

Figure 2 illustrates the preamplifier stage, composed of a differential amplifier (M1 and M2) with active loads (M3 and M5), designed to amplify the input signal to enhance comparator efficiency. Its function is twofold: first, it elevates the minimal input signal required for the comparator to reach a decision; second, it shields the comparator's input from kickback noise originating from the positive feedback step. Additionally, the preamplifier stage mitigates the input-referred offset voltage [4]. The sizing of the transistors in the differential stage (M1 and M2) is determined by the input capacitance and the transconductance of the differential amplifier (gm1=gm2). This transconductance dictates the gain of the stage as well as the input capacitance (Purushothaman, A. et al., [5]; Bahmanyar, P. et al., [6]).

Latched Comparator Design with Preamplifier

The positive feedback latch stage of the comparator serves to discern and amplify discrepancies between the input signals. Following this stage, the comparator's output section, termed the buffer stage, is comprised of a self-biased differential amplifier followed by an inverter. This configuration enables the comparator to accommodate differential inputs while delivering full-scale digital logic-1 and logic-0 outputs.

The design of the latched comparator with a free amplifier is shown in Figure 3, and the conversion delay for this design is Td = 648.83261ps.

DOUBLE TAIL LATCH COMPARATOR

Figure 4 illustrates a double tail architecture.

Jain, R., et al., [7], which employs two distinct tail currents and clock signals. One tail current is dedicated to the input stage, while the other serves the latch stage. This architecture operates in two modes: precharge mode (clock=0) and evaluation mode (clock=1). Notably, this version features reduced stacking and functions at a lower supply voltage. The precharge transistor consumes a substantial current that remains independent of the input common mode voltages. Furthermore, the size of the transistor's differential pair is diminished, necessitating less supply voltage and yielding lower offset voltage.

In this design conversion delay is 0.831103 usec and power dissipation is 140.7 uw.

When (clock = 0 V) precharge mode, M7 and M8 turn ON and charges to VDD, which can charge regenerative nodes to VDD, it means it is at logic-1(high) of transistors M5 and M3 output nodes discharge to ground.

During the evolution mode (clock=VDD), transistors M0 and M11 are activated, causing the common mode voltage to gradually decrease, thereby generating a differential mode voltage. This differential voltage is conveyed to the latch through M3 and M5. Subsequently, the inverter initiates the regeneration of the voltage difference as soon as the common mode voltage at the node falls below the threshold necessary for M3 and M5 to constrain the output to ground. Figure 6 depicts the output

response and delay analysis of the Double tail latch comparator design, with a conversion delay of 0.831103 usec.

SELF-CALIBRATING DYNAMIC COMPARATOR

In the self-calibrating dynamic comparator depicted in Figure 6, and its response shown in Figure 7, the input-referred latch offset is mitigated by employing two transistors (designated as tail 2 for compensation) as loads in the latch stage. This configuration reduces the maximum drive current of output nodes by half the supply voltage. To address the precision timing issue between clk and clkb, the calibrated circuit replaces clkb with the Ni node value. Input-referred offset voltage denotes the static offset caused by mismatch in identical pairs of input transistors, which could potentially influence the comparator's behavior. While a preamplifier can be utilized in the comparator architecture to minimize input offset, it introduces additional circuit complexity and consumes more power. The matching of CMOS transistor properties encompasses factors such as threshold mismatch and current factor mismatch, which can be approximated for a given gate oxide thickness and transistor size. Random mismatches can be characterized as

$$\sigma^2(V_{th}) = \frac{A_{VTH}^2}{WL_{eff}} \tag{1}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL_{eff}} \tag{2}$$

Where σ = standard deviation, A =area proportionality constant, WL are the width and length of transistors.

The transistors mismatches are statistical value and these are modeled as Gaussian distribution.

The total referred offset is given as

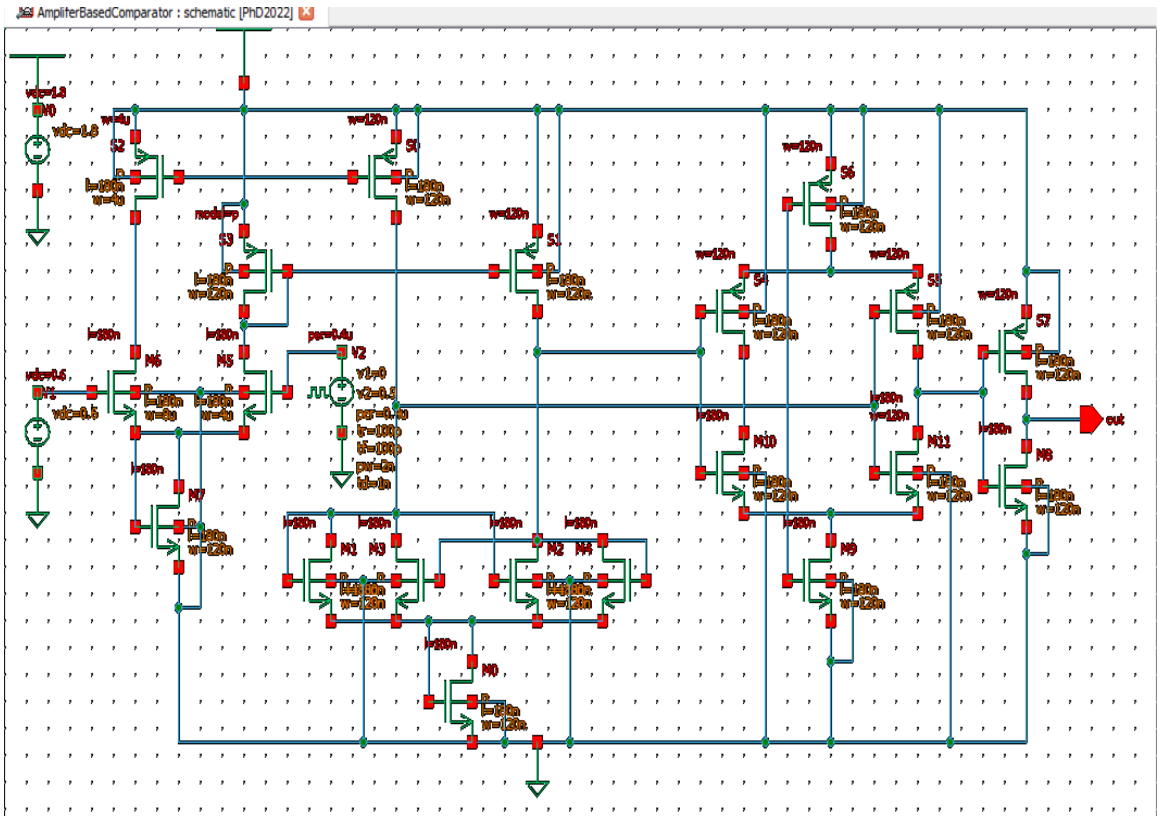

Figure 2. Latched comparator design with preamplifier.

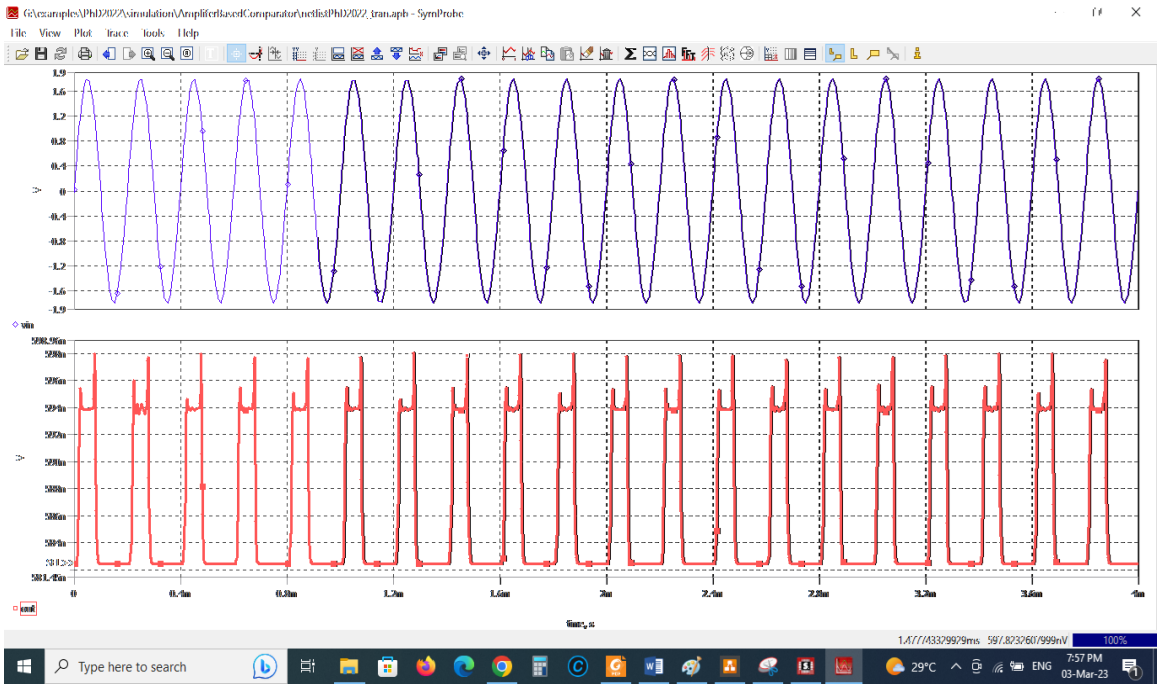

Figure 3. Latched comparator design with free amplifier.

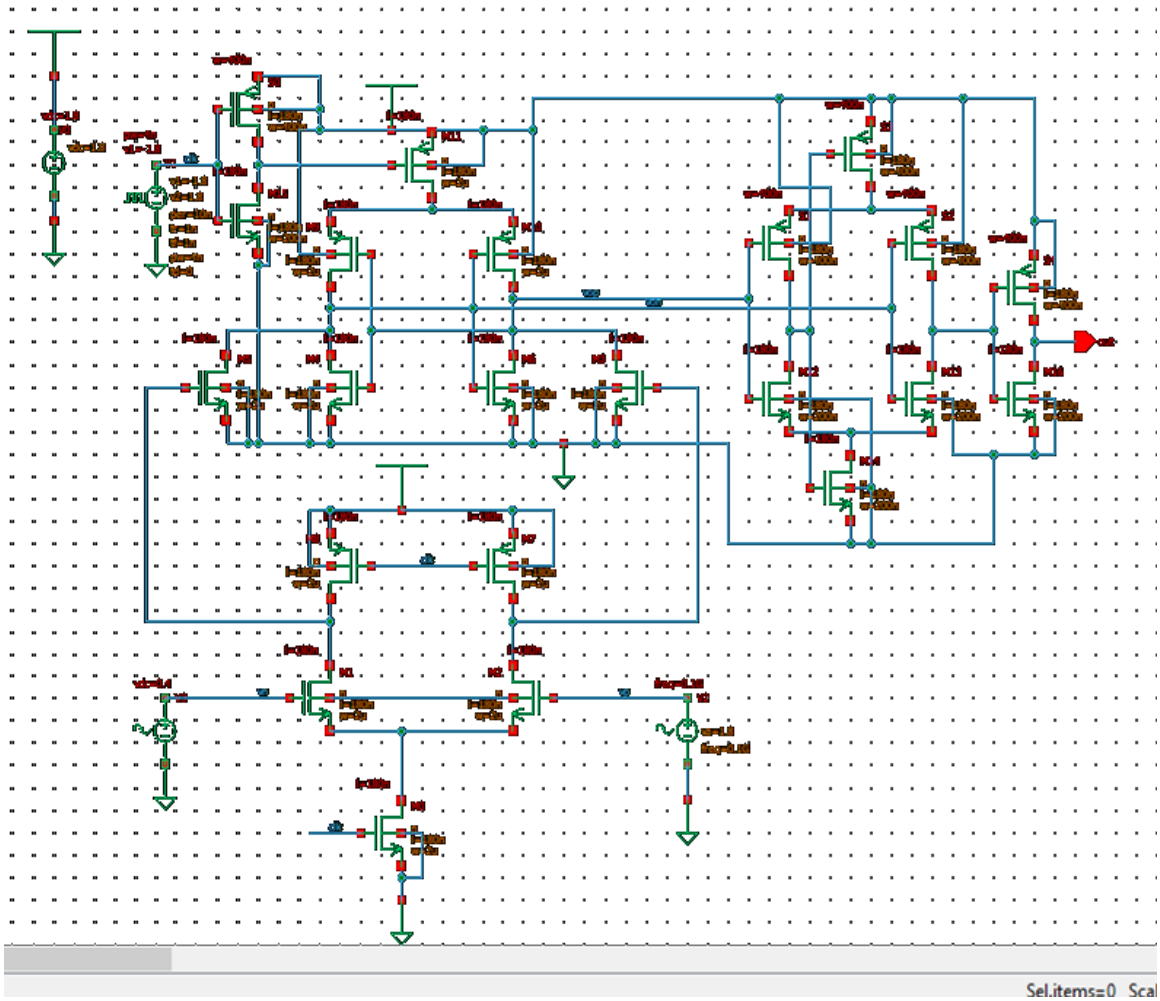

Figure 4. Double tail latch comparator design.

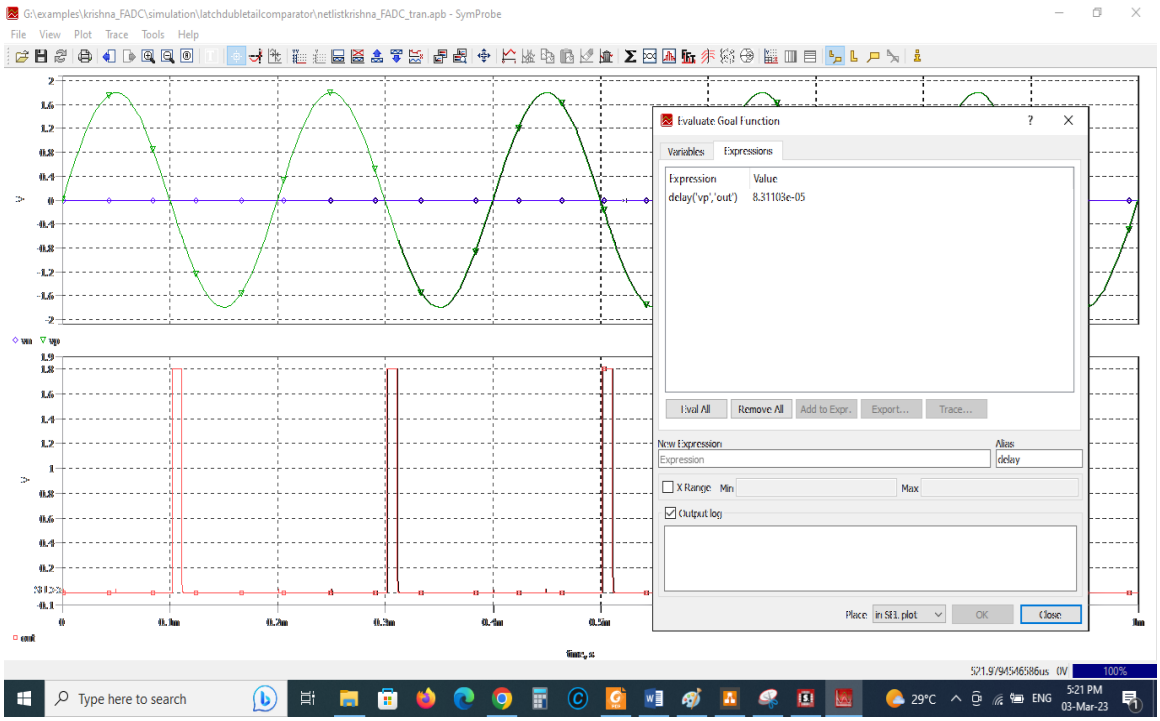

Figure 5. Double tail latch comparator design output response.

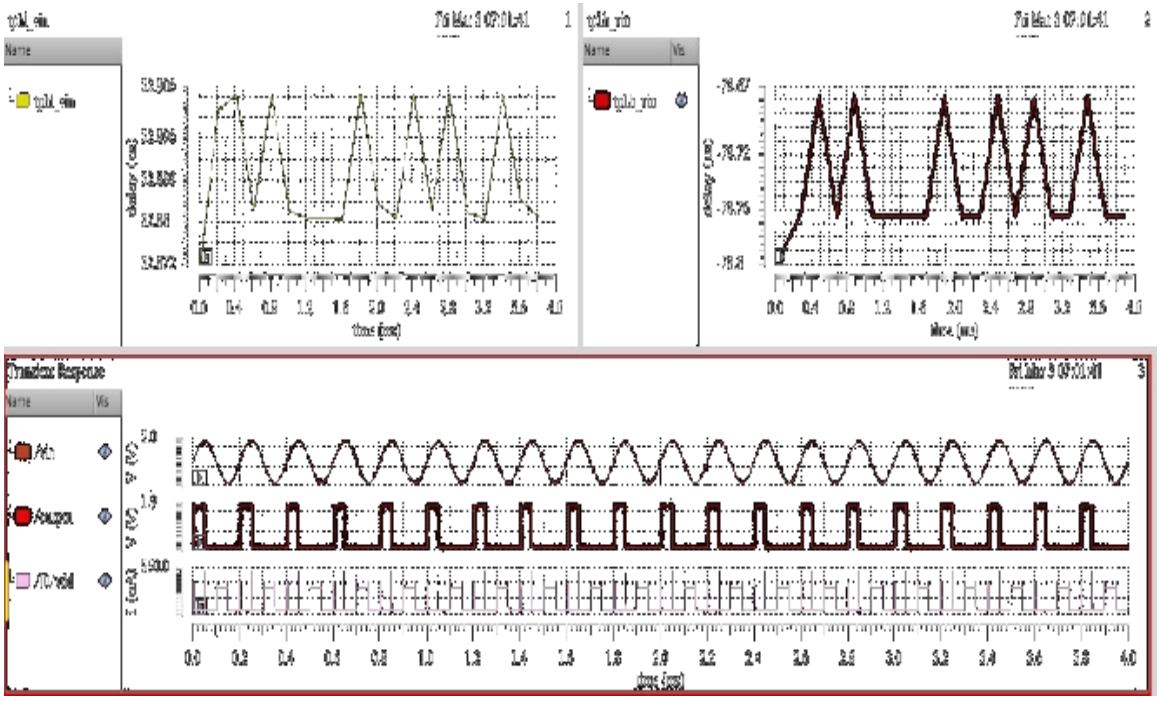

Figure 6. Double tail latch comparator design output response with delay analysis.

$$\sigma_{total}^2 = \sigma_{\Delta vth1}^2 + \sigma_{\beta 1}^2 + \sigma_{\Delta vth2}^2 + \sigma_{\beta 2}^2 \quad (3)$$

The mismatch in comparator leads to reduce the ADC resolution.

The circuit diagram for the Self Calibration Dynamic Latch Comparator is displayed in Figure 6, and Figure 7 exhibits the circuit's output responses. The calculated delay for the output response is 0.302529 us, and the power dissipation is 2.2 mw.

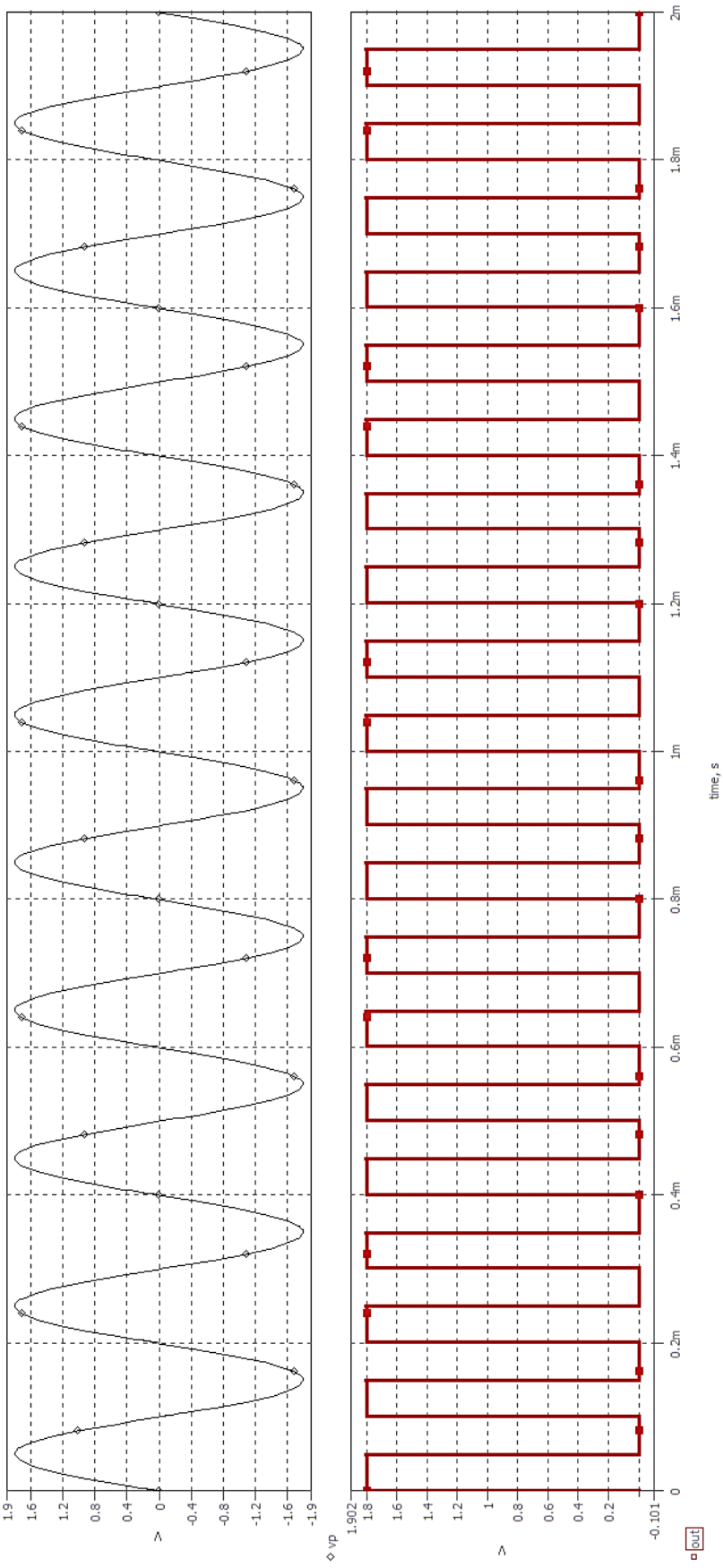

Figure 7. Self calibration dynamic latch comparator circuit output responses.

DUAL RAIL DOUBLE TAIL LATCHED DYNAMIC COMPARATOR

The double tail latched comparator, depicted in Figure 8, is designed to eradicate weakly regeneration nodes by inserting an inverter between the input and output nodes.

This configuration enables the comparator to operate at a higher speed and consume less power compared to conventional comparators (Dubey, A. K., et al., [8]; Varshney, V., et al., [9]; Dubey, A. K., [10]). The dynamic comparator's transient behavior, illustrated in Figure 9, portrays a sinusoidal input voltage source against a DC reference voltage, with a supply voltage of 1.8 volts and a reference voltage of 0 volts, as outlined in Table 1.

Figure 9 displays the output responses of the Dual Rail Double Tail Latched Comparator, while the simulated response allows for optimization of power, with power=Vdd×Ids=1.8132.94*10-6 watts, resulting in P=0.024 µW. Furthermore, Figure 10 illustrates the frequency responses of the same Dual Rail Double Tail Latched Comparator.

Table 1. Comparator design specifications

Parameters	Specification
Technology	180 nm
Supply voltage	1.8 v
Clock frequency	500 MHz
Clock voltage	0v-0.6 v
Rise time	50ps
Falls time	50ps
Pulse width	2ns
Reference voltage	0.1v-0.8
Temperature	27°c

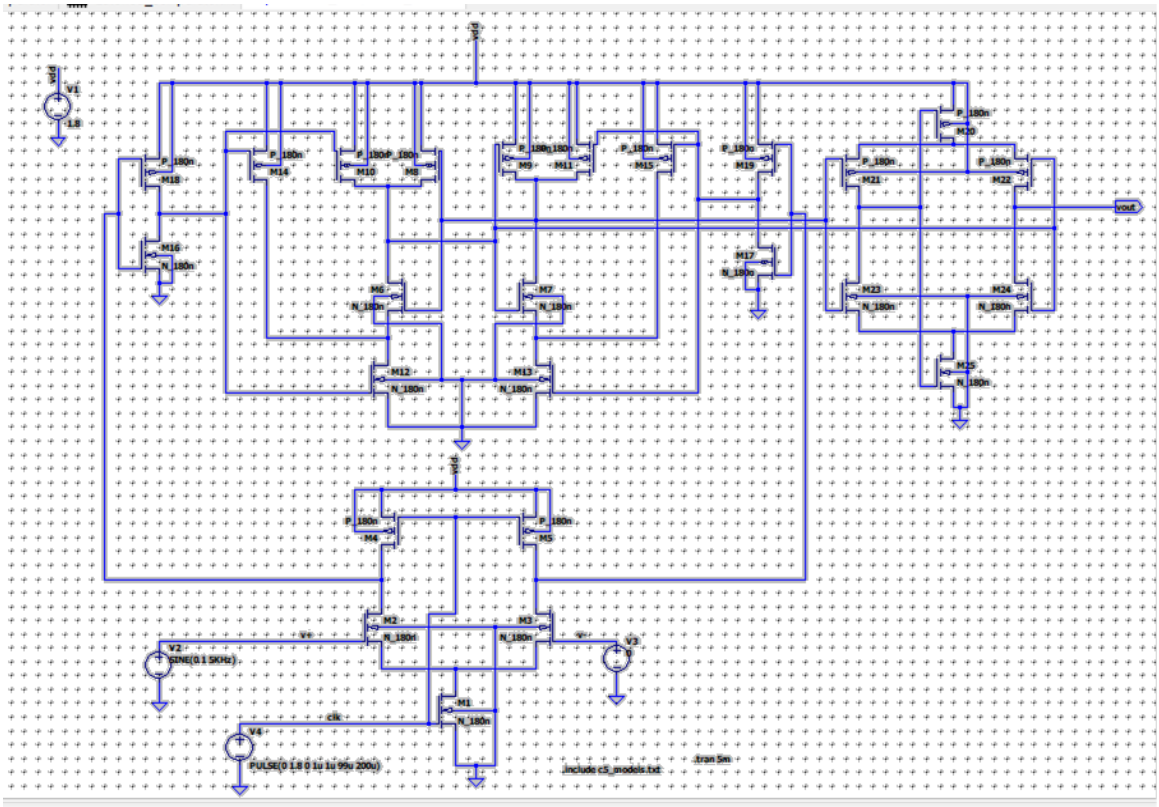

Figure 8. Dual rail double tail latched comparator.

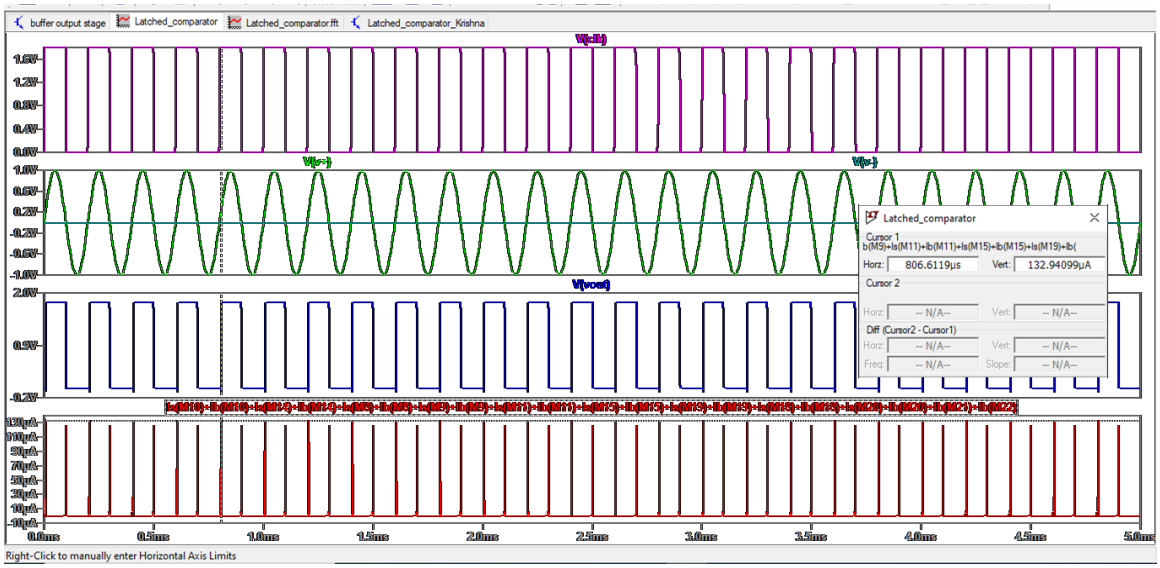

Figure 9. Dual rail double tail latched comparator output responses.

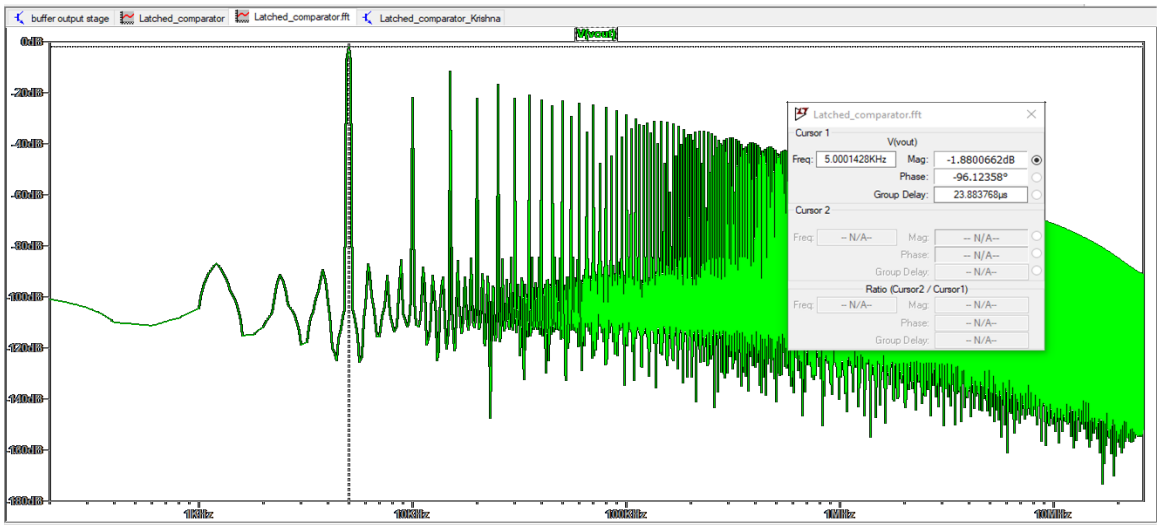

Figure 10. Dual rail double tail latched comparator frequency responses.

Table 2. Parameters comparison at different architectures

Parameters at Comparators	Preamplifier based comparator	Double tail latch comparator	Self-calibration Dynamic comparator	Double tail dual rail comparator
Speed [GHz]	1.54	1.1	2.5	9.8
No. of. Transistor	20	22	23	25
Power dissipation [w]	102.5 µ	64.7 µ	2.2 m	0.024 µ
Delay [ps]	648.8	875.6	395.56	102.3
Offset voltage[mv]	18.4	36.1	13.9	12
Supply voltage [V]	1.8	1.8	1.8	1.8
Technology	180 nm	180 nm	180 nm	180 nm

SIMULATIONS RESULT ANALYSIS AND COMPARISON

To enhance the speed of the comparator and mitigate the overhead issue, a dynamic double tail comparator based on optimized design principles was proposed. Table 2 demonstrates that the latency and energy consumption of the proposed comparator are significantly lower than those of the standard dynamic comparator and double tail comparator. In comparison to the existing comparator structure,

the suggested circuit exhibits reduced power consumption and lower latency. Noise and input-referred offset voltage serve as resolution-limiting parameters, denoted as VLSB.

$$\text{Where } V_{LSB} = \frac{1}{2^N} \tag{1}$$

Propagation delay is the average delay time of rising and falling propagation delay times and it is measured between the transition of the input and output signals when they reach 50% of the signals level. i.e.

$$T_p = \left(\frac{T_{pr}+T_{pf}}{2}\right) \tag{2}$$

Where T_p =Propagation delay, T_{pr}=Rising propagation delay, T_{pf} =Falling propagation delay
Latched comparators are fast and more suitable to be used in high speed ADCs.

The delay of comparator is calculated as

$$\text{Delay time } T_d = \left(\frac{c}{g_m}\right).\ln\left(\frac{V_{out}}{V_{in}}\right) \tag{3}$$

Where c= parasitic capacitance of transistor, $g_m = \mu_{\frac{n}{p}} c_{ox} \frac{w}{L}(v_{gs} - v_{th})$ = transconductance of transistor

CONCLUSION

This work shows a high-speed latch type comparator design and simulation results in the symica and Ltspice EDA tools utilizing 180 nm CMOS technology, as well as an analysis of offset voltage, power dissipation, and latency of several changed comparator topologies. Among the comparators designed, the double-tail dual-rail latch comparator with back-to-back inverter stage has a low power dissipation. Based on these findings, a double-tail comparator was designed to improve the comparator's performance and eliminate the clock overhead issue. In comparison to a preamplifier-based comparator, dynamic comparators have lower dynamic power dissipation and input offset voltage. The design was produced with the symica and Ltspice simulation EDA tools and 180 nm CMOS technology.

Conflict of Interest

The authors affirmed that the research was conducted without financial backing and declared no conflicts of interest.

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REFERENCE

1. Jeon, H., & Kim, Y. B. (2012). A novel low-power, low-offset, and high-speed CMOS dynamic latched comparator. *Analog Integrated Circuits and Signal Processing*, *70*(3), 337-346.
2. Dhal, L. M., & Pradhan, A. (2013). *Study and Analysis of different types of comparator* (Doctoral dissertation).
3. Babayan-Mashhadi, S., & Lotfi, R. (2013). Analysis and design of a low-voltage low-power double-tail comparator. *IEEE transactions on very large-scale integration (vlsi) systems*, *22*(2), 343-352.
4. Yaqubi, E., & Zahiri, S. H. (2017). Optimum design of a double-tail latch comparator on power, speed, offset and size. *Analog Integrated Circuits and Signal Processing*, *90*(2), 309-319.
5. Purushothaman, A., & Parikh, C. D. (2015). A new delay model and geometric programming-based design automation for latched comparators. *Circuits, Systems, and Signal Processing*, *34*(9), 2749-2764.
6. Bahmanyar, P., Maymandi-Nejad, M., Hosseini-Khayat, S., & Berekovic, M. (2016). Design and analysis of an ultra-low-power double-tail latched comparator for biomedical applications. *Analog Integrated Circuits and Signal Processing*, *86*(2), 159-169.

7. Jain, R., Dubey, A. K., Varshney, V., & Nagaria, R. K. (2017, October). Design of low-power high-speed double-tail dynamic CMOS comparator using novel latch structure. In *2017 4th IEEE Uttar Pradesh section international conference on electrical, computer and electronics (UPCON)* (pp. 217-222). IEEE.
8. Dubey, A. K., & Nagaria, R. K. (2018). Optimization for offset and kickback-noise in novel CMOS double-tail dynamic comparator: A low-power, high-speed design approach using bulk-driven load. *Microelectronics Journal*, *78*, 1-10.
9. Varshney, V., & Nagaria, R. K. (2020). Design and analysis of ultra-high-speed low-power double tail dynamic comparator using charge sharing scheme. *AEU-International Journal of Electronics and Communications*, *116*, 153068.
10. Dubey, A. K., & Nagaria, R. K. (2019). Low-power high-speed CMOS double tail dynamic comparator using self-biased amplification stage and novel latch stage. Analog Integrated Circuits and Signal Processing, 101(2), 307-317.

