STM JOURNALS
Journal of
VLSI Design Tools & Technology
https://journals.stmjournals.com/jovdtt
ISSN: 2249-474X (Online)
ISSN: 2321-6492 (Print)
Volume 16, Issue 1, 2026
January–April
DOI (Journal): 10.37591/JoVDTT

Design and Analysis of Low-Power CMOS Inverter Chains for High-Speed Digital Circuits

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Abstract

This report briefly explains the design process, structure, and evaluation of a Complementary metal-oxide-semiconductor (CMOS) inverter designed using a 45 nm technology process with a focus on its propagation delay and power consumption. Moreover, the CMOS inverter design will be created using the Cadence Virtuoso design environment, along with a post-layout analysis of the design. Performance evaluation of the designed circuit will be carried out through the execution of a transient analysis process, considering the standard operating conditions of the circuit. Based on the simulated results, the proposed design demonstrates a significant reduction in the value of propagation delay compared with existing CMOS inverter designs, along with improved power efficiency. Transient analysis is performed under standard operating conditions to evaluate the inverter's dynamic behavior. The circuit's switching characteristics, such as rise time, fall time, and propagation delay, can be ascertained through this analysis. According to the simulation results, compared to traditional inverter designs, the proposed CMOS inverter design significantly reduces propagation delay, improving overall speed performance. Furthermore, the leakage power analysis of the CMOS inverter circuit has been carried out under different operating conditions of the P-type Metal-Oxide-Semiconductor (PMOS) and N-type Metal-oxide-semiconductor (NMOS) devices of the circuit, with improved insights into the value of the leakage current. The results prove the improved energy efficiency of the designed CMOS inverter circuit with optimal power-delay performance suitable for very large scale integration (VLSI) designs.

Keywords: CMOS inverter, inverter chains, leakage power analysis, 45 nm technology

INTRODUCTION

The continuing progress of Complementary metal-oxide-semiconductor (CMOS) technology has facilitated the development of digital integrated circuits that are not only high-performing but also energy-saving devices. Among the numerous digital components, the CMOS inverter is considered the most critical; hence, the power, speed, and reliability of advanced logic circuits are significantly influenced by it. The performance of inverter chains is a significant issue in modern VLSI systems because they are extensively used in buffering, signal restoration, and clock distribution networks [–13].

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Received Date: March 02, 2026
Accepted Date: March 09, 2026
Published Date: April 02, 2026

Citation: Anupriya V., Hemalatha R., Kaviya Sri A., Madhumitha P., Nanthitha S. Design and Analysis of Low-Power CMOS Inverter Chains for High-Speed Digital Circuits. Journal of VLSI Design Tools & Technology. 2026; 16(1): 40–57p.

Power dissipation has become an important issue in the development of digital circuits owing to advancements in deep submicron technology. The switching speed and leakage current increase considerably owing to the extreme scaling down of the transistors. Therefore, it is essential to achieve a proper trade-off between delay and power while building low-power VLSI circuits. The maximum [4–7] achievable speed in digital circuits is usually accompanied by the highest power dissipation and thus requires careful optimization at the circuit level [8, 9].

Many proposals have been made in the literature for low-power and high-speed inverter designs, including the sizing of transistors, methods for leakage reduction, and optimizations at the logic level. However, many current studies tend to concentrate on either delay or power minimization without addressing the specific leakage characteristics under different operational scenarios [10, 11]. Furthermore, some methods rely on relative performance improvements without a complete transistor-level evaluation.

The construction of a 45 nm technology node CMOS inverter chain with high-speed and low-power consumption is presented. In this study, the proposed architecture provides a detailed study of the leakage power of both P-type Metal-Oxide-Semiconductor (PMOS) and N-type Metal-Oxide-Semiconductor (NMOS) while focusing on enhancing the power-delay trade-off [12, 13].

LITERATURE SURVEY

Survey

In previous studies, a low-power dynamic CMOS inverter design with the Leakage control transistor and LECTOR-B methods applied in 45 nm technology has already been reported. The proposed method incorporates additional leakage control transistors to mitigate the static power loss of CMOS inverters. The LECTOR-B method was shown to yield better power-delay performance compared to the traditional inverter, mainly because of the reduced leakage power. However, the presented results were largely given in terms of percentage improvements in the power delay and power-delay product, without providing absolute performance metrics. Moreover, the study was limited to the performance of a single inverter and did not consider the behavior of inverter chains or a detailed examination of transistor-level leakage under different operating conditions. In addition, layout-level validation and post-layout performance evaluation were not addressed. These limitations necessitated the present study, which focuses on the design and analysis of a series of low-power CMOS inverters with improved power-delay characteristics and a thorough leakage examination using an integrated design and verification process [14–16].

Literature Summary

The reviewed literature places a strong emphasis on the significance of optimizing leakage reduction. This is particularly significant for deep submicron technologies. Recent approaches have indicated that the application of control measures for leakage reduction can significantly reduce the consumption of leakage power while providing a significant improvement to the overall energy efficiency of the system. However, as observed in most of the literature that deals with this theme, most of it is still centered on the evaluation of the performance of individual inverters [21]. Moreover, most studies present the results in terms of relative percentage improvement as opposed to absolute measurements. In addition to this, it can be seen that the evaluation of the inverter chain, the entire power and delay evaluation, as well as leakage evaluation, have to be conducted to ensure a better implementation in high-speed digital circuits [17–19].

PROPOSED METHODOLOGY

CMOS Inverter Design

The basic element of the proposed inverter chain is a stand-alone CMOS inverter consisting of PMOS and NMOS complementary transistors in the pull-up and pull-down modes, respectively. The dimensions of the transistors are optimized in such a way as to obtain the lowest propagation delay, at the same time keeping the dynamic and static power consumption very low (Figure 1). The inverter was processed in the 45 nm technology node, and the supply voltage was chosen to guarantee dependable switching and proper logic-level transitions. This simple inverter layout forms the basis for constructing an inverter chain, which allows for detailed studies of the delay, power, and leakage under actual circuit conditions [20].

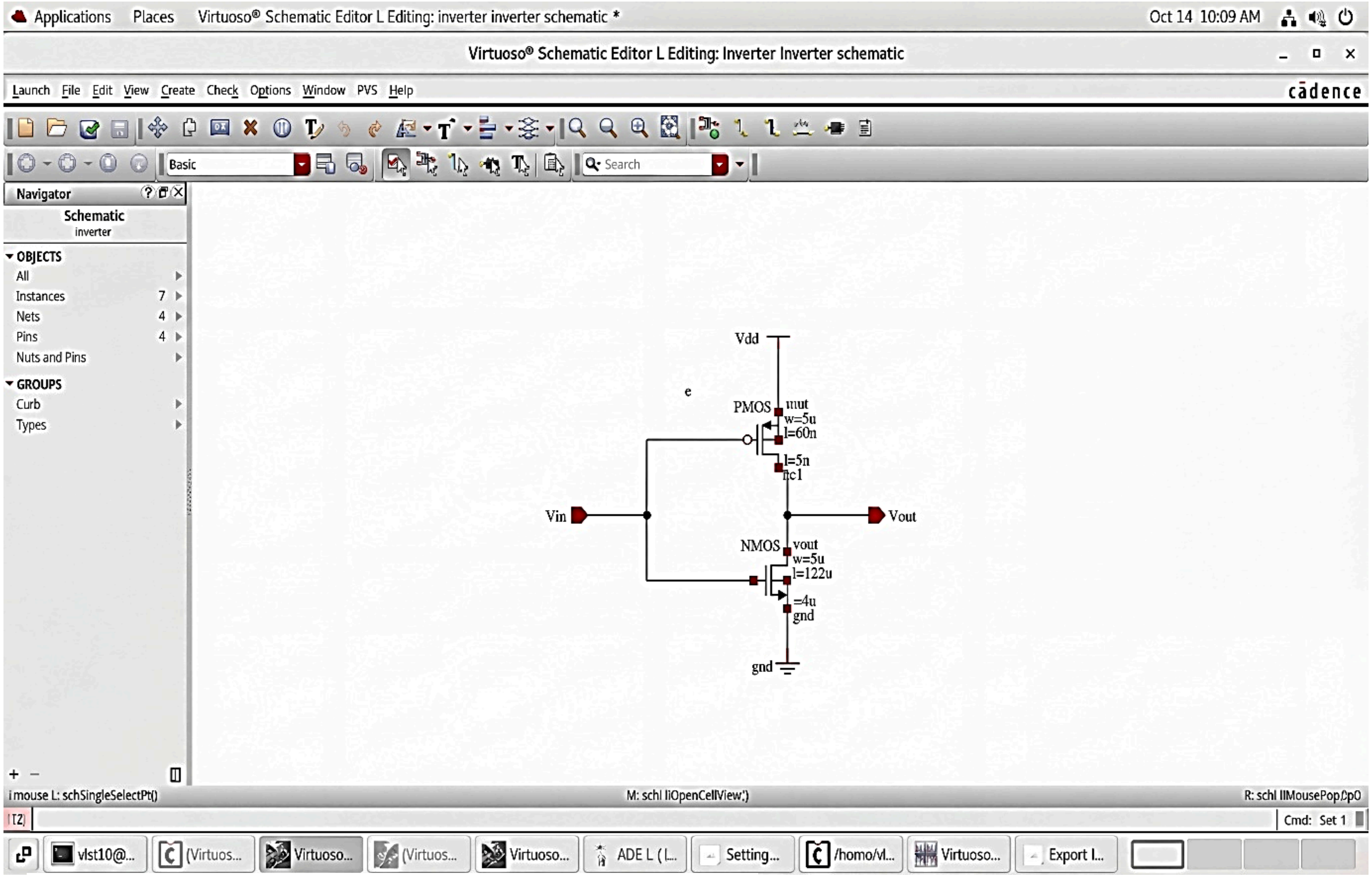

Figure 1. Schematic of a CMOS inverter implemented in 45 nm technology.

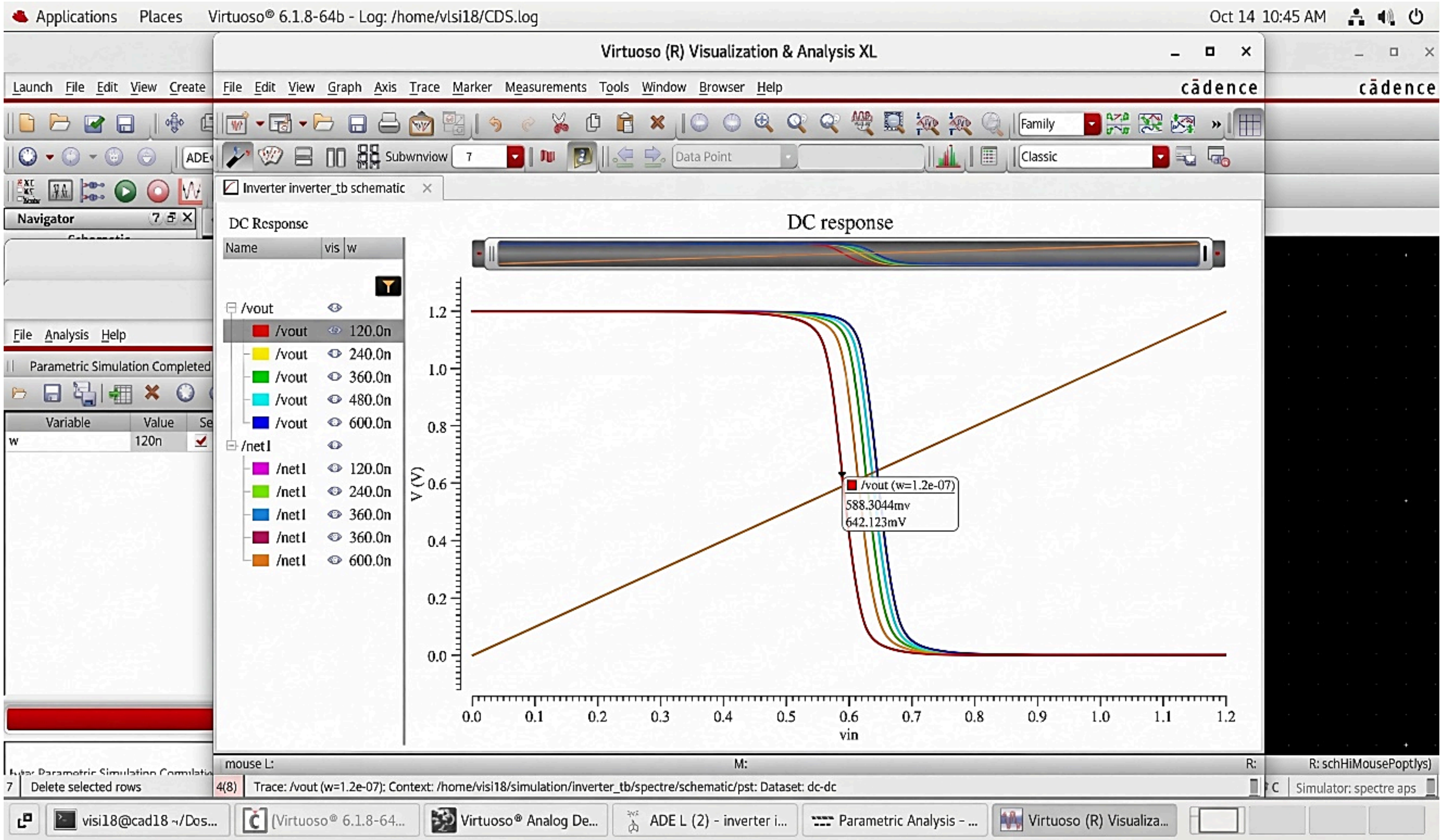

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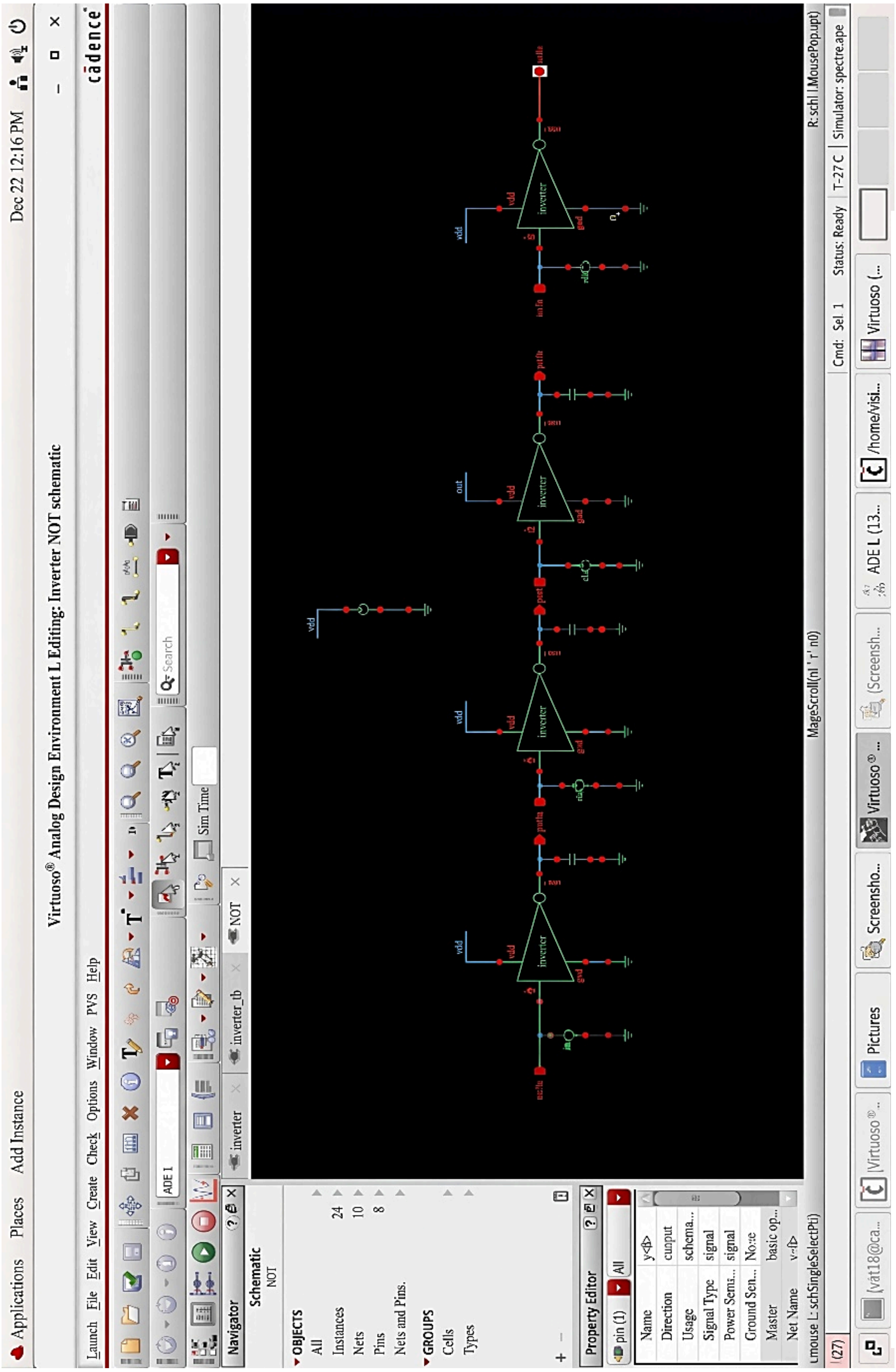
Figure 2. Parametric analysis of W/L ratio.



Property	Value
Name	y
Direction	output
Usage	schema...
Signal Type	signal
Power Sens...	signal
Ground Sen...	None
Master	basic op...
Net Name	y

Objects	Count
Instances	24
Nets	10
Pins	8

Cmd: Sel: 1 Status: Ready T=27 C Simulator: spectre.ape

Figure 3. Schematic of CMOS inverter chain implemented using multiple cascaded inverter stages in 45 nm technology.

Transistor sizing and switching threshold analysis. The goal of choosing the W/L ratio of the transistors is to guarantee that the switching threshold voltage is reached at its ideal value. The voltage value at which the switch toggles between states is indicated by the voltage transmission curve, where $V_{in} = V_{out}$. The developed inverter circuit diagram shows the $V_{in} = V_{out}$ condition at approximately 0.6 V. This shows that the voltage transmission curve is nearly symmetrical [22]. The DC voltage gain can be obtained using the slope of the voltage transfer curve to calculate the ratio of the change in the output voltage to the change in the input voltage. The DC voltage gain in this case (Figure 2).

Switching Threshold Voltage (Vm)

$V_{in} = V_{out}$
W = 120 nm, V_{in} = 588.3 mV, V_{out} = 642.1 mV
$Vm \approx 0.6$ V

DC Gain

$$Av = \frac{dvout}{dvin}$$

$Av \approx -13$

Inverter Chain Configuration

The CMOS inverter chain is a series of identical inverter stages connected one after another, where the output of the first inverter is connected to the input of the second stage and so on. This configuration provides an accurate evaluation of the total propagation delay, power loading effects, and signal quality during dynamic operation scenarios. All the inverters in the chain use transistors of the same size, which ensures that the performance is the same throughout the different stages (Figure 3). The chain of inverters receives a pulse input at the first stage, and the output response is detected at the following stages of the chain. To mimic the interconnect and fan-out effects typically found in real digital circuits, the output nodes are connected to load capacitances. The proposed methodology captures delay accumulation, dynamic power dissipation, and switching behavior, which are pertinent to high-speed digital systems, by studying the inverter chain rather than a single inverter [23].

Simulation Setup

The designed CMOS inverter and inverter chain were tested in the Cadence Virtuoso Analog Design Environment (ADE) using a 45 nm process technology. The dynamic switching characteristics of the inverter chain were evaluated by conducting a transient analysis. A pulse input signal with appropriate rise and fall times was applied to the first inverter, and the output waveforms were captured at different points along the chain (Figure 4). Simulations were performed at a standard temperature and supply voltage to ensure that the results were consistent and reliable. The fundamental performance parameters, including propagation delay, rise time, fall time, and power dissipation, were derived from the simulated voltage and current waveforms. Static power is measured under quiescent conditions, whereas dynamic power is computed by averaging the supply current during switching events. The steady-state and transient characteristics of the proposed inverter were thoroughly and accurately assessed in this simulation environment [24].

Propagation Delay and Power Measurement

The propagation delay is determined by measuring the time interval between the 50% transition points of the input and output voltage signals during a transient simulation. For each inverter stage in the sequence, delays for both low-to-high (tpLH) and high-to-low (tpHL) transitions were reported. To determine the average propagation delay, which indicates the total switching speed of the inverter chain, the mean of these two values is calculated.

The power consumption was determined by measuring the current drawn from the power supply while the circuit was operating. Dynamic power is produced during active switching conditions by taking the average of the supply current over a complete input cycle, whereas static power is measured during the steady state when the input is constant at a particular logic level. This approach separates the dynamic and static power components without disturbing the circuit performance [25].

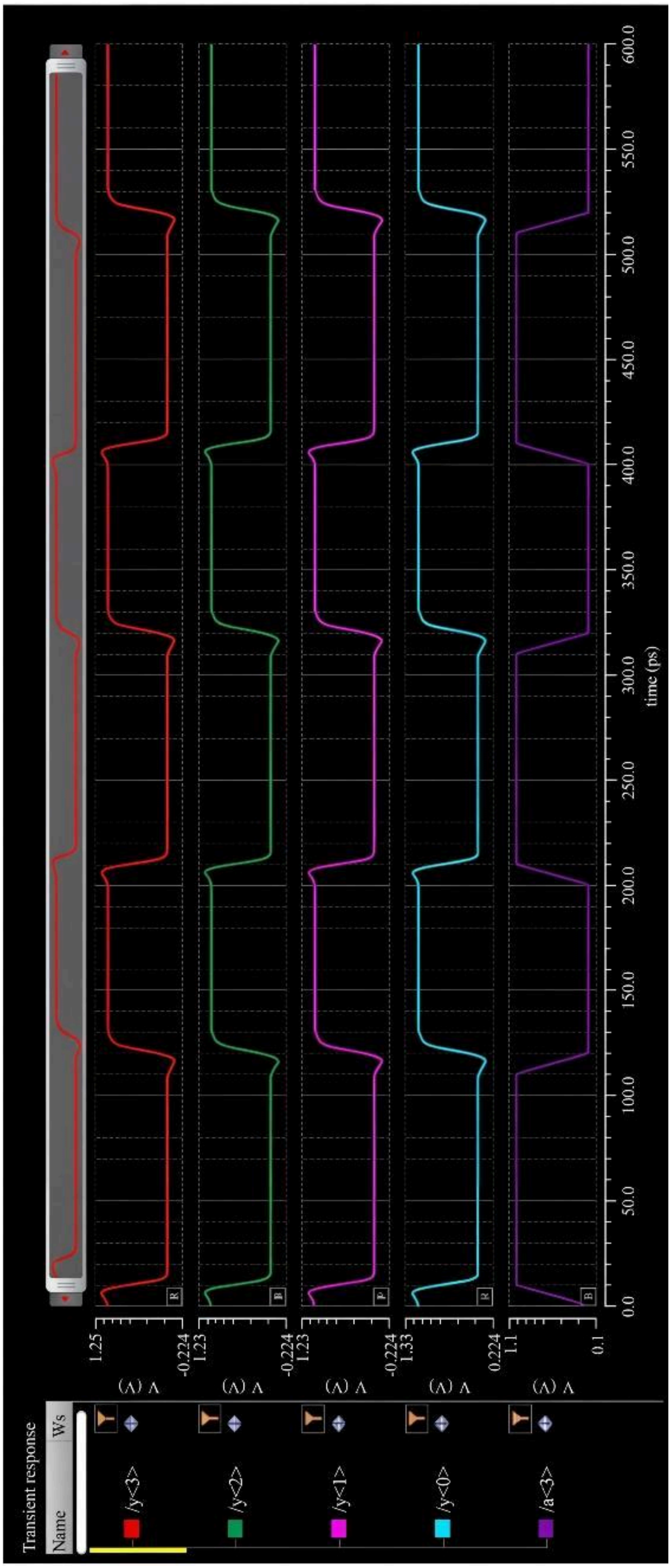


Figure 4. Output of the CMOS inverter chain.

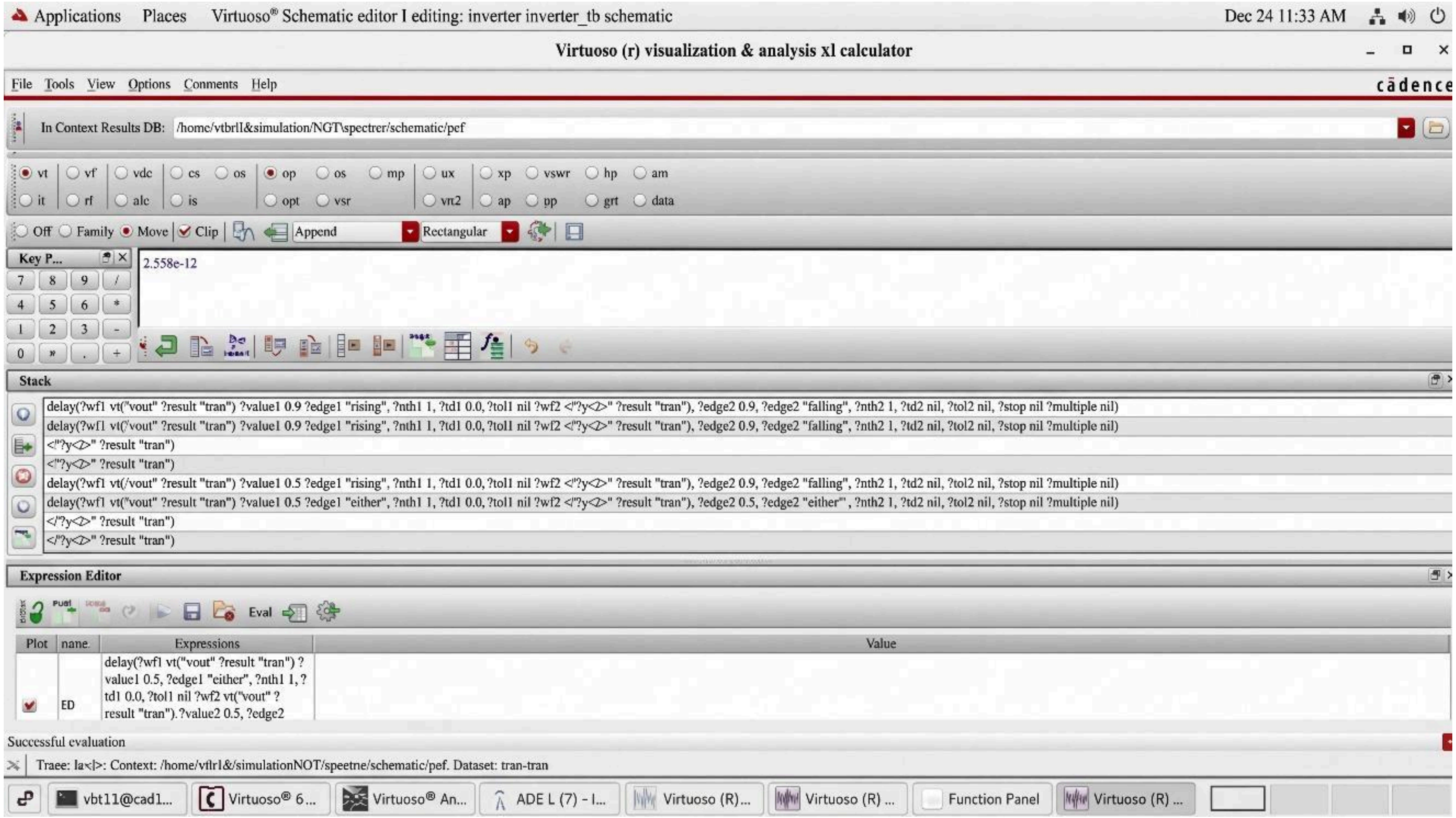


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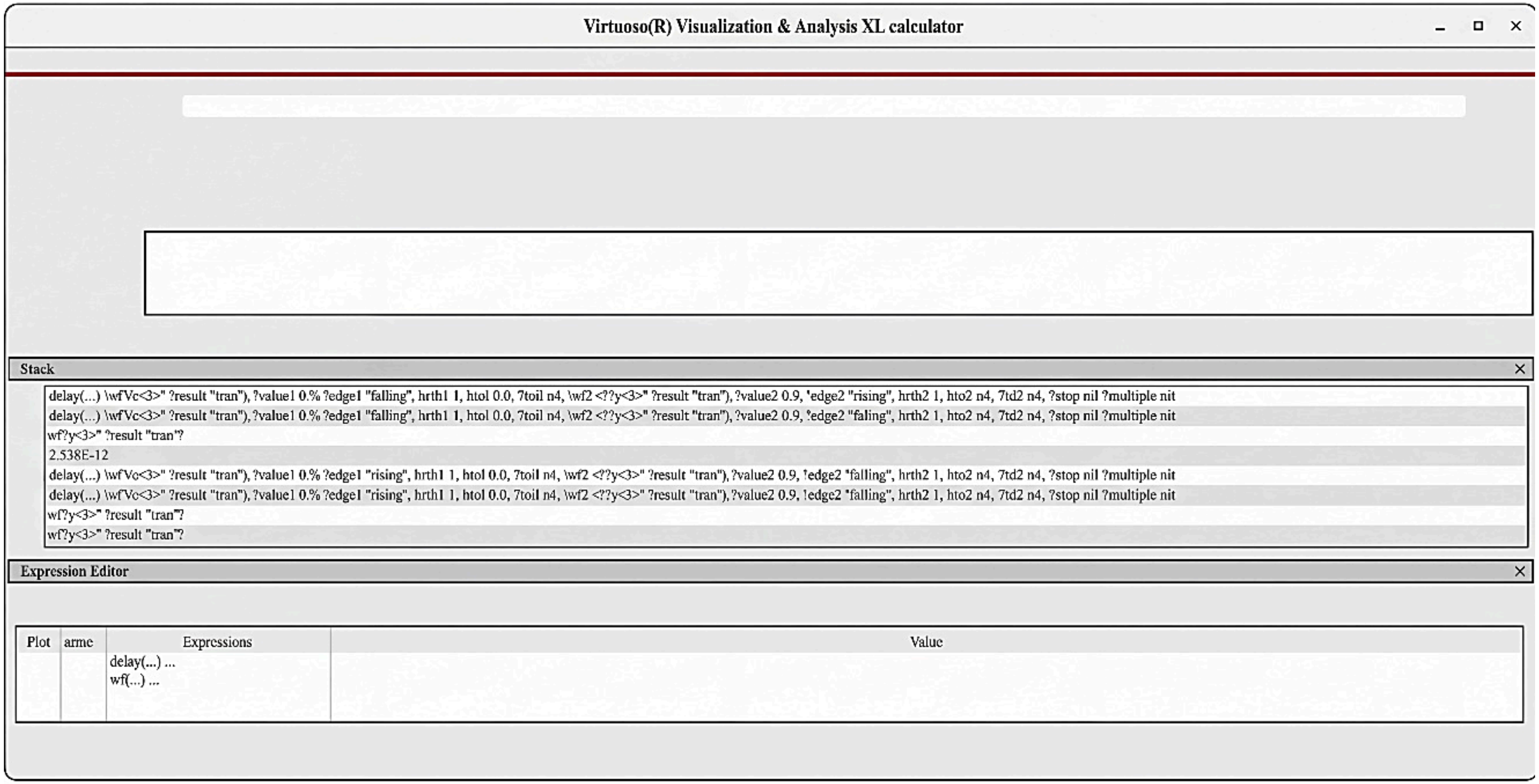
Figure 5. tpHL (rising to falling).



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delay(...) \wfVc<3>" ?result "tran"), ?value1 0.% ?edge1 "falling", hrth1 1, htol 0.0, 7toil n4, \wf2 <??y<3>" ?result "tran"), ?value2 0.9, 'edge2 "rising", hrth2 1, hto2 n4, 7td2 n4, ?stop nil ?multiple nit
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Figure 6. tpLH (falling to rising).

Leakage Power

Leakage power analysis involves the assessment of PMOS and NMOS transistors in both their conducting and nonconducting states. During steady-state operation, the leakage currents were measured to study the contributions of subthreshold and gate leakage. Separate measurements were performed for each of the four cases, PMOS-ON, PMOS-OFF, NMOS-ON, and NMOS-OFF, to obtain a detailed understanding of the leakage properties at the transistor level in the inverter chain.

RESULT AND DISCUSSION

In this section, the simulation results for the proposed CMOS inverter chain, which was built using 45 nm technology, are displayed. The propagation delay, power consumption, and leakage characteristics were used to evaluate the performance of the design using the measurement techniques described in Section III. The results were then analyzed and compared with those of previous studies to show how well the proposed approach lowers the latency while using little power (Figure 5).

Propagation Delay

The propagation delay of the inverter chain was extracted from the transient simulation data by taking the average of the low-to-high and high-to-low transition delays. The proposed inverter chain has an average propagation delay of 101.54 ps. This shows a significant improvement compared with the previously reported delay of 140.20 ps for conventional inverter designs. One of the main reasons for the significant delay reduction is the improved aspect of transistor sizing, switching threshold characteristics, and reduced effective capacitive loading at the output of inverter cascades. The results confirm that the proposed design is the best fit for high-speed digital circuit applications (Figure 6).

$$tp = \frac{tpLH + tpHL}{2}$$

$$tp = \frac{4.823 \times 10^{-12} + 2.538 \times 10^{-12}}{2}$$

$$tp = 25.384 \text{ ps}$$

$$T_{total} = N.tp$$

Where, N is number of inverter chains.

$$T_{total} = 4 \times 25.384$$

$$T_{total} = 101.54 \text{ ps}$$

Power Consumption Analysis

The total power is partitioned into dynamic and static parts to evaluate the power consumption. The maximum power dissipation of the proposed inverter chain was 14.60 nW. Of this, the dynamic power part amounts to 14.597 nW, and the static power loss is limited to 3.171 pW (Figure 7). The use of scaled CMOS technologies to minimize delay often results in increased dynamic power; however, the proposed design maintains a favorable power-delay trade-off. The very low static power indicates excellent management of leakage currents, which makes the design suitable for low-power digital systems (Figure 8).

Average Power

Expression: average(getData(“pwr”?result “tran”))
Value: 14.60E-9

To investigate the power consumption characteristics of the CMOS inverter, the power dissipation in the ON and OFF states of both PMOS and NMOS transistors was measured. The data was acquired through transient simulation and calculator functions in Cadence Virtuoso. The results indicate that the PMOS transistor is responsible for a larger amount of leakage power than the NMOS transistor, particularly in the OFF state. The OFF-state power of the PMOS transistor increases as the subthreshold and gate leakage currents become predominant at deep submicron technology levels.

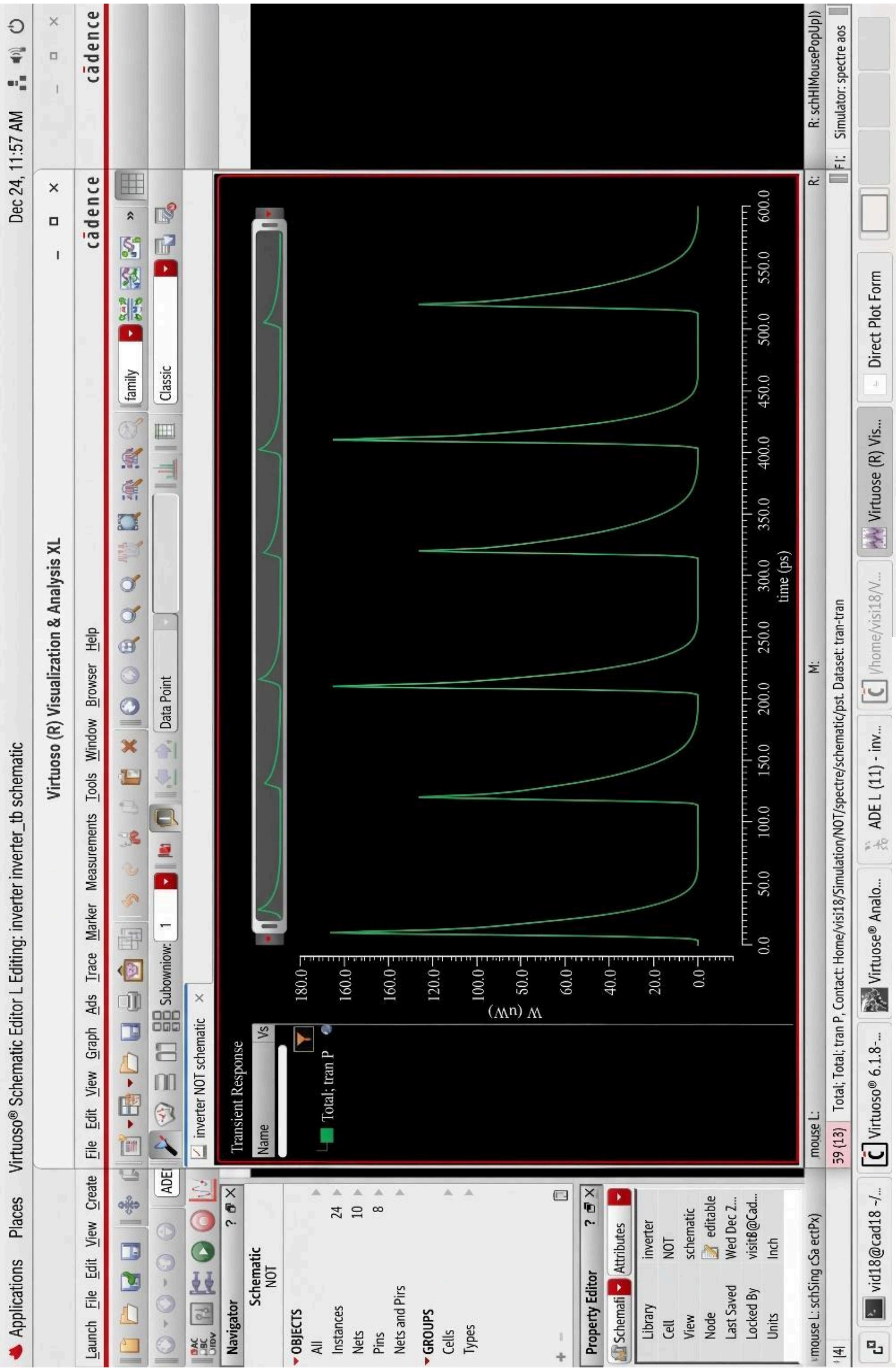

Figure 7. Transient waveform for tPLH measurement of the CMOS inverter.

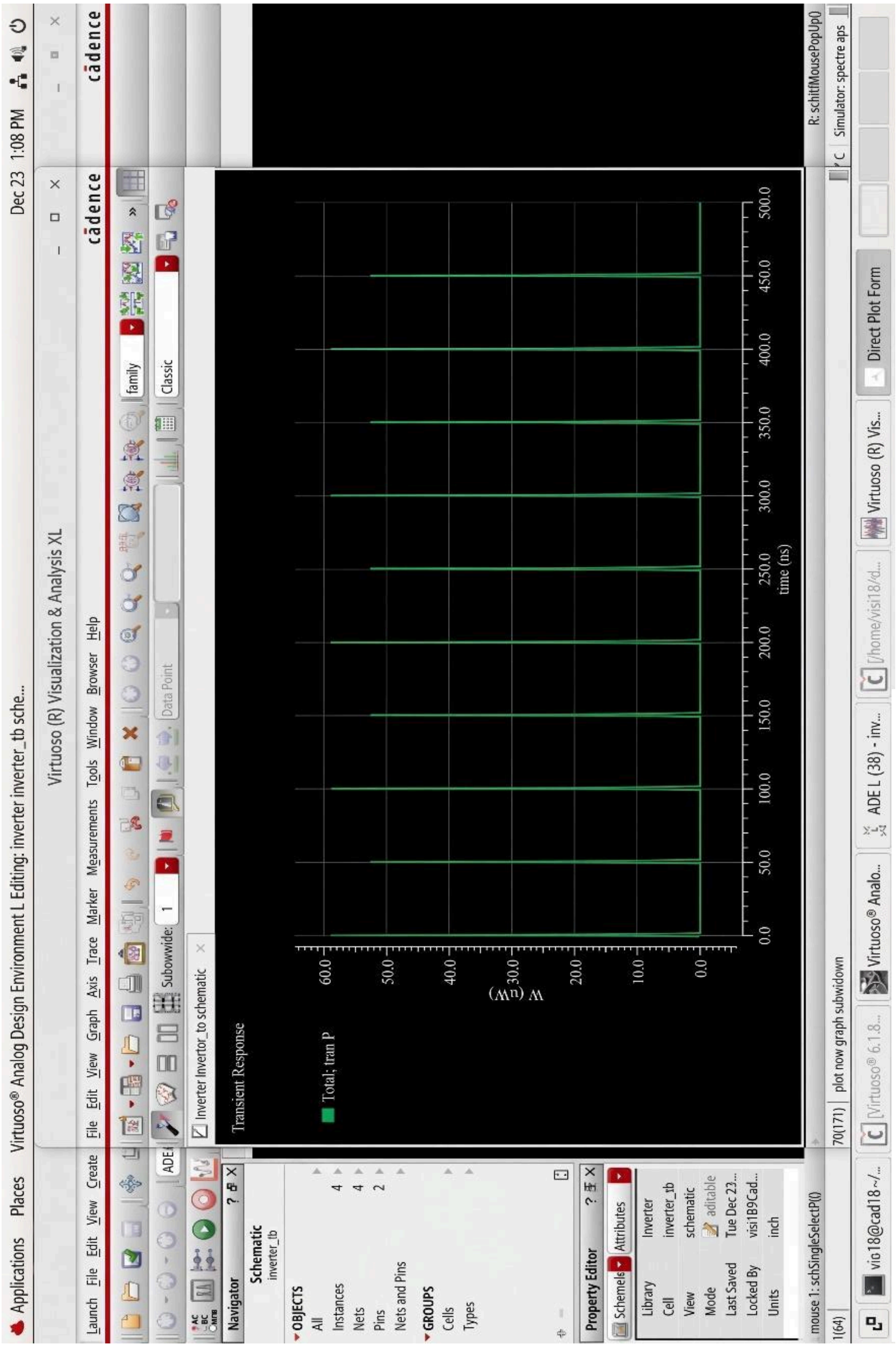

Figure 8. Transient power waveform of the CMOS inverter chain.

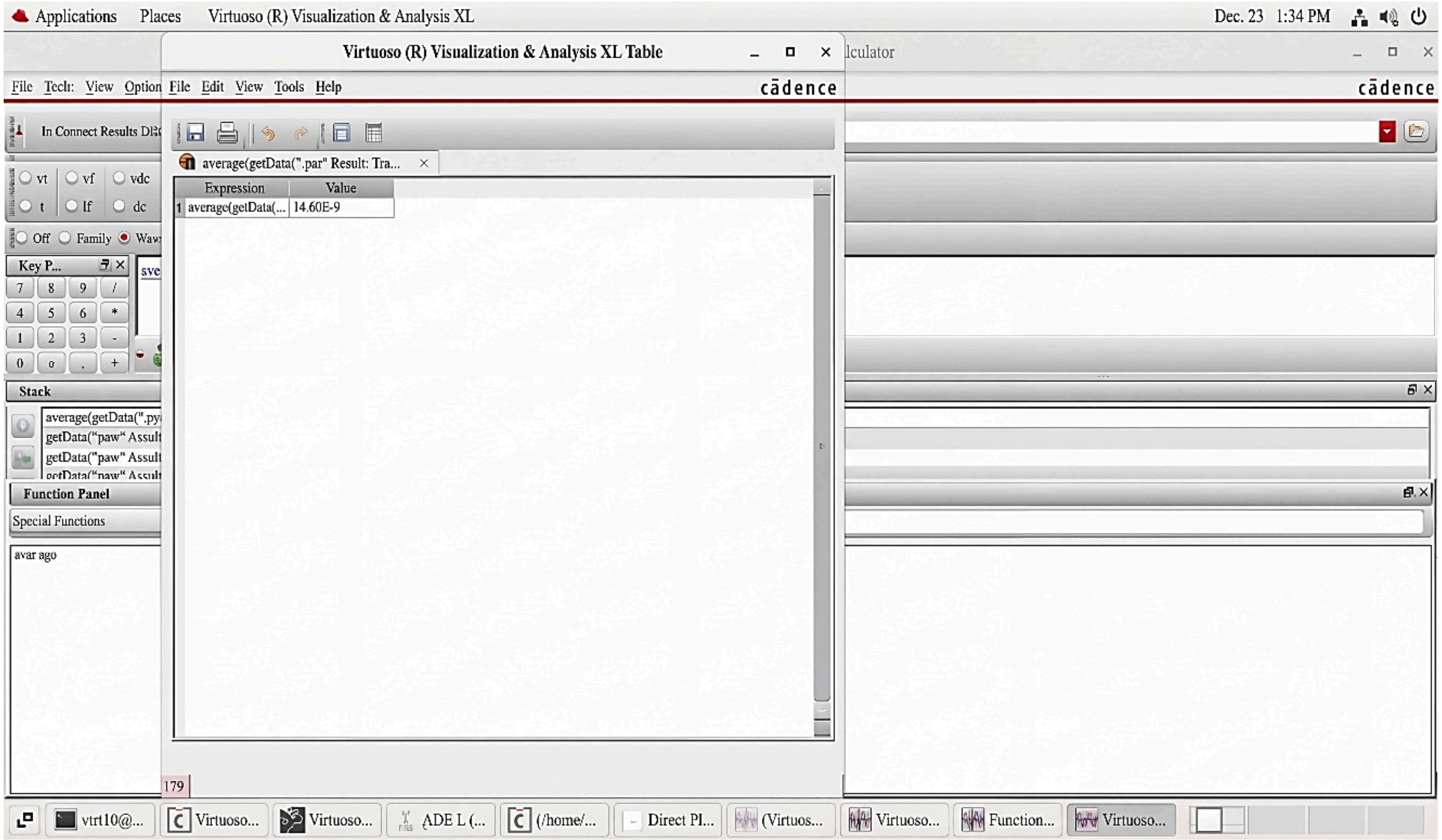

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Figure 9. Average power computation using Cadence Virtuoso ADE.

Table 1. Propagation delay (tpLH and tpHL) variation with supply voltage for the CMOS inverter.

Voltage	tpLH	tpHL
1.1 V	4.823 ps	2.538 ps
1.8 V	3.05 ps	1.62 ps

Table 2. ON- and OFF-state power consumption of CMOS inverter transistors.

Transistor	State	Power
PMOS	ON	1.339×10^{-12}
PMOS	OFF	3.0581×10^{-10}
NMOS	ON	1.853×10^{-21}
NMOS	OFF	1.132×10^{-15}

Table 3. Comparison between conventional CMOS/existing low-power techniques and the proposed low-power CMOS inverter chain.

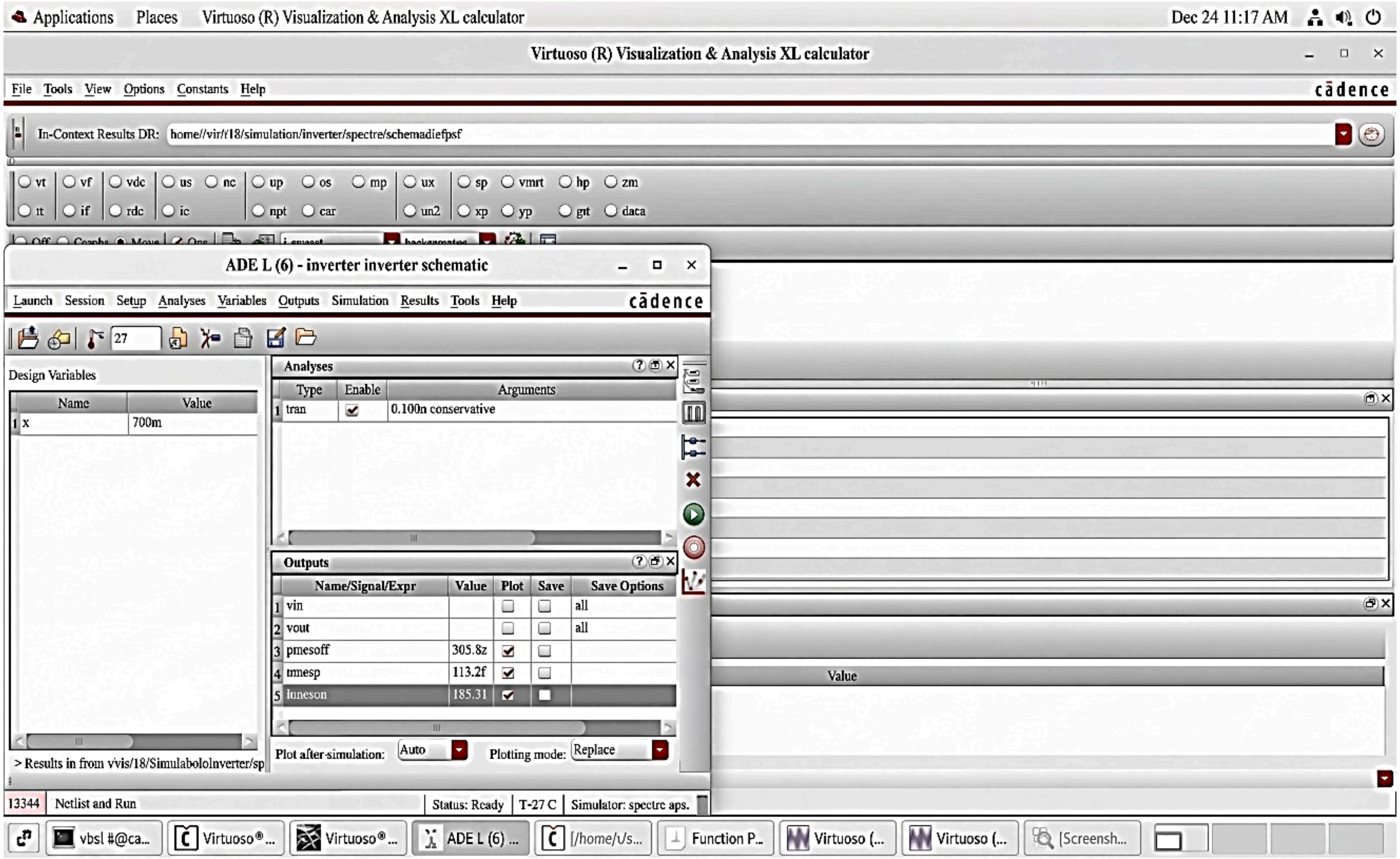
Parameters	Conventional CMOS/existing low-power techniques	Proposed low-power CMOS inverter chain
Technology node	90 nm/180 nm	45 nm
Supply voltage	1.0–1.2	1.8 V
Static power	High	305.9 pw
Dynamic power	μω range	14.29 nw
Average propagation delay	40–60 ps	25.38 ps
Total delay	140.200 ps	101.54 ps
Power delay	Moderate to high	Significantly reduced
Overall speed	Moderate	Increased
Power efficiency	Average	High

In contrast, the NMOS transistor exhibits almost negligible power dissipation in the ON state and somewhat less leakage in the OFF state. This confirms that the PMOS leakage characteristics essentially control the static power dissipation of the inverter. The ON-state power reflects the conduction properties during switching, whereas the OFF-state power indicates the static leakage power when the transistor is inactive. These findings demonstrate that to drastically lower static power dissipation, leakage reduction strategies such as LECTOR and LECTOR-B designs must be used in the design of CMOS inverters. For low-power VLSI applications, controlling the leakage currents in both PMOS and NMOS transistors can significantly improve the total power efficiency of the inverter (Figure 9).

Leakage Power Analysis

The leakage power was assessed at the transistor level by analyzing the PMOS and NMOS parts in both the ON and OFF conditions. This detailed study reveals not only the standby power distribution but also the leakage diffusion across the inverter chain. The measured leakage power values for the different transistor states are listed in Table 1. The results indicate that the leakage of PMOS in the OFF state has a larger influence on the total leakage than NMOS devices, which is in line with the expected behavior in deep submicron CMOS technologies. Nonetheless, the total leakage power remained low and did not significantly contribute to the overall power consumption (Figure 10).

P_{static} = PMOS-OFF + NMOS-OFF
P_{static} = 305.8 pW + 0.1132 pW
$P_{static} \approx$ 305.9 pW
$P_{avg} = P_{static} + P_{dynamic}$
$P_{dynamic} = P_{avg} - P_{static}$
$P_{dynamic}$ = 14.60 nW − 0.3059 nW
$P_{dynamic} \approx$ 14.29 nW



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Design Variables

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Analyses

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Outputs

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2	vout		☐	☐	all
3	pmesoff	305.8z	☑	☐	
4	nnesp	113.2f	☑	☐	
5	luneson	185.31	☑	☐	

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Figure 10. ON- and OFF-state power consumption of CMOS inverter transistors.

Comparative Analysis

Table 2 compares the proposed low-power CMOS inverter chain with classic CMOS and previously mentioned low-power techniques. Table 3 shows the progress of the proposed low-power CMOS inverter chain. While previous research has largely focused on leakage reduction techniques, such as LECTOR, LECTOR-B, Sleepy CMOS, and Multi-Threshold CMOS (Complementary Metal-Oxide-Semiconductor), at technology nodes of 90 and 180 nm, the proposed design works at a node of 45 nm and employs optimal transistor sizing and inverter chaining.

The proposed inverter chain compares favorably with the reported ranges in the literature through a significant reduction in static power to only 140.200 pW and a relatively small total propagation delay of 101.54 ps. Additionally, the power consumption during maximum operation is limited to a few nanowatts, which results in a lower power-delay product (PDP). The results indicate not only a higher speed but also better power efficiency, making the design suitable for low-power and high-speed digital applications.

CONCLUSION

A low-power CMOS inverter chain was developed and evaluated using 45 nm technology, targeting decreased power consumption and propagation delay. The overall power was thoroughly assessed by dividing it into static and dynamic parts. Static power, which is the part due to the leakage of PMOS and NMOS transistors when they are OFF, was found to be only 305.81 pW, indicating very low leakage. The dynamic power was found to be 14.29 nW, which means that the power consumption owing to switching activity dominates the total power consumption rather than leakage.

Propagation delay testing showed that the new inverter reduced tpLH and tpHL, resulting in faster switching characteristics at high supply voltages. The tested inverter chain delay of 101.54 ps is a significant improvement over the 140.200 ps delay of the existing designs. This indicates that the performance was accelerated by the interconnection of the inverters and optimal sizing of the transistors.

The proposed design is suitable for high-speed and low-power digital applications because it reduces both delay and power consumption, which also leads to a significant improvement in the PDP. An important component of the next generation of low-power VLSI systems and high-speed digital circuits, the suggested low-power CMOS inverter chain is an excellent solution that does not sacrifice performance or power efficiency.

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