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A Majority Function Based Full Subtractor

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Abstract

In the present landscape of very large-scale integration (VLSI) technology, the imperative to implement Boolean functions with minimal gate count remains a cornerstone of efficient circuit design. This pursuit has only grown more critical with the evolution of low-power design strategies, which now offer significantly enhanced benefits compared to traditional approaches. The trifecta of performance, affordability, and dependability continue to drive innovation in this field, shaping the trajectory of technological advancements across various sectors. Of particular importance is the escalating recognition of power dissipation as a pivotal factor in shaping competitive markets, such as those for wireless applications, laptops, and portable medical equipment. As consumer demand for efficiency and longevity in battery-powered devices intensifies, reducing power consumption has become synonymous with improving product usability and market competitiveness. This paper contributes to this ongoing discourse by focusing on the comparative analysis of multiple full subtractor circuits, evaluating their transistor count and overall power consumption. Central to our investigation is the introduction of a novel full subtractor design based on majority logic, which promises substantial advancements over established methodologies. By leveraging the inherent advantages of majority logic, our proposed circuit aims to streamline operations, minimize gate complexity, and ultimately enhance power efficiency—a critical consideration in contemporary VLSI design paradigms. Through meticulous experimentation and comparative study, we highlight the distinct advantages of our proposed majority logic-based full subtractor. Not only does it exhibit a reduced transistor count and lower power consumption compared to traditional designs, but it also demonstrates robust performance metrics across varying operational conditions.

Keywords: VLSI, majority function, leakage power, MTCMOS, threshold

INTRODUCTION

In contemporary digital circuit design, the process of subtracting two single-bit numbers typically begins with a half subtractor that handles basic subtraction operations. However, when more complex scenarios arise, such as subtracting three single-bit numbers, or when a borrow-in mechanism is necessary, a full subtractor circuit becomes indispensable. Unlike its half-subtractor counterpart, a full subtractor can handle three inputs (minuend, subtrahend, and borrow-in) to produce two outputs: the difference and a borrow-out signal.

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Traditionally, full subtractors have been implemented using a combination of logic gates and flip-flops, which require a significant number of transistors for their operation. Recent advancements in circuit design have explored alternative methodologies to enhance efficiency and reduce component counts. One such innovation is the application of the majority of logic functions in the design of full subtractors.

The majority function, which is a fundamental concept in digital circuitry, outputs a logic high [1] when most of its inputs are high (1s). This principle

was leveraged in our proposed full subtractor design to streamline operations and minimize transistor usage. By integrating the majority logic, our design reduces the transistor count to 12, compared with 20 transistors in traditional designs and 14 transistors in another existing model [2]. This reduction in transistor counts not only contributes to circuit simplification but also enhances power efficiency and operational reliability.

The schematic diagram (Figure 1) illustrates the generalized structure of a majority function, showcasing its fundamental components and operational principles. This diagram serves as a visual aid in understanding how majority logic can be effectively integrated into full subtractor designs to optimize performance.

In conclusion, this paper presents a novel approach to designing full subtractors using majority logic, demonstrating its efficacy in achieving substantial reductions in transistor counts while maintaining robust functionality. By pushing the boundaries of conventional circuit design paradigms, we aim to foster advancements in digital logic implementation, paving the way for more efficient and versatile applications of VLSI technology and beyond.

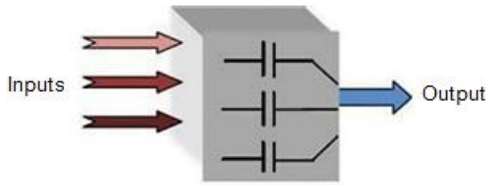

Figure 1. Majority function.

Existing Methodology

20 Transistor Model

Various approaches have been proposed in the recent literature to enhance the efficiency of both full adders and subtractors by reducing the transistor count, thereby addressing concerns related to Power consumption, delay, and fabrication costs [1, 3,4]. Figure 2 shows a detailed transistor-level circuit diagram of a Full Subtractor utilizing 20 transistors. This design not only achieves reduced power consumption, but also offers advantages such as lower leakage current and a smaller footprint compared to static CMOS Full Subtractor implementations, owing to its lower transistor count [5].

In this specific configuration, six transistors are dedicated to computing the difference, and an additional ten transistors are employed to derive the borrow output, facilitated by the inversion of four transistors [5]. These design choices reflect optimizations aimed at maximizing efficiency within the given technological constraints.

The dimensions of transistors are crucial parameters that affect the performance and characteristics of the circuit. In this case, the PMOS and NMOS transistors had lengths of 0.25µm. The PMOS transistor width was specified as 2.175µm, whereas the NMOS transistor width was 4.175µm. These dimensions were carefully selected to balance the speed, power consumption, and area considerations in the design process [6].

Overall, this detailed analysis underscores the importance of transistor-level optimization in achieving efficient digital circuit designs. By leveraging advancements in transistor sizing and configuration, designers can achieve significant improvements in the performance metrics that are crucial to modern VLSI implementations. Ongoing research and development continue to drive innovations aimed at meeting the evolving demands of digital technology applications.

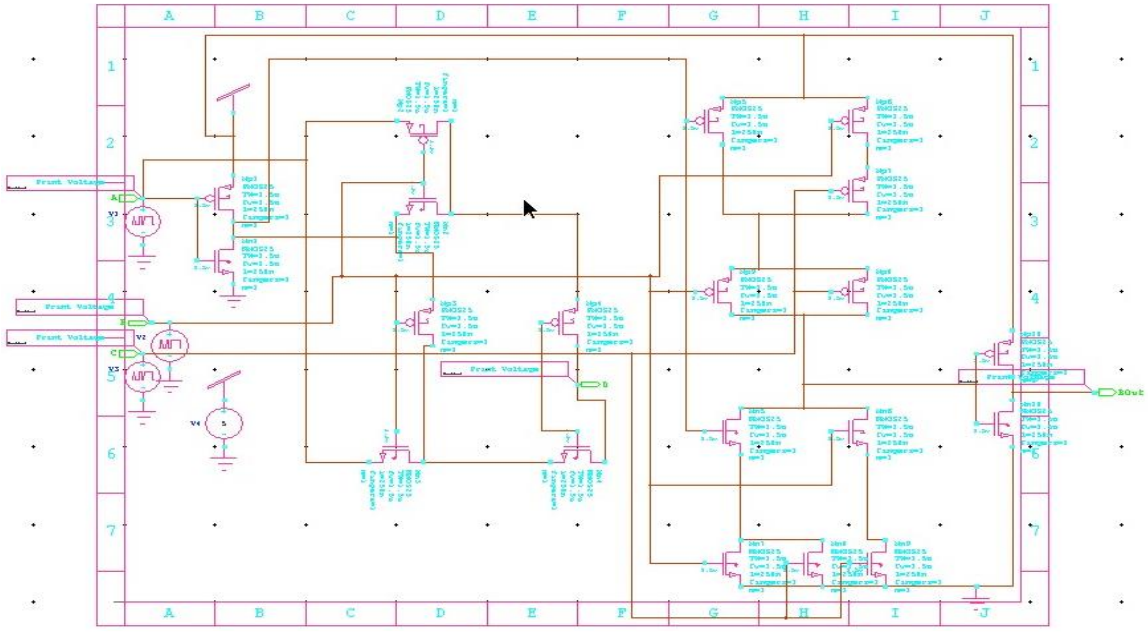

Figure 2. Full subtractor with 20 transistors.

Output of 20t Model of Full Subtractor

After simulating the circuit of 20 transistors model the Tanner EDA tool (250 nm), the output is as shown in Figure 3. Where the "difference" part has a little noise/distortion. This can be rectified by changing the input parameters or adjusting the width of the transistors.

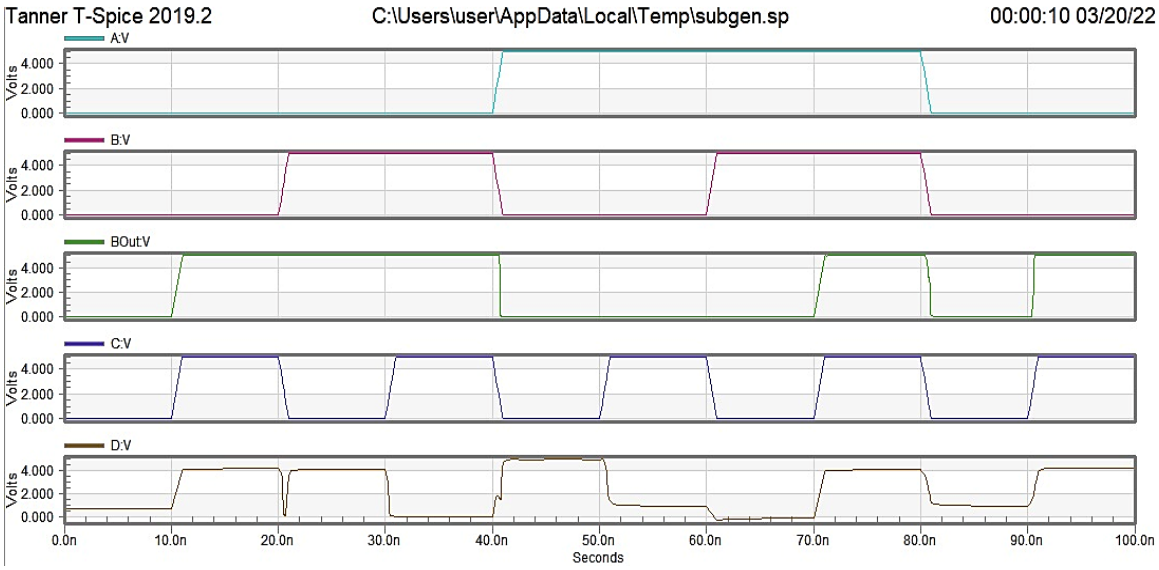

Figure 3. Output of full subtractor with 20 transistors.

14 Transistors Model

Figure 4 shows a 1-bit Full Subtractor transistor-level circuit. The six-transistor XNOR-XOR modules generated two intermediate signals that were fed into the MUX (2 × 1). The two intermediate signals produced by the above logic gates serve as inputs to the MUX (2 × 1), while the 3rd input serves as the multiplexer's selection line. The output of the multiplexer is used to calculate the difference between inputs A, B, and C. Two AND gates and one OR gate are used to create Borrow [7–11]. Here, the length, width, and width of the PMOS, NMOS, and PMOS are 0.25, 2.175, and 4.175 µm, respectively.

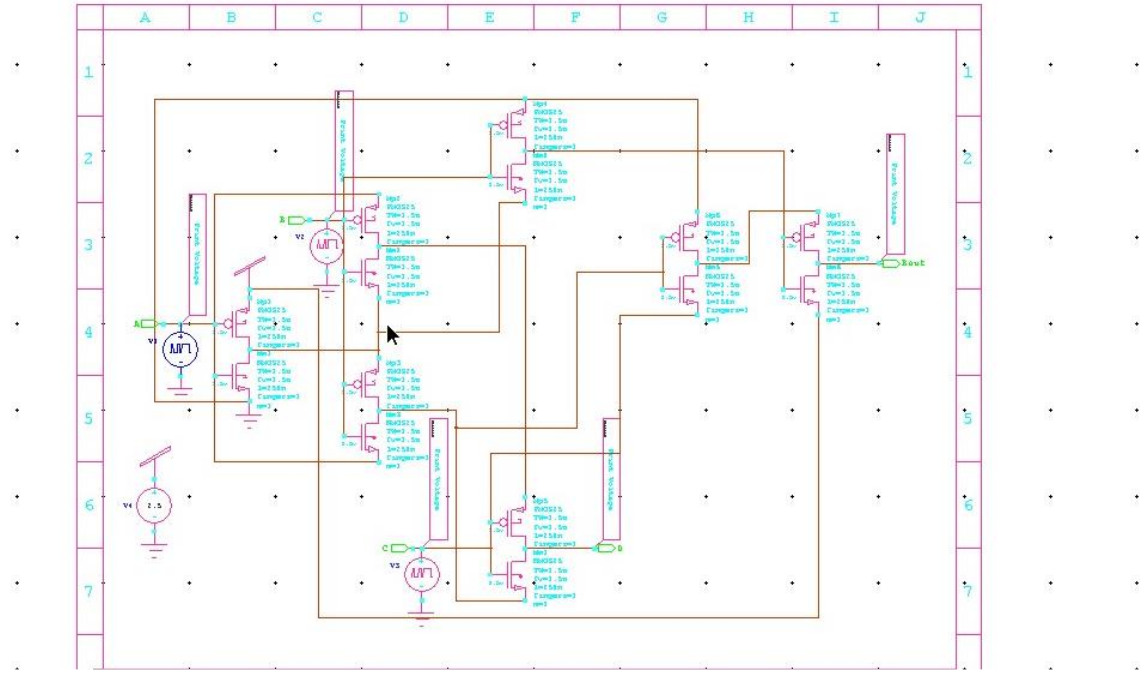

Figure 4. Full subtractor with 14 transistors.

Output of 14T Model of Full Subtractor

After simulating the circuit of 14 transistors model the Tanner EDA tool (250 nm), the output is as shown in Figure 5. Where the "difference" part and the "borrow" part have a little noise/distortion. This can be rectified by changing the input parameters or adjusting the width of the transistors.

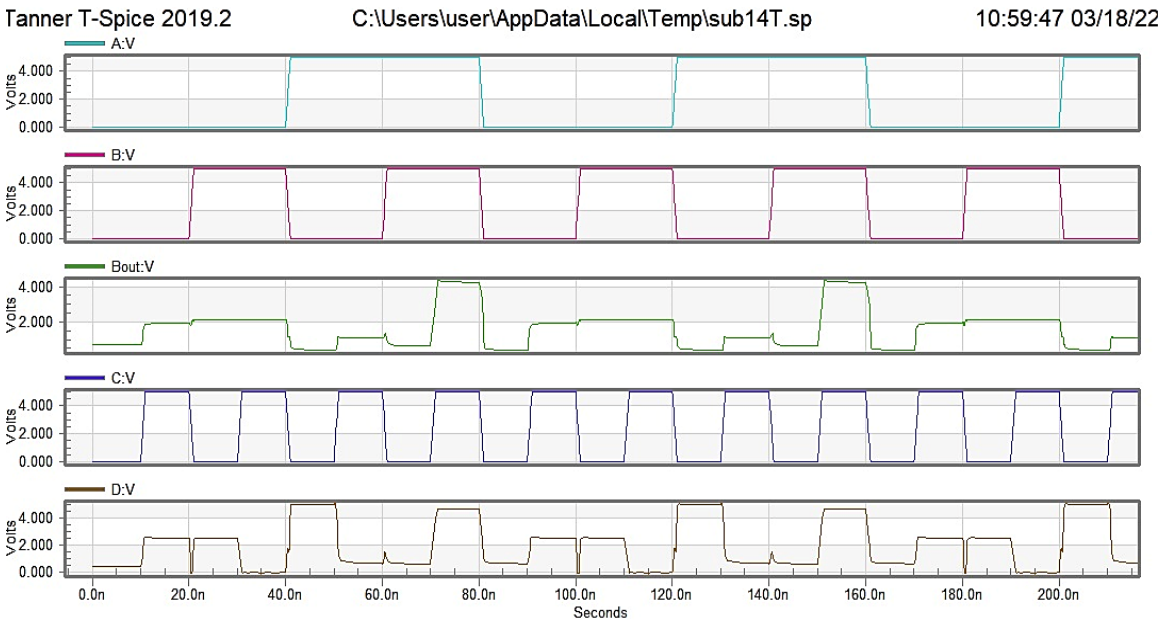

Figure 5. Output of 14 transistor model of full subtractor)

Proposed Design of Full Subtractor with 12 Transistor

Fig. 6 shows the proposed design of the full subtractor using 12 transistors. The circuit consists of 12 transistors (six NMOS and six PMOS transistors). No changes were made to the (D) difference section of the full subtractor compared to its existing counterpart. However, borrowing was deduced using the majority function [11]. The value of all capacitors was taken as 5 fF.

The output of the borrow section which is built around the majority function changes its state whenever its inputs are at majority '1' or majority '0. ' If more than two of the inputs are at logic '1,' then its output will also be at logic '1' or vice versa.

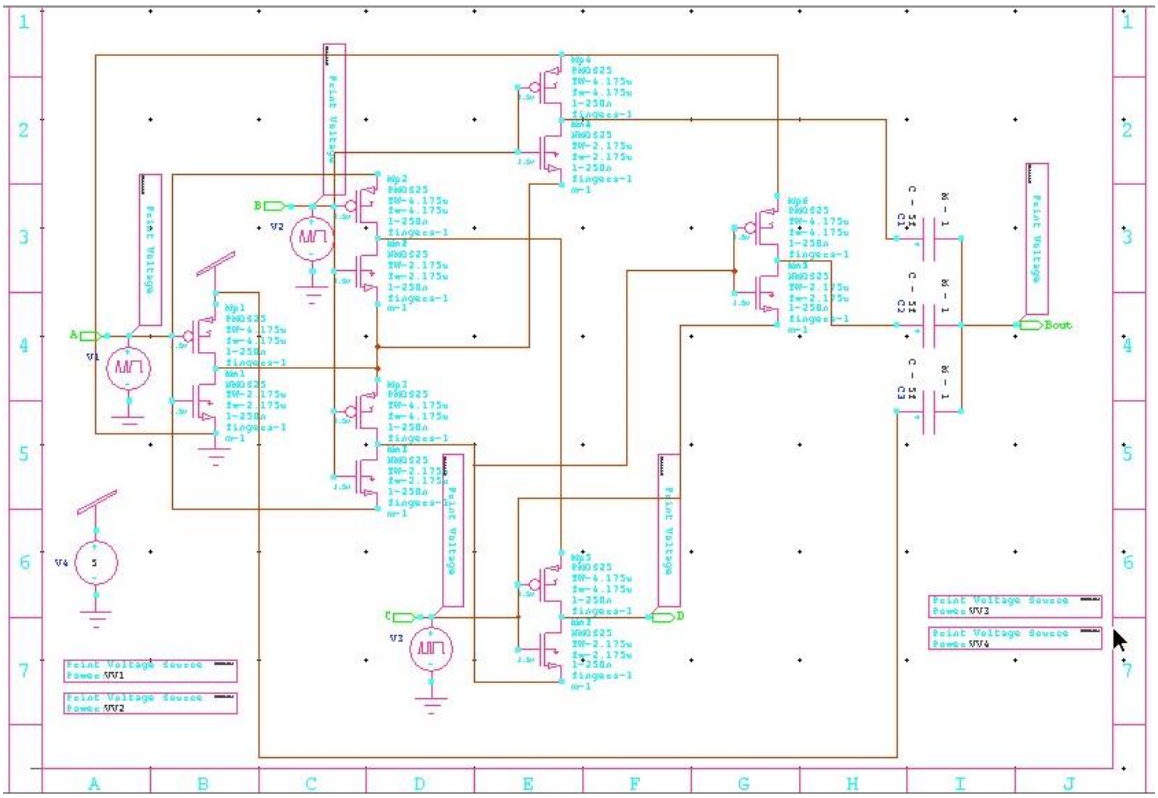

Figure 6. Proposed 12 Transistor models.

Output of Proposed 12 Transistor Design

Figure 7 shows the output of the proposed design of 12 transistors model. where A, B, and C are the inputs and D and Bout are the outputs. At the Bout and D sections (Figure 7), there is distortion or noise, which can be properly achieved by changing the values and parameters in the circuit.

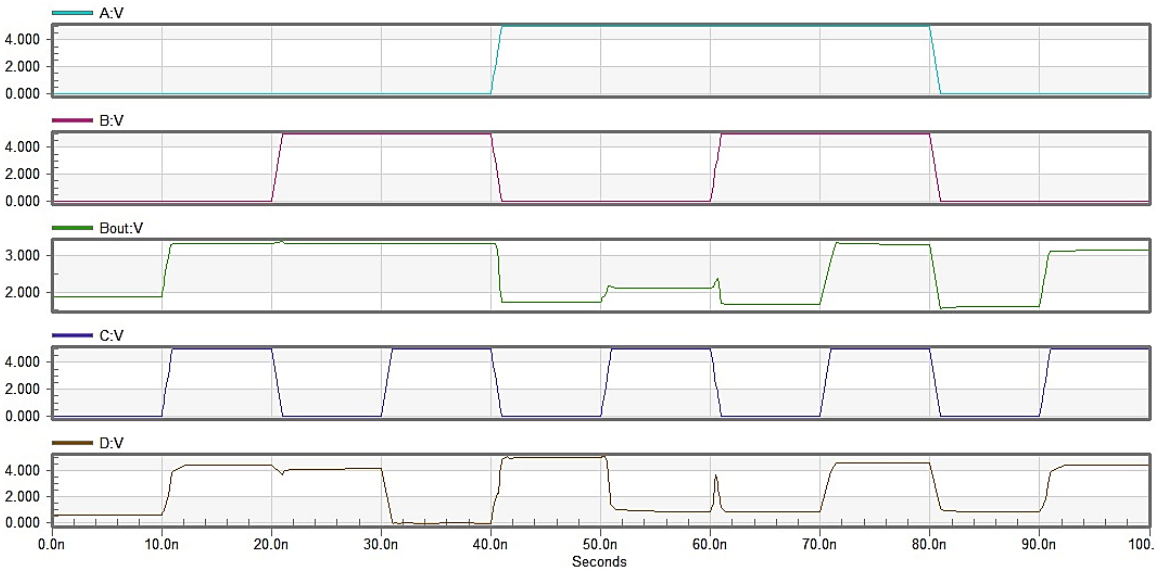

Figure 7. Output of proposed 12 transistors.

Comparison Among Different Circuits

In Table 1, a comparison of 20 transistors, 14 transistors, and the proposed 12 transistor design is presented. In every model, the length of all transistors was kept at 0.25um. The widths of the PMOS and NMOS were maintained at 4.175um and 2.175um, respectively. The capacitance of the capacitor was chosen to be 5fF.

In 250 nm technology, the average power consumed by the 20-transistor model is 227.49uw and the 14-transistor model has an average power consumption of 99.52uw. The proposed design of a majority function-based subtractor has an average power consumption of 98.84uw, which is slightly less than the 14-transistor model which can be further lessened by changing the parameters of the transistors (Table 1 and Figure 8).

Table 1. Comparison of 20T, 14T, 12T full subtractor.

20T Model of Full Subtractor	**14T Model of Full Subtractor**	**Proposed 12T Model of Full Subtractor**
*Transistors used =20	*Transistors used = 14	* Transistors used = 12
10 NMOS and 10 PMOS has been used	7 NMOS and 7 PMOS have been used	6 NMOS and 6 PMOS have been used
Length of NMOS and PMOS = 0.25u Width of NMOS=2.175u Width of PMOS =4.175u	Length of NMOS and PMOS = 0.25u Width of NMOS 2.175u Width of PMOS=4.175u	Length of NMOS and PMOS = 0.25u Width of NMOS 2.175u Width of PMOS =4.175u Capacitor = 5fF
Average power consumed is 227.49uw	Average power consumed is 99.52uw	Average power consumed is 98.84uw

Comparison Chart of Existing and Proposed Techniques

The proposed design of a majority function-based subtractor has an average power consumption as shown in Figure 8.

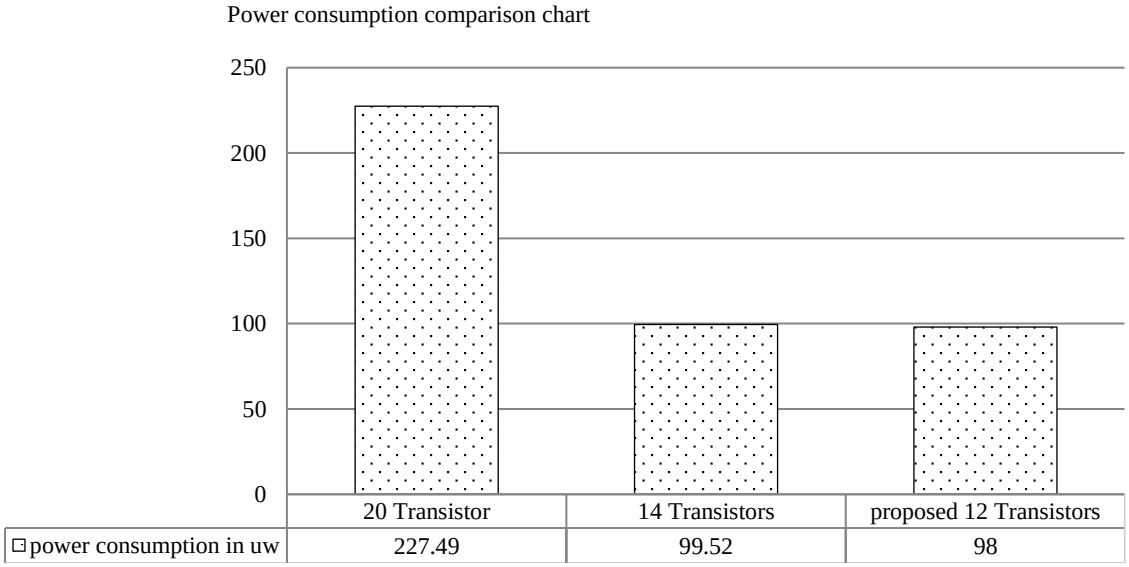

Figure 8. Comparison of different techniques.

CONCLUSION

Based on the output waveform and numerical analyses, implementing a full subtractor using 12 transistors can significantly reduce power consumption while maintaining functionality. This achievement marks a notable advancement in circuit design, reflecting ongoing efforts to optimize the

efficiency of digital logic implementations. However, it's important to note that despite these advantages, there may be instances where noise is present at the output. This noise is often attributed to a low voltage swing (VoL), a phenomenon in which the output voltage levels do not reach their full potential owing to various factors such as transistor sizing, biasing, or circuit layout. To mitigate the effects of low-voltage swing and thereby reduce noise at the output, it is crucial to adopt appropriate voltage swing techniques during the design phase. Techniques such as adjusting transistor sizes, optimizing biasing conditions, or employing level shifters can help ensure that the output signals achieve adequate voltage levels. These strategies not only enhance the signal integrity but also contribute to the overall circuit reliability and performance.

In summary, while the implementation of a full subtractor using 12 transistors represents a significant step forward in reducing power consumption, addressing issues related to low-voltage swing through appropriate design techniques remains essential for achieving optimal circuit performance in practical applications. By carefully balancing transistor configurations and implementing effective voltage-swing strategies, designers can further enhance the efficiency and robustness of digital circuits in diverse technological environments.

Future Work

The proposed 12 T design of the full subtractor has the desired output, but it suffers from a low-level output swing (VoL). Through further research, the noise can be reduced to zero by adopting appropriate output voltage swing techniques.

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