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Simulation of Adder Circuit Using Reversible Gates in Verilog HDL

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Abstract

The emerging field of quantum computing uses quantum logic gates. The reversibility of logic gates is an important aspect of quantum logic gates used in VLSI and quantum computing. Reversibility ensures that power consumption is minimized. This study explores the field of reversible logic and utilizes Peres gate to develop a full adder circuit that shows a significant reduction in power consumption in simulations performed in Xilinx Vivado. We have achieved a power consumption figure that is 97% lower along with a 15% reduction in junction temperature, as compared to conventional full adder. We have shown the methodology to create and obtain a reversible gate full adder circuit in Xilinx Vivado. Because they rely on irreversible computations, traditional logic gates cause bit erasure and consequent power loss. A developing field called reversible computing promises to solve this issue by guaranteeing that no data is lost during computation, therefore lowering power consumption. In this regard, modeling adder circuits using reversible gates is an important first step towards designing arithmetic circuits that consume less energy. This article uses Verilog Hardware Description Language (HDL), a popular tool for modeling and simulating digital circuits, to examine the design and simulation of a reversible adder circuit.

Keywords: Full adder, Verilog HDL, reversible logic, power optimization, Peres gate

INTRODUCTION

Power dissipation is one of the most important factors in large-scale integrated (VLSI) circuit design. Traditional and conventional gates, which have been widely adopted and used in almost every industry, have some drawbacks. While effective, classical gates are irreversible. Because of this irreversible nature, information is lost, resulting in heat dissipation. Part of the energy dissipation is due to the nonidentity of the switches. Although advancements in material science and fabrication processes have drastically reduced power loss, overall, energy dissipation still exists. According to Landauer's principle, for every bit operation lost in an irreversible process, kTLn (2) joules are dissipated [1], where k is the Boltzmann constant, and T is the temperature of the system. On a large scale, microchips containing millions of tiny transistors may lose significant energy, which may affect and alter the thermal performance of the board. In 1973, Bennett [2] showed that kTLn (2) energy would not be dissipated from a system, as long as the system allowed the reproduction of the inputs from the observed outputs, which did not result in information loss.

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The concept of reversibility has been developed as a solution to this problem. Generally, there are one or more inputs and only one output in an irreversible gate. However, the input cannot be reconstructed using these outputs. In low-power VLSI, reversible logic is implemented to overcome this drawback [3]. Information is not lost in reversible gates, and back-computation is possible

in reversible circuits with reduced power dissipation. In reversible circuits, one-to-one mapping between inputs and outputs exists. In a system, energy loss is directly proportional to the number of bits or information lost during the computation process. Reversible computation utilizes one-to-one mapping of inputs with respect to outputs and hence prevents bit loss. The minimum number of gates is used for operations while minimizing heat. The advantages of applying reversible logic to multipliers have been demonstrated in the literature [4]. Multipliers using the Toffoli gate, Peres gate, and Double Peres gate have been proposed to minimize the constant input, garbage output, and quantum cost [5]. Power-efficient reversible logic-based architectures have also been proposed for multipliers [6]. The physical interpretation of reversibility refers to the slow transmission of charges from one node to another instead of being dissipated. Thus, optimal energy efficiency is achieved. Logic gates based on reversibility are important in the field of quantum computing. In this study, we explore the means of reducing power consumption in a full adder (FA) circuit through a reversible gate. Kamanga et al. studied the use of FPGA and Verilog HDL to enhance these three variables. Owing to VLSI technology, FPGAs have smaller dimensions and better delay performance, and millions of logic gates are packed into small spaces. The study used Verilog HDL to further increase the delay performance by using brief instructions that skipped pointless iterations. This study compared same-sized RCA and CLA designs with an enhanced 64-bit CLA design. To model the design, an environment called Vivado HLX was used. A ZYNQ-7ZC702 board was employed in the FPGA simulation. The proposed design is contrasted with RCA and CLA. 13.1% less area, 5% less power usage, and 14.03% better system delay performance compared to CLA showed improvements [4].

Using reversible logic, Batish et al. provided a comparative analysis of a 1-bit full adder circuit to determine which circuit was the most efficient compared to the ones that were already in place in terms of dynamic power, leakage power, area, and delay [5].

An inexact Baugh-Wooley Wallace tree multiplier with a unique architecture for an inexact 4:2 compressor that was tuned for realization through reversible logic was proposed by Raveendran et al. 12.5% error rate (ER) and ±1 error distance (ED) is found in the suggested inexact 4:2 compressor [6].

A reversible digital full adder circuit, which is a crucial component in determining the Energy Delay Product (EDP) for numerous computer applications, was the subject of Pakkiraiah et al. study. Using the logic decomposition method and switching activity notion, a new reversible binary full adder was constructed [7]. By presenting a thorough overview of reversible gates, including their fundamental concepts, design approaches, and different applications, Naz et al. analyzed a number of reversible gates [8].

Peres Gate

The gate used for the reversible adder circuit is the Peres gate, whose block diagram is shown in Figure 1. It is a 3×3 gate with three inputs that match its three outputs. It has the lowest quantum cost of 4, which is generally preferred. It also produces an identity output that ensures that an extra bit is not lost. For inputs I (A, B, C) and outputs O (P, Q, R), the mapping is P=A, Q=A^B, and R=AB^C [7, 8].

It is asserted that the components of computing machines invariably carry out logical operations for which there is no single-valued inverse. This logical irreversibility is related to physical irreversibility and necessitates a minimum amount of heat generation, often on the order of the kTper machine cycle

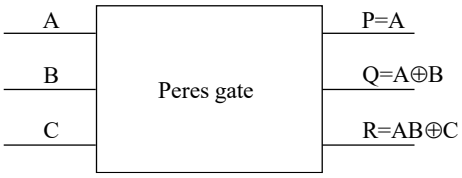

Figure 1. Block diagram of Peres gate.

for each irreversible function. To standardize signals and make them independent of their precise logical history, this dissipation is necessary. A more thorough examination of the switching kinetics of two straightforward but representative models of bistable devices is conducted to determine the relationship between speed and energy dissipation and to calculate the impact of mistakes caused by thermal fluctuations. A typical general-purpose computing automaton, such as a Turing machine, lacks a single-valued inverse in its transition function, making it logically irreversible.

PROPOSED METHODOLOGY

The process of obtaining the power and area consumption parameters of both full adder and reversible full adder circuits is performed through a simulation on Vivado. Verilog designs of full adders based on reversible gates, such as Feynman Gate and Fredkin Gate, are available in the literature [9, 10]. However, power consumption statistics are not provided for the Feynman and Fredkin gates. We present our work on the Verilog design of a full adder based on reversibility with Peres gate, along with power consumption statistics. The existence of thermodynamically reversible computers, which may carry out practical computations at practical speeds and dissipate significantly less energy than kT at every logical step, is made possible by this conclusion, which is of major physical interest. The logically reversible automaton resembles comparable irreversible automata in the initial step of computing, but it avoids the irreversible process of erasure by saving all intermediate outcomes [11].

For the basic full adder, we created a normal full adder design using the standard code. With this code, we opened the elaborate design and simulated Vivado. The implemented power report generated is presented by the project manager shown in Figure 2.

The implemented full adder design showcases that the total power consumption used is 0.972 W with a junction temperature of 29.9°C. Junction temperature, also known as transistor junction temperature, is the highest operating temperature of a semiconductor component in an electronic device. The total on-chip power refers to the power consumed internally within the device, which is equal to the sum of the static power and design power of the device. This is also known as thermal power. In summary, we can say that these two parameters represent our point of comparison.

For the reversible full adder, the process is slightly more complex and requires the design and input of the said design into Vivado through the block diagram to create features. We used a Peres Gate Full Adder Design (PGFA). The intended result was printed in the second step. After that, the third stage

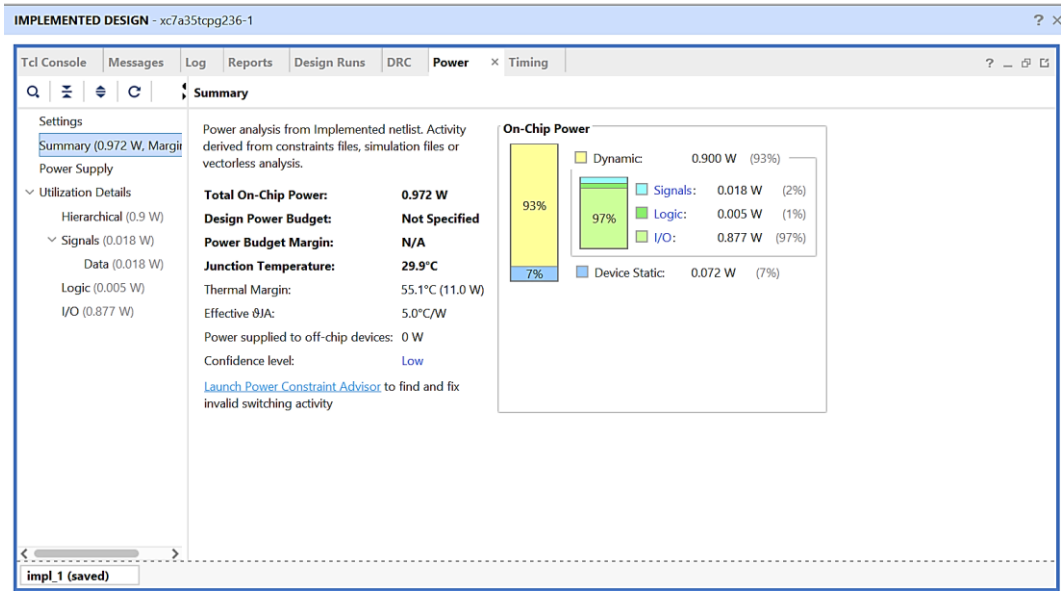

Figure 2. Power consumption report generated by the simulator.

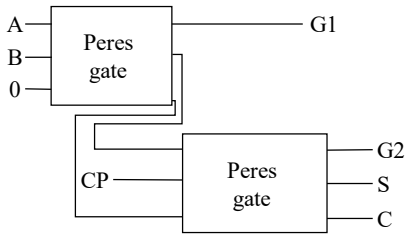

Figure 3. Peres gate full adder design.

reversibly eliminates all the undesirable intermediate results by going backward through the first stage's steps (a procedure made possible only by the first stage's reversibility), returning the machine, aside from the now-written output tape to its initial state. Thus, the final machine configuration contains no additional unwanted data other than the desired output and a reconstructed copy of the input. An explicit example of the above results is provided using a particular type of three-tape Turing computer. One physical example of reversible computation is the production of messenger RNA.

The PGFA shown in Figure 3 utilizes two Peres gates with two identity outputs G1 and G2, which will not be used. The third input into the first PGFA was maintained low throughout. The method to create and utilize this gate in Vivado is to create two Peres gates with 3 × 3 mapping and subsequently take the A^B and the AB^C output of the first Peres gate as the input of the second Peres gate along with the Carry-in. The Verilog HDL code for Peres gates is as follows:

```
module PeresGate1(input A, input B, input C, output G1, output D, output E);
assign G1 = A;
assign D = A ^ B;
assign E = A&B;
endmodule

module PeresGate2(input F, input Cin, input G, output Sum, output Cout, output G2);
assign Sum = F^Cin;
assign Cout = (F&Cin)^G;
assign G2 = F;
endmodule
```

The required outputs of the full adder are from Sum and Cout and should be cautious to ensure that the output from Peres Gate1 to Peres Gate2 is correctly mapped.

The next step is to create a block design for the FPGA using this tool. Once a blank block design space is opened, using the input tool, two Peres gates are inserted from the design sources. The gates were connected in the required manner. Constant input sources are inserted, and the input values are maintained to obtain the FA outputs. We proceeded with inputs A and B of the first Peres gate as high and C as low, and for the second Peres gate, C_{in} was kept high. This ensured that all the constant widths were within the range. Further, the simulation is run, power is obtained, and thermal consumption statistics are obtained inside the project manager.

The graph in Figure 4 and the test bench results show that the results/truth table of the reversible full adder matches that of the conventional full adder.

A schematic generated by the proposed process is shown in Figure 5. We have given Cin as always high for the sake of convenience; however, the result generated, that is, the truth table, remains the same regardless of whether we continuously change the value of the truth table. We verified the sum and output values of the circuit for all input values, which are in line with the truth table of a full adder. The power consumption characteristics of the PGFA are shown in Figure 6.

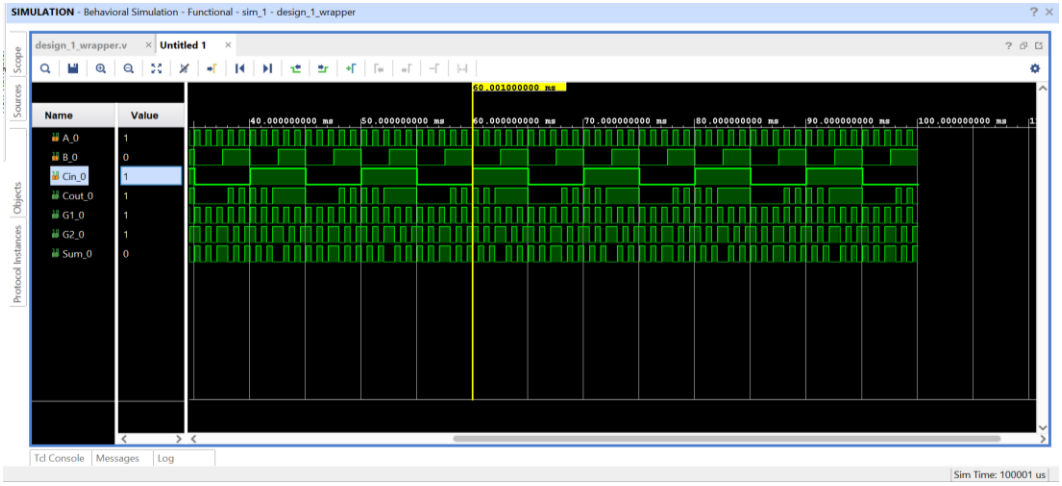

Figure 4. Simulation results of reversible full adder.

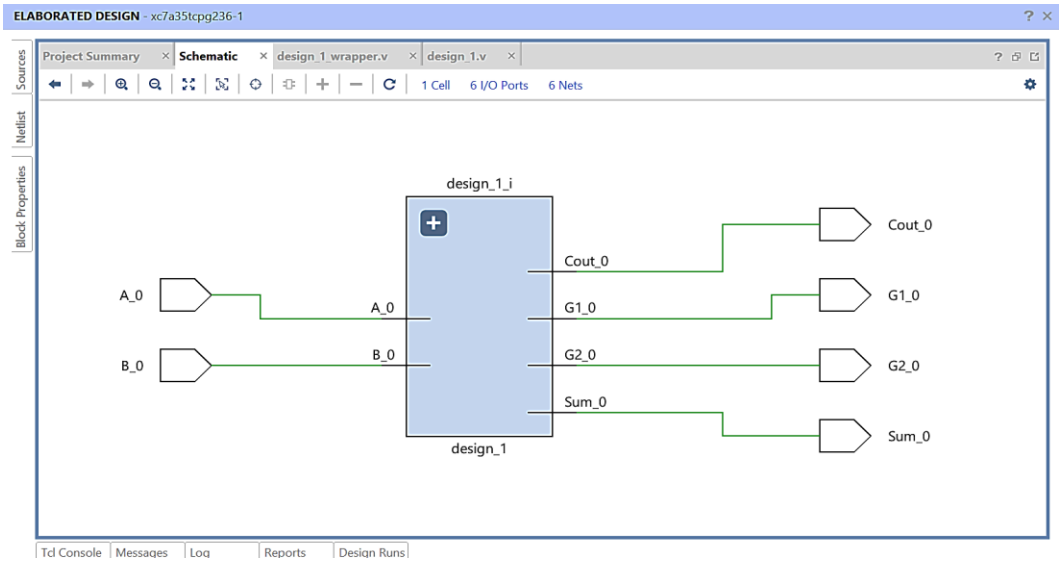

Figure 5. Schematic of the entire circuit.

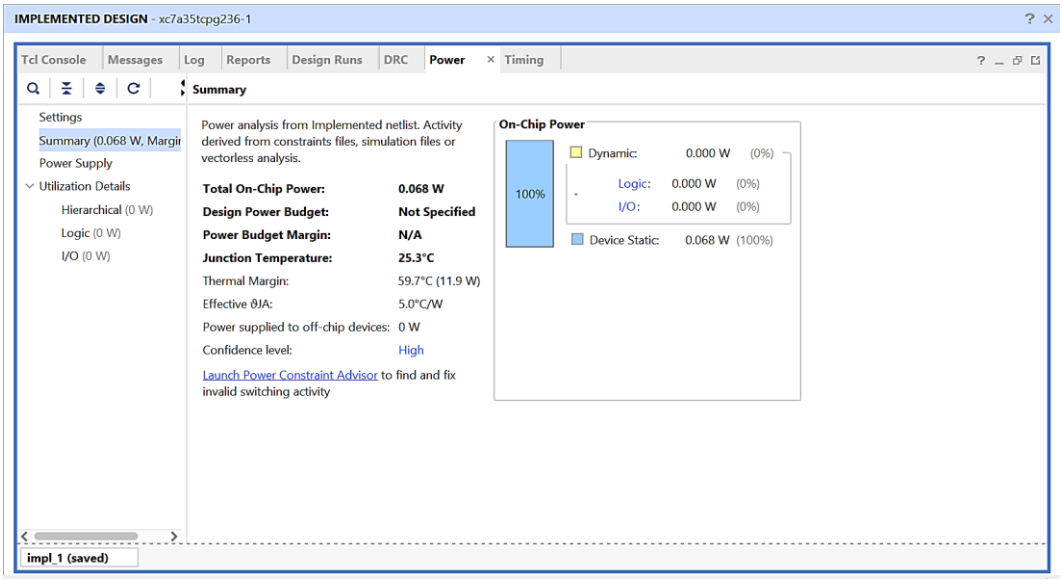

Figure 6. The generated power report on Vivado.

RESULTS

From the simulation, we obtained the total on-chip power consumption to be significantly less than that of a conventional full adder at 0.068 W. The junction temperature was also lower at 25.3°C. These values were 97% and 15% lower than those of a conventional FA, respectively. This extreme reduction in value can be attributed to the fact that reversible circuits do not lose information bytes, and for small-bit values, the difference between the energy consumed is greater than that for a higher number of bytes.

In the above simulations, a brief overview of the power consumption characteristics of a PGFA was presented. The design of an existing PGFA was implemented in Xilinx Vivado through the mapping of gates as per the convention. Proper steps and precautions were taken to ensure that the simulated results shown were valid, and a drastic decrease in power consumption was observed. The PGFA showed the proper truth table of a conventional adder when given inputs changing at different frequencies, as given in Table 1.

Table 1. Full adder results received from PGFA.

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	0	0	1
1	1	0	0	1
1	1	1	1	1

Scope of Exploration

The future scope of this study lies in the design of circuits based on this simulation and the investigation of power consumption. It is crucial to know whether a circuit can be implemented in real life.

CONCLUSION

We conclude that using reversible logic results in a drastic decrease in the power consumption of a full adder circuit. The 97% power reduction can in part be explained by the fact that reversible logic does not require the device to be in the dynamic power consumption mode, as shown in the implemented power report. The entire operation of the circuit is performed in static mode.

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