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Design and Simulation of Low Power Alowarea High Speed Carry Save Adderusing CMOS 16 nm Technology

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Abstract

In this Article we propose a novel 1-bit hybrid full adder circuit is implemented using eighteen transistors. Simulations are done using the Mentor Graphics Tool 16nm technologies. The performances are evaluated based on its speed, average power consumption, and power-delay product. The essential components of arithmetic units including compressors, comparators, parity checkers, etc. are full adders. Thus, raising the performance of the entire adder will raise the performance of the system. An improved design can lower power consumption, delay, and maintain good performance in the full adder circuit even at low supply voltages. Furthermore, it's critical to give complete adders enough driving power even under varying loading circumstances, prevent errors, and generate balanced outputs. The proposed hybrid full adder has low power and energy consumption as compared to other full adder designs. Finally, a four operand, eight-bit carry-save adder the final carry propagate adder was implemented using the proposed full adder, and its performance is analyzed based on its average power consumption in 16nm technology. This design also Wave rage power consumption compared to CSA implementation using other existing full adder design styles.

Keywords: Full adder, CSA, compressors, comparators, parity checkers

I. INTRODUCTION

In this technological era, there is a rapid growth in the usage of battery-operated portable devices such as mobile phones, smart watches, Bluetooth speakers, and laptop computers. So, the demand for VLSI designs with improved power delay characteristics is increasing day by day. Full adders are the fundamental building blocks of arithmetic units such as compressors, comparators, parity checkers, etc. Therefore, improving the full adder's performance will enhance the overall system's performance. In the full adder circuit, optimized design can reduce power consumption, delay, and provide good performance even at low supply voltages. Moreover, it is essential to provide adequate driving capability in full adders even at different loading conditions and avoid glitches produce balanced outputs. A wide range of papers has been published based on the full adder's design. Even though all circuits perform the same function, their internal logic structures are different, leading to a change in propagation delays and power consumption. Full adder cells can be broadly classified into three categories based on theological equations for output and their module-level structures.

1. Hybrid-CMOS full adder even though this circuit provides better driving capability and full swing output but suffers from higher power consumption [2].

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2. DPL logic style was designed to obtain a better power delay product. Still, it has high power consumption and requires many transistors(28T)
3. Kumar's Full adder design, the main drawback of this design is the propagation delay of carry is more due to the sharing of carry input with other modules.

LITERATURE SURVEY

Design of Robust Energy-efficient Full Adders for Deep-sub–Micrometer Design Using Hybrid-CMOS Logic Style

The adder circuit consists of three individual components. The fundamental elements of this architecture are the XOR and XNOR gates. Sum is generated by expressing the Sum and Carry. We present a new design fora1-b full adder featuring hybrid-CMOS design style. Our exploration of a hybrid CMOS architecture was motivated by the need for low-power, high-noise devices at deep sub-micrometer dimensions. By fusing together several CMOS logic type circuits, a new generation of complete adders with the necessary performance may be designed and manufactured utilizing the hybrid-CMOS design approach. As a result, the designer has greater freedom to come up with novel solutions and create products with many uses. In addition to this operational categorization, we separate hybrid-CMOS full adders into three structural categories. Using this categorization, many full-adder designs can be conceived. It will be shown that a novel, all-encompassing adder architecture may be placed in one of the suggested taxonomies. The one-of-a-kind full adder is powered by a novel XOR-XNOR circuit that produces XOR in parallel. The average PDP for this circuit is 5-37% greater. We provide an alternate XOR/XNOR output stage constructed using standard CMOS components. The high driving power of this stage makes it well suited for implementation in buffer-free cascade adders. PDP requirements are now 40% lower than before. We found that several of the adders we had previously tested had weak swing and substantial noise when operating from low supply voltages. The suggested full adder uses less energy than previous full adders while maintaining the same level of performance and reliability. Because of its high driving power and outstanding signal integrity, the innovative full-adder circuit can function well at low voltages. To evaluate the performance of the new full adder in a real circuit, we embedded it in a 4-and8-b,4-operand carry-save array adder with final carry-propagate adder. The novel adder was just as effective as the more traditional full adders. To meet the rising demand for portable electronics, manufacturers have enhanced silicon area, processing speed, battery life, and durability. Every decision must be made with the goal of minimizing energy use in mind. Full adders are used in a wide variety of circuits, including compressors, comparators, parity checks, and full adders.

The power consumption of a typical current high-performance central processing unit. The data path is responsible for around 30% of the overall energy used by the system. You should learn everything you can about adders before you really need them. The usage of adders is commonplace in data channels. Maintaining dependability at low supply voltage is essential for circuits designed for deep sub micrometer technology, as it minimizes loss of output voltage, power consumption, and key route delay. It is equally important that the system works reliably and consistently. Due to their prevalence in large replication, studies examining the stability of adder cells and the intricacy of their connections are strongly needed. Many different methods of reasoning have been used to construct whole adder cells. Each method of layout has its advantages and disadvantages. Every step follows the same logic as a standard full adder. One example of such a design is the standard static CMOS full adder [10].

The conventional CMOS structure on which these transistors are based ensures full-swing output and robust driving capabilities. Static CMOS circuits' biggest issue is PMOS blocks, which are much slower than NMOS devices [8]. To provide the desired performance, bigger PMOS parts are necessary. In a static CMOS gate, the capacitance at the inputs is rather large since each input links to the gates of both a PMOS and an NMOS device. As a result, the processing speed of static CMOS gates is somewhat slow. To do computations, pass-transistor logic (CPL) is now favored over complement.

High-speed, reliable driving is made possible by a differential stage built from cross-coupled PMOS transistors and output static inverters. Even when using several static inverters and internal nodes, considerable power loss remains. The layout of a CPL cell is also not as straight forward as a static CMOS cell due to its irregular transistor arrangement. Fast computations are made possible using high-mobility NMOS transistors in the construction of dynamic CMOS logic. Since PMOS transistors are not used, the input capacitance is smaller, which results in faster processing times. Workload increases and reorganization of responsibilities point to underlying problems. The use of switches has become more common, and noise reduction techniques have improved. Consistent effort is required to keep time accurately. Leakage is made more likely when dynamic logic is used in an implementation. Because of these limitations, we are unable to further explore the dynamic logic approach.

EXISTING METHOD

The schematic of Hybrid full adder simulation in Figure 1. A wide range of papers has been published based on the full adder's design. All functionally equivalent circuits have various underlying logic architectures, which results in differing propagation delays and power consumption. The output logic equations and the module-level architectures of full adder cells allow for a rough categorization into three main types.

This circuit has superior driving capabilities and full-swing output than the hybrid-CMOS full adder [1], but it consumes more power. To improve the power delay product, the DPL logic style was developed. However, it uses a lot of energy and needs a lot of transistors (28T). Sharing the carry input with multiple modules slows down carry propagation, which is a major drawback of Kumar's Full Ladder design [3].

There are a total of three modules making up the adder circuit. The initial part of this system is an XOR/XNOR gate combination. Module III produces both Sum and Cout. The results of Sum and Carry may be expressed in two different ways: (1) and (2) Module 1, seen in Figure 1, is an XOR-XNOR cell that generates the H and H signals that power Modules 2 and 3. Three transistors provide an XOR output H, which not only produces the H and H signals but also switches ON the Mpf in the feedback loop. If A=B=1, the modified XOR output H displays weak logic 1 (VDDVTN), yet it may turn ON the Mnf and Nf. Passes logic0 to output H; as a result, Mpf is turned ON and obtain perfect logic1at the H output. As a result, the necessary voltage levels will be attained at the outputs for any combination of inputs for activating the other two modules. The XOR gate is the second module in the whole ladder. It produces the Sum output from in termediate signal Hand input Cin where Sum=Cin⊕H. The Gate Diffusion Input design method [5] was used to create Module 2. For every given input configuration, the Gate Diffusion Input (GDI) may provide full swing output. XOR with the GDI circuit needs an inverter to create a complement signal to either of the two inputs, however this circuit may be used as the second module in the proposed full ladder with only four transistors.

Two 2-to-1 Multiplexer circuits are linked together to form the third module of a hybrid full adder [6]. Only four pass transistors are required for the two main inputs (A and Cin), the select line (H), and the output (Cout). One PMOS and one NMOS conduct in all input states, allowing for a full-swing output. When H and an equal 0 Mp1 and Mn2, these transistors provide a perfect logic 0. If the total number of hands is 1, then logic 1 is sent via the two MOSFETs labeled (Mp2) and (Mn1). Cout. The output of this circuit is a carry signal, denoted by Cout. The first cell is an XORXNOR circuit. The H and H signals it produces then provide energy to the system's other two components. All the arithmetic, the second and third modules each employ just four transistors to prevent a drop in output voltage threshold.

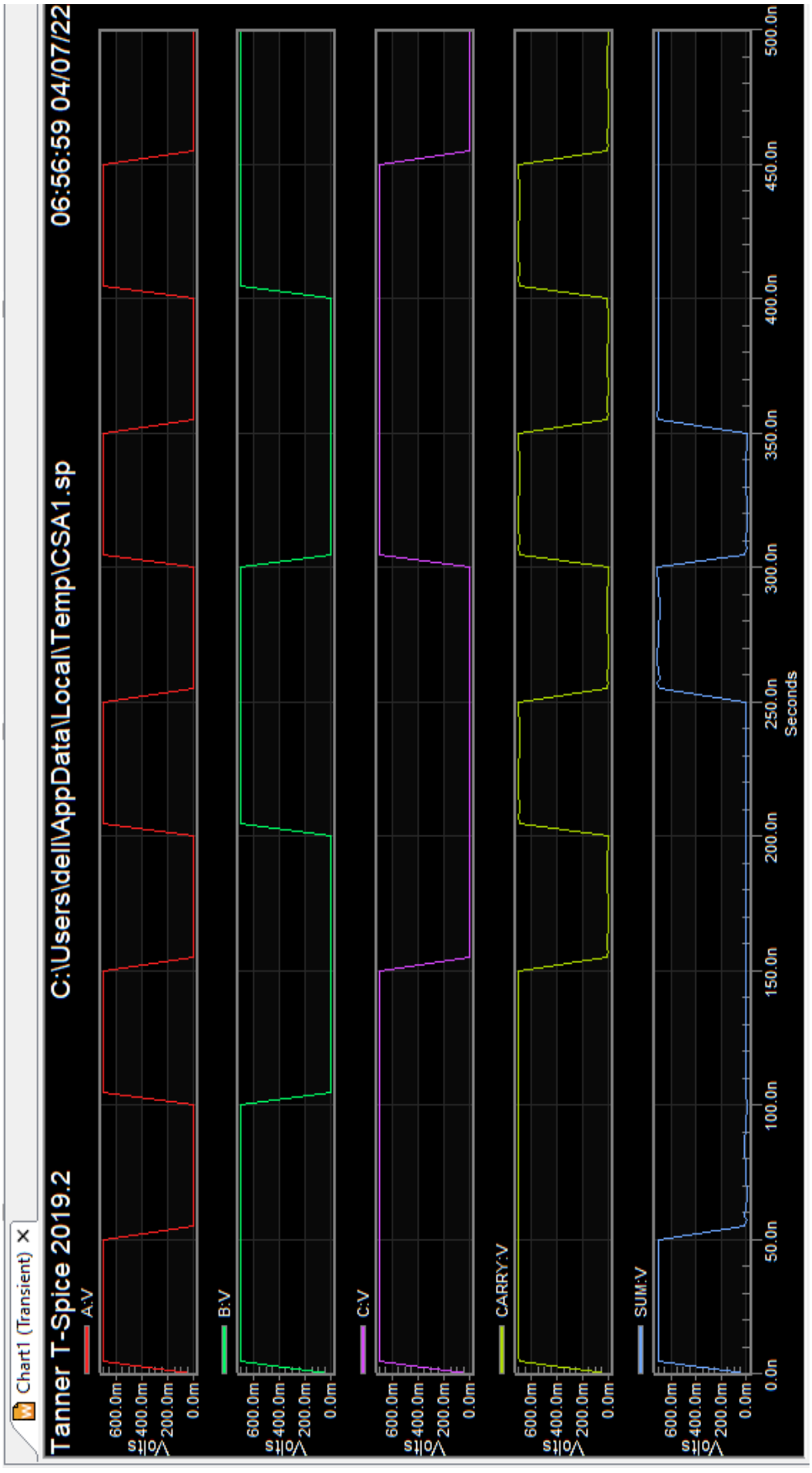

Figure 1. Simulation results of hybrid full adder.

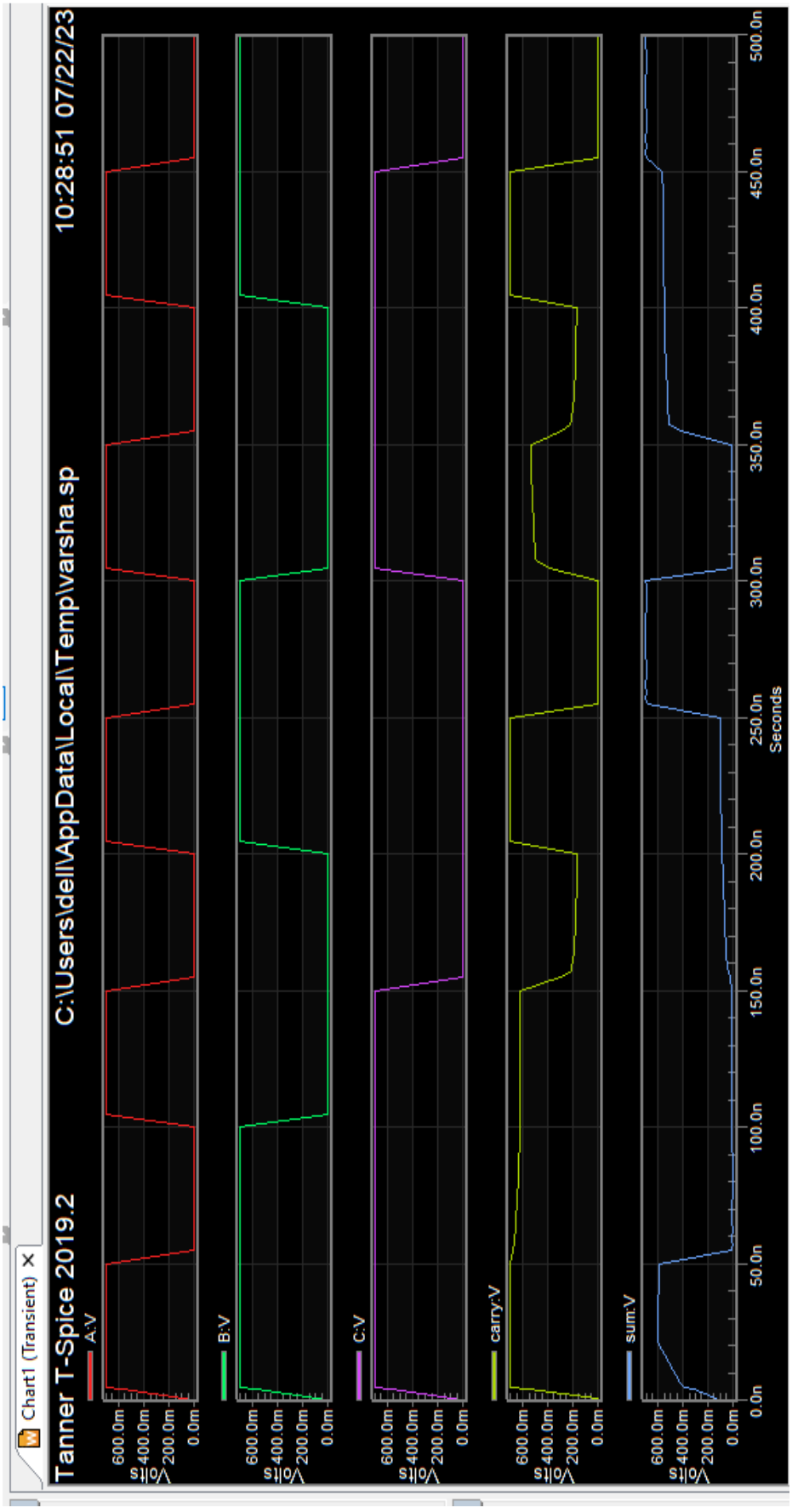

Figure 2. Simualtion of proposed schematic of hybrid full adder.

Simualtion of proposed schematic of hybrid full adder is the result of modifying three transistors in an XOR gate and an XNOR gate [4], with an inverter linked to input B.A feedback loop is linked into both the modified Hand and Hand outputs since it cannot provide sufficient voltage levels at those points. This means that the other two modules may be powered by the XOR and XNOR outputs generated by the given circuit. Mpf and Mnf are PMOS and NMOS transistors, respectively. If inputs A=B=0, weak logic 0 levels (VTP)produce at the modified the hybrid full adder simulations were carried out in both the technology nodes, as shown in Figure 3, then compared its performance in both nm technologies Both a 180 nm and a 90 nm simulation with a 1.8 V supply voltage and a 1.2 V simulation with a 1.2 V supply voltage were performed. In a complete adder, a glitch appears in the final output if the signals arrive at the gate at various times. The average power used, latency, and power-delay product of the complete adder for both nm technologies.

PROPOSED METHOD

Proposed Full Adder With 14 Transistors

The above schematic contains 14 Transistors that are used to design single bit full adder. The above schematic has been designed with Mentor Tanner 16 nm Technology. The above Full adder can be used in designing of CSA adder.

In the above schematic 7 PMOS and 7 NMOS transistors are there. In the schematic 5 transistors are used to design XOR characteristics, and 5 transistors produce XNOR characteristics. And TWO transistors, one PMOS and One NMOS are connected in Pass transistors behaviors to produce Sum. And TWO transistors, one PMOS and One NMOS are connected in Pass transistors behaviors to produced carry.

The proposed 14 Transistor Full adder based on Pass Transistor has Average power consumption 14.86 micro watt, Static power consumption is 1.06 micro-Watt, Dynamic Power consumption 87 Pico Watts

A 4-operand, 8-bit carry-save adder with maximum carry propagation may be constructed using the given 1-bitfull adder cell [9]. The four operands in each column are the alphabetic letters A, B, C, and D. Each operand consists of eight bits (A0-A7), and the 1-bit hybrid full-ladder is employed to realize the blocks' functionality [7]. The first block in a column receives the inputs (A0, B0, and C0) and produces full adder output; the resulting Sum is then sent into the second block in the same column. The first block's left-side carry-out becomes the following block's carry-in. The inputs (D0), the carry from the previous phase, and the output Sum from the first block are used by the second block to compute the corresponding Sum (S0). The leftmost column gets the burden of carrying it. Carry is propagated to get to carry C, as shown in Figure 3 result for average power consumption.

```
VV1 from time 0 to 5e-07
Average power consumed -> 1.48644le-07 watts
Max power 1.092574e-06 at time 3.55e-07
Min power 8.715653e-11 at time 2.90778e-08


Measure information will be written to file "C:\Users\dell\App

Measurement result summary
   tdealy          = 605.6800p
```

Figure 3. Result for average power consumption analysis.

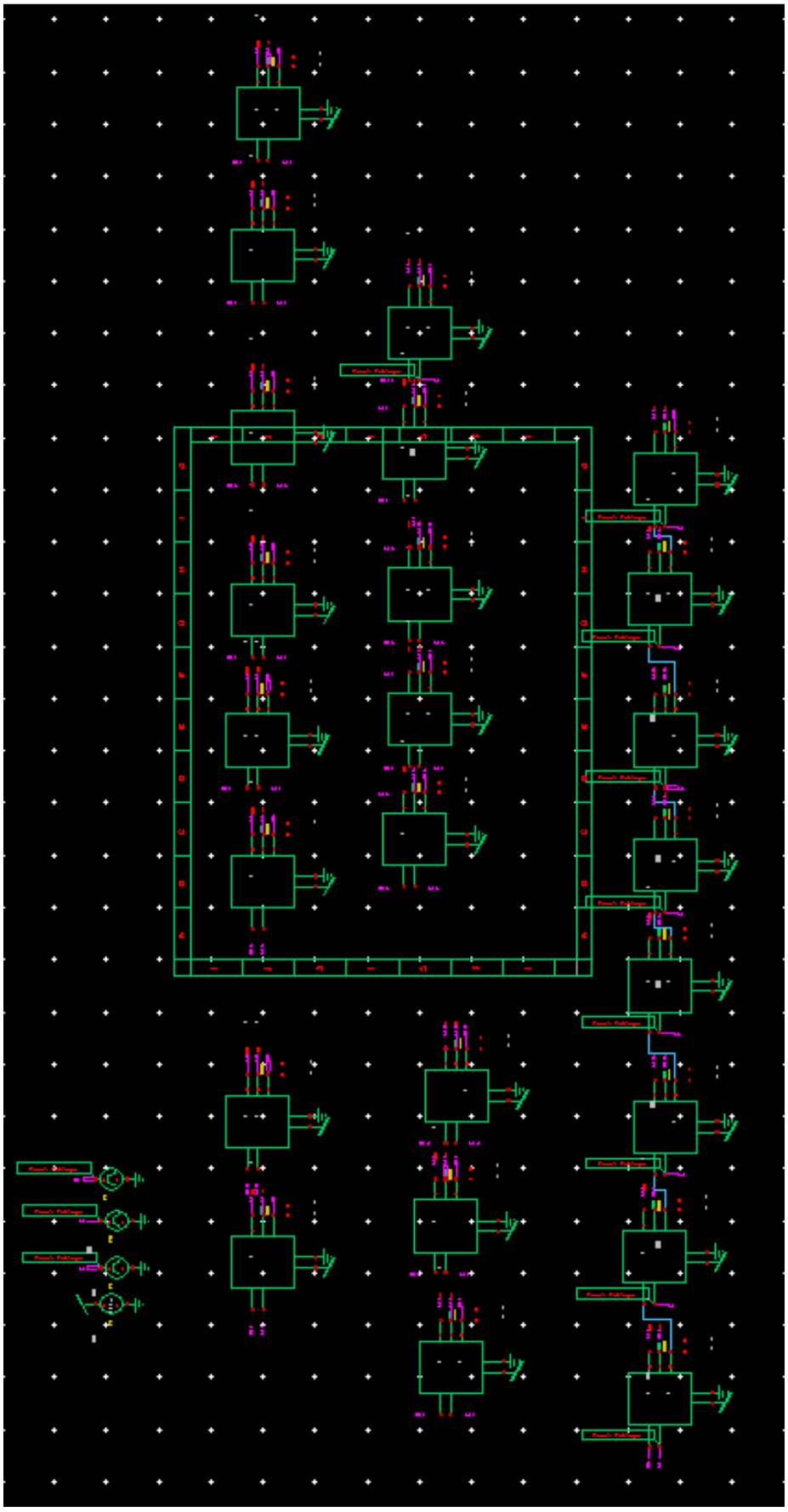

Figure 4. Schematic of 8-bit CSA.

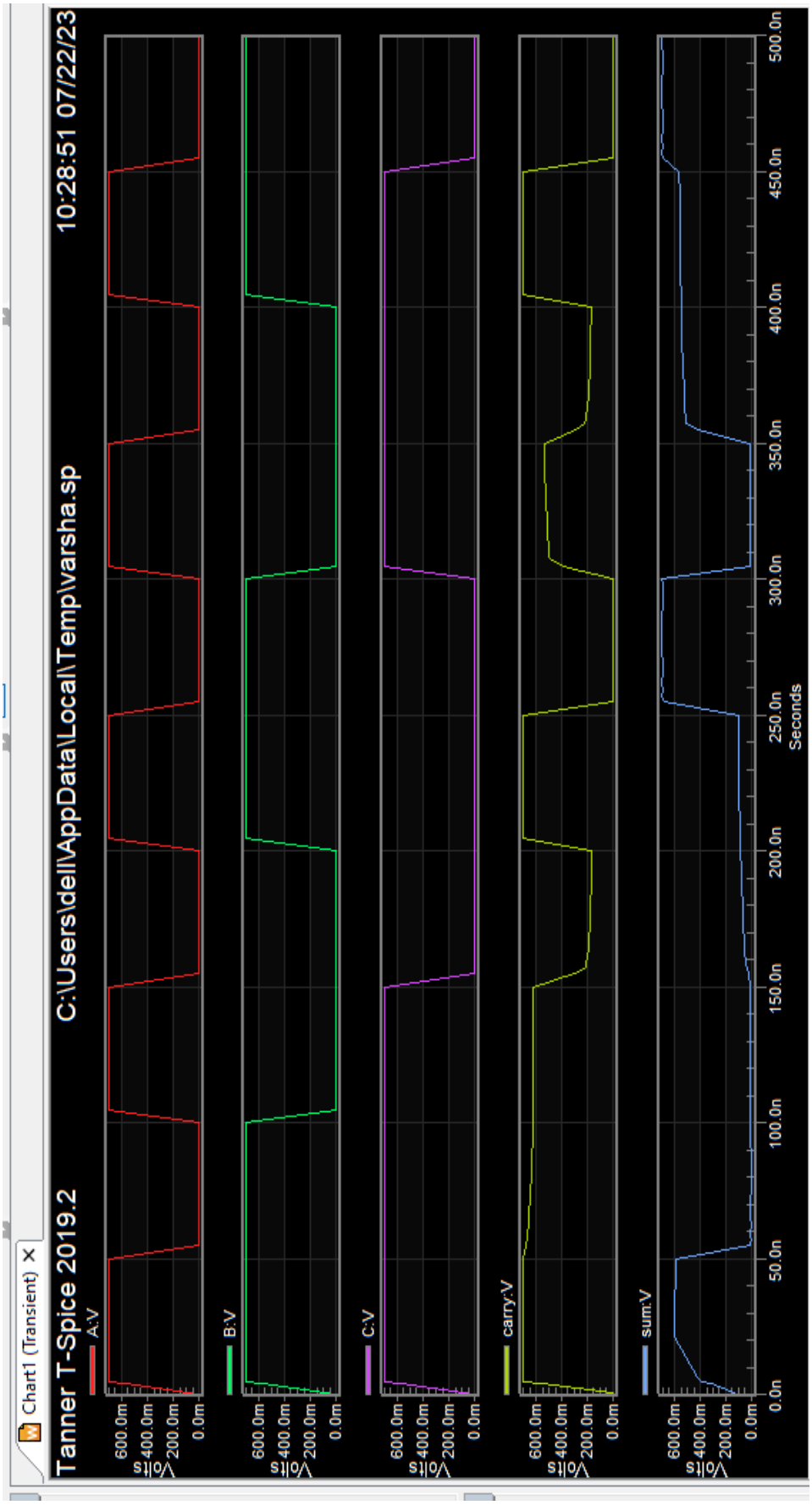

Figure 5. Simulation of 8-bit CSA.

The block-level simulation of the CSA is shown in Figure 6. Eight-bit, four-operand CSA performance was measured using 16nm technology. Table 1 compares the power usage of the old CSAs with the new ones that have been introduced. Since the 1-bit full adder carry structure consists only of pass transistors to provide output, increasing the number of stages likewise increases the latency. The addition of suitable buffers between the steps solves this issue.

Table 1. Simulation results comparison.

CSA Design Using:	Power(µW)	Delay(ns)	References
Hybrid-CMOSFA	158.4	150.33	[1]
Proposed FA	55.24	4.63	Present

```
Power Results

VV1 from time 0 to 1e-06
Average power consumed -> 5.552498e-05 watts
Max power 7.118233e-05 at time 9.03953e-07
Min power 5.227599e-05 at time 4.04227e-07
```

Figure 6. Simulation result for power analysis.

CONCLUSION

In this Article, we introduce a unique hybrid FA architecture that significantly outperforms prior art systems. Twenty preexisting FAs' characteristics were analyzed and compared to those of the novel FA. Mentor Graphics' simulation tools were used to measure the system's efficiency. The simulation findings show that the suggested FA increases both speed and PDP when applied to a single cell. Words up to 64 bits in length have been processed to verify the FAs' scalability. The only architectures that can directly run at 64 bits are the proposed FA and five current systems. The suggested architecture beats alternatives in the cascade mode, which is important since longer word-length adders are the current trend in contemporary computer systems, which need fast, efficient processing while using less power.

Future Scope

The XOR and XOR-XNOR gates that we proposed were used in six more FA cells that were given. Furthermore, a novel method for calculating the optimum size of transistors in digital circuits was created. Numerical computation's PSO algorithm is used in the new method to find the best transistor size rapidly and accurately for a circuit. The simulation results for FA cells demonstrated the effectiveness of the proposed.

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