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Implementation of Adders Using Ternary Based Multiple Valued Logic

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Abstract

In today's world VLSI chips are widely used in various branches of Engineering like Voice and Data communication networks, Digital signal processing, Computers, Commercial Electronics, Automobiles, Medicine and many more. So, there have been major advances in IC technology which have both made feasible and generated great interest in electronic circuits which employ more than two discrete levels of signals such circuits called Multiple valued logic circuits, offer several potential opportunities for the improvement of present VLSI circuit designs. Multi value logic can carry more information on single line. The key benefits of MVL are Increased data density, delay, reduced dynamic power dissipation and chip area. The major area of binary logic ICs are occupied by interconnections. The more effective utilization of interconnections is possible which uses a larger set of signals over the small area in MVL devices. The higher radix in use is the ternary (radix - 3) and Quaternary (radix - 4). In this paper our objective is to implement different high speed low power adders like RCA and CLA by using ternary based multiple valued logic. The functional verification is performed by using Xilinx ISE design suite by considering Verilog HDL.

Keywords: Ternary, MVL, CSKA, CSLA, RCA, HDL

INTRODUCTION

With less chip area needed, more complicated digital applications can be implemented in large part because of multiple valued logic. When compared to binary logic systems, multiple-valued logic systems provide significant energy usage improvements. Due to the numerous connections, the binary circuit is limited, necessitating a complex chip area and significantly more energy. Comparatively, a multi-valued logic (MVL) system uses more than two values of logic to reduce the number of connections, chip size, and energy usage by up to 70%. Ternary logic systems [1] can be expressed in two different ways: ordinary (unbalanced) ternary logic (0, 1, 2) corresponds to (0, Vdd/2, Vdd), and balanced ternary logic (1, 0, 1). For the past decade, MVL has attracted researchers' attention over binary logic. MVL can be implemented in software (algorithm) and circuit design such as logic gates, combinational circuits, memory circuits, programmable logic arrays (PLAs), MV-Quantum Logic, and wireless sensor networks.

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The base or radix of the ternary numeral system is 3 [2]. The number of distinct digits or distinctive symbols that can be conveyed using a single digit is known as a radix. In a binary system, a value is represented by the two logic symbols 0 and 1, whereas in a ternary system, a value is represented by the three logic symbols (0, 1 and 2). One of the ternary logic system's approaches is the bipolar notation, which is represented by the symbols -1, 0, and 1. The notation used in this essay is 0, 1, and 2.

Three-valued switching is explained by the ternary logic system. Comparing the ternary logic system, which has three values, to the binary logic system when building digital circuits, there are several advantages. It is possible to reduce chip space, but more crucially, it is possible to use error detection and repair codes that are simple to use. Examples include the ability to transfer more data on a set of lines of a certain length, the observation of a decline in the complexity of interconnections, the reduction of chip size, and, most significantly, the ability to detect and repair coding errors. Over the binary logic system, the ternary logic system has some important advantages [3, 4]. The chip space has been lowered because of the decrease in the number of connections in a circuit used to implement the various logic operations. More crucially, more data can now be sent while using less memory. In addition, the serial, and some serial- parallel processes are performed at very fast speeds. It has been used in sectors like digital signal processing and communications.

The most crucial performance evaluation metrics, latency, power consumption, and area characteristics, are all directly impacted by logic design. In addition to the conventional definition, there are two others. Logic value "1" is replaced by "0" ("2") in the first (second) interpretation of negative (positive) ternary, which is indicated by (+). As a result, they are binary functions. First, complementary positive and negative outputs (and) are produced. Binary inverters then transform into Out and Out+, respectively. Finally, two transistors divide the voltage to produce STOut (1). Voltage division therefore only occurs once a ternary function is implemented. When more than two states are required to encode information, ternary logic can be especially helpful. It might stand in for three-level signals in communication systems, three-state drivers in digital circuits, or multi-valued data in some computational models, for example. To handle the many permutations of ternary inputs and produce accurate ternary outputs while taking carry propagation and borrow propagation into consideration, ternary logic adders must be designed using a variety of ways. All things considered, research and development into ternary logic adders can be interesting and fruitful, especially as computer technology develops and new applications are made that might profit from the increased efficiency and information density that ternary logic offers [15]. Ternary (base 3) inputs and outputs are used in these operations by ternary logic adders, as their name implies. Given that they may handle more data per signal transition, ternary logic adders may occasionally be more effective than their binary counterparts in particular applications. Implementing ternary logic, however, poses considerable difficulties because more states call for more hardware and intricate designs. Using balanced ternary notation is one typical method of ternary value representation. In this example, -1 is used in place of 2, and the set of legal numbers is -1, 0, and 1. For instance, the decimal equivalent of the value +121 in a balanced ternary would be 1*(32) + 2*(31) + 1*(30) = 13. To handle the many permutations of ternary inputs and produce accurate ternary outputs while taking carry propagation and borrow propagation into consideration, ternary logic adders must be designed using a variety of ways. All things considered, ternary logic adders can be an exciting and promising field of research and development, particularly as computer technologies advance and new applications are created that might benefit from the greater efficiency and information density provided by ternary logic [12].

Contribution of Work

The Half Adder, which has sum and carry as its two outputs, is the most fundamental adder. Full Adder is a term used to describe a device that can add up to three bits as input and output two values, Sum and Carry. However, these adders can do calculations for a single set of bits at once. By utilizing full adders in parallel blocks, the multi-bit addition is carried out. When calculation is carried out in parallel, each bit's sum is computed simultaneously, the carry is passed along as an input to the following block, and the final carry output is determined from the previous adder block. Numerous adders, including the ripple carry adder (RCA), carry look ahead adder (CLA), carry increment adder (CIA), carry skip adder (CSKA) [7], carry save adder (CSA), and carry select adder (CSLA), have been developed thus far [5, 6, 7, 8]. The RCA is the easiest adder to comprehend. Full adders are coupled in parallel to form RCA. If higher order bits produce a carry, Carry Look Ahead (CLA) is formed after observing the lower order bits and is appended. Because CLA has fewer gates than RCA, the area and

propagation delay [9] are often less with CLA. But its uneven layout causes problems. Three bits are added in parallel (simultaneously) in Carry Save Adder, and carry is propagated through the stages. The precomputation of all possible carries is performed in Carry Select Adder, greatly reducing the latency. However, when compared to all the adders, the CIA is the best at solving these issues. Two RCA blocks with four bits each make up the Carry Increment Adder. Its main component is an increment block made up mostly of Half Adders (HA). By integrating the characteristics of two or more different adder operations, some hybrid adders may be made, which have a smaller area-on-chip and propagation delay than other adders.

Ripple Carry Adder

A full adder (FA) is a combinational circuit that receives two operand bits and a carry bit as inputs and outputs sum (S) and carry bit (Co). The operand bits are A, B, and Ci, respectively. This output Carry bit Co will act as the input Carry bit for the succeeding full adder with Sum=A⊕B⊕C and Carry=AB⊕BC⊕CA. The Sum and Carry Boolean equations are followed by the combinational circuit. A ripple carry adder is a straightforward higher operand adder solution for two operands A and B that is created by cascading n of these fundamental full adder units. This adder has a straightforward architecture and is simple to implement, however it has significant latency problems. Therefore, each full adder contributes to a 2-gate delay in the process of rippling the carry.

Carry Select Adder

Carry chooses adder, which pre- calculates the "Sum" and "Co" for the two potential scenarios of Ci = 0 and Ci = 1, is taken into consideration to shorten the time. A multiplexer receives the calculated Sum and selects the appropriate output based on the Ci from the previous stage. The delay of the rippling of Carry, which can use only one multiplexer for each stage, is decreased by the pre-computation of the Sum. When compared to ripple carry adder, carry select adder utilizes more hardware while providing the same amount of delay. Therefore, there is a trade-off between different adders in terms of area, power, and latency.

Carry Look Ahed Adder

To reduce the total delay in parallel addition, various methods have occasionally been offered [5]. One such method is to use intermediary words, such as "Generate (G)" and "Propagate (P)" terms, to generate the "Sum" and "Carry" outputs [5, 6]. create a term creates a carry-out independent of the carry-in, meaning that if both of its inputs, A and B, are '1', then G = A.B. regardless of the carry-in. When only one of the inputs is high, the Propagate term converts the input Carry to the output Carry, and is therefore defined as P = A⊕B. In the Propagate case the ‘Carry-out’ depends on the ‘Carry-in’, i.e., when ‘Carry-in’ is 0 ‘Carry-out’ is 0 and when ‘Carry-in’ is 1 ‘Carry-out’ is 1 and in the case of Generate, no matter what the ‘Carry-in’ is ‘Carry-out’ is always 1.

PROPOSED WORK

Ternary Ripple Carry Adder

The Ternary Ripple Carry is a circuit shown in Figure 1 that is used in digital circuit operations for adding n-bit integers. Binary ripples carry adders and ternary ripple carry adders have similar architectural designs, but there are differences in how inputs are applied to the complete adders [14]. In binary, there are only two possible logic values-0 (low) and 1 (high), however in ternary logic, there are three possible values - 0, 1, and z (high-impedance). This adder uses n complete adder circuits to perform addition operations on two n-bit ternary values.

Ternary Carry Look Ahead Adder

The Ternary Carry Look Ahead adder as shown in Figure 2.2 reduces the propagation delay by using two signals, carry generate and carry propagate. The carry generated is said to be 1 when the count is nonzero irrespective of the applied ternary inputs [13]. Coming to the propagate signal, it is said to be 1 when the input carry signal, Cin is equal to output carry. Over ripple carry adder, the propagation

delay is expected to be reduced as it avoids the carry being propagated from one full adder to another (n full adders in case of n bit adder).

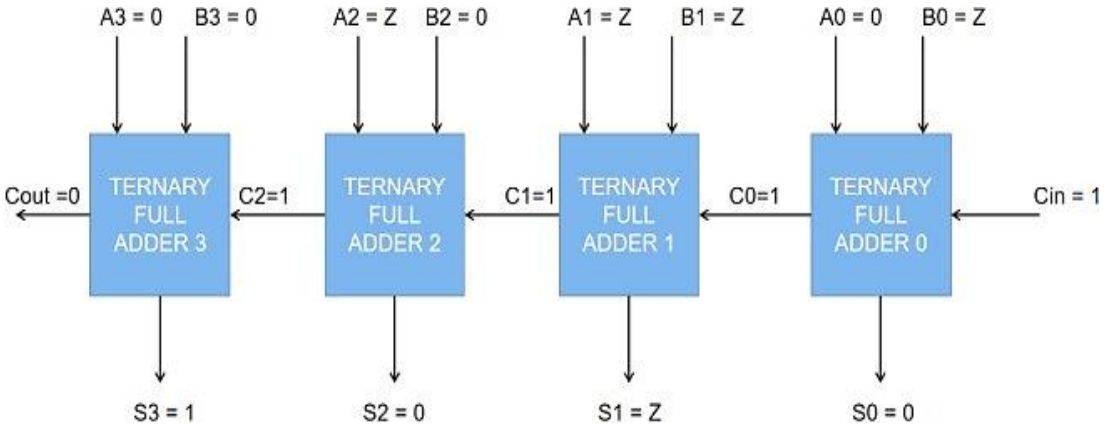

Figure 1. Ternary Ripple carry adder.

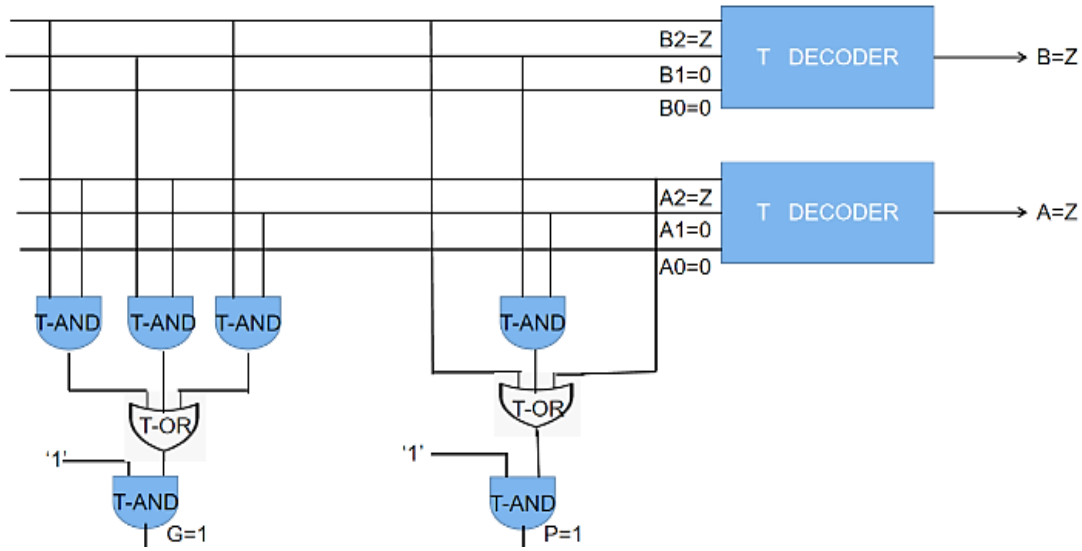

Figure 2. Ternary carry look ahead adder.

Ternary Carry Select Adder

In ternary carry Select Adder as Shown in Figure 3, there are three ripples carry adder blocks. Each RCA block has pre-defined C in as logic '0', logic '1' and logic 'z' [11]. The multiplexers here are of great advantage whose selection line is C in. Based on the Cin, the selection of the 4-bit sum and carry is signaled as output with the help of ternary multiplexer. The ternary multiplexer has three inputs, one selected output and one selection line. This is one of the high-speed adders which can be used for various applications.

Ternary Carry Skip Adder

The ternary skip adder as shown in Figure 4 is a sophisticated adder. There is usage of the propagate signals which are derived from carry look ahead adder [10]. The full adder blocks give out the sum values. The advantage of skip adder is that in certain cases, the entire calculation of carry could be skipped. Suppose all the propagate signals p0, p1, p2, p3 are equal and non-zero, then the applied input signal Cin is directly sent as the output carry signal, Cout. Hence, by "skipping" the propagation of carry from all the full adder blocks. That reduces the delay which makes it a high-speed adder.

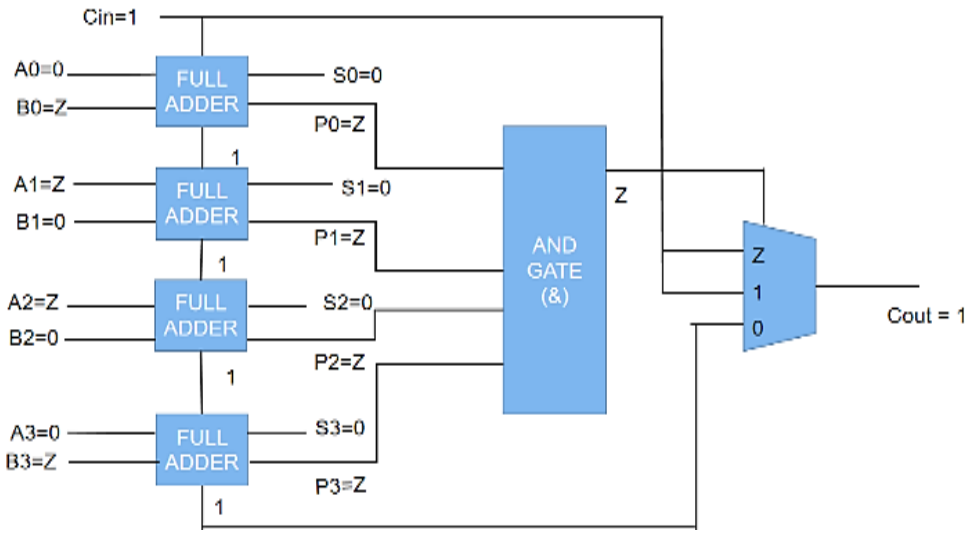

Figure 3. Ternary carry selects adder.

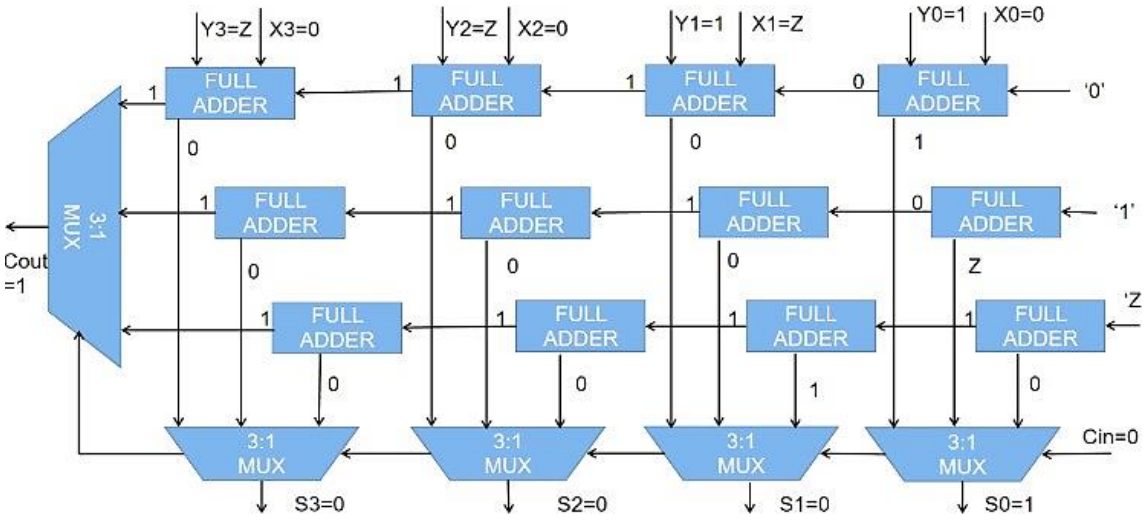

Figure 4. Ternary carry skip adder.

Carry Save Adder in Ternary

A ternary carry-save adder as shown in Figure 5 is a type of adder that can efficiently perform addition of large ternary numbers. It is a variation of the regular ternary adder, but instead of computing the final sum directly, it separates the sum into three parts: the ternary sum bits, the ternary carry bits, and the ternary overflow bits.

The ternary sum bits are computed using a regular ternary adder, while the ternary carry and overflow bits are stored separately. The carry and overflow bits can be added together using a smaller number of adders than the sum bits, which reduces the overall complexity and size of the circuit [13]. Additionally, carry-save adders can be easily pipe-lined, which further improves their performance.

SIMULATION RESULTS

Any digital application's performance is evaluated by considering the variables propagation delay and power dissipation. the propagation delay reduction utilized to implement high-speed applications. Low power-based applications can be implemented with a reduction in power dissipation. However, as not all circuits can minimize power consumption and propagation delay, a trade-off between the two must always be maintained. Observe the functional behavior at each level when building the fundamental primitive elements in advance to analyze the ternary design process. Then, performance

indicators such as power and delay are scrutinized. Finally, Tables nos. 1, 2, and 3 below compare the evaluation parameters of several adders. The functional verification of the adders is carried out utilizing various Verilog HDL modelling techniques. The performance metrics values provide information on how to implement sophisticated digital tasks with a smaller chip and fewer interconnections. From Table 1, it can be shown that the chip's area decreases to 40.7% in area (LUT slices) as compared to binary-based logic circuits. In comparison to binary-based logic circuits, the chip's power dissipation decreases to 76.26%, as shown in Table 2. According to Table 3, the chip's delay decreases to 49.57 seconds when compared to binary-based logic circuits.

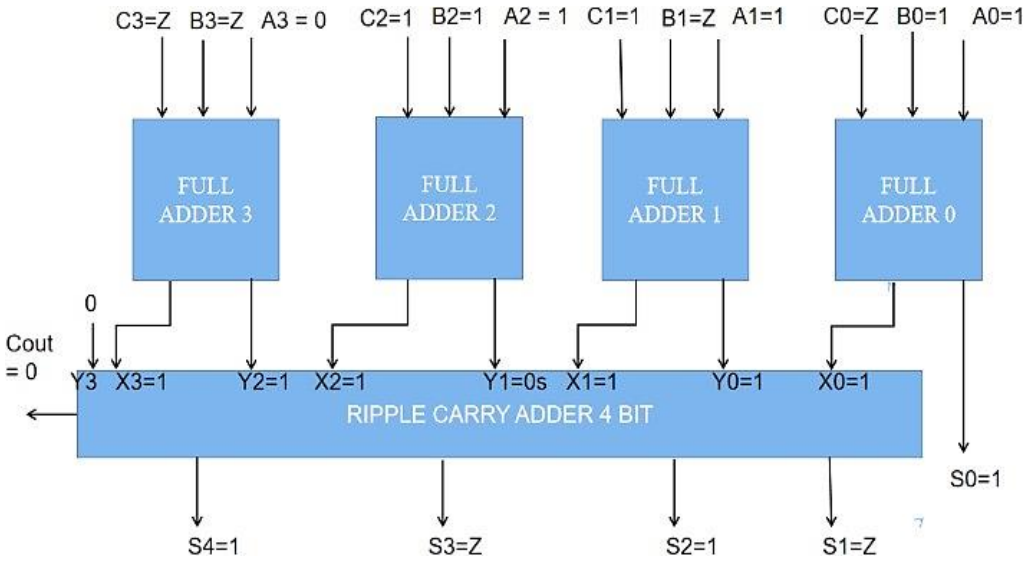

Figure 5. Ternary carry save adder.

Table 1. Area Comparison between binary and ternary.

Adders	Binary (number of LUT Slices)	Ternary (number of LUT Slices)
Ripple carry Adder	6	4
Carry look ahead Adder	6	4
Carry save Adder	9	5
Carry Select adder	6	3
Carry skip Adder	7	4

Table 2. Power comparison between binary and ternary.

Adders	Binary (watts)	Ternary (Watts)
Ripple carry Adder	3.036	0.864
Carry look ahead Adder	3.048	0.788
Carry save Adder	3.866	0.928
Carry Select adder	2.766	0.249
Carry skip Adder	2.773	0.861

Table 3. Delay comparison between binary and ternary.

Adders	Binary (nsec)	Ternary (nsec)
Ripple carry Adder	1.728	0.893
Carry look ahead Adder	1.551	0.898
Carry save Adder	2.156	0.893
Carry Select adder	1.551	0.757
Carry skip Adder	1.566	0.822

CONCLUSION

The functional verification of several ternary logic gates, including and, or, x-or, x-nor, nand, nor, and inverter primitives, is carried out in the proposed study. Ternary adder circuits are implemented, including ternary ripple carry adders, ternary CLAs, ternary save adders, ternary select adders, and ternary skip adders. With the XILINX ISE DESIGN SUITE, performance parameters like area, latency, and power were observed. Verilog HDL, a descriptive programming language, is used to implement the functional behavior of digital applications. Ternary circuits outperform binary ones by 49.5% in terms of delay, 76.26% in terms of power, and roughly 40.7% in terms of area (LUT slices). As a result, these ternary-based logic applications are appropriate for low power ones.

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