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# The Past, Present, and Future of Power Conversion Technologies for Computer, Networking, and Telecom Power Systems

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***Abstract***

*The power systems of modern computers, networking, and telecom equipment face formidable challenges due to the ongoing increase in power-density and efficiency requirements. Significant technological breakthroughs in system designs, devices and materials, topology optimization, and packaging/thermal design will be necessary to meet these objectives. To address these challenges, ongoing research and development efforts are being conducted in academia, industry, and government institutions. These efforts aim to revolutionize power system designs, improve energy efficiency, and meet the increasing power demands of contemporary computer, networking, and telecom equipment. This entails developing effective voltage regulators, power converters, and energy storage solutions, while also advancing control algorithms and intelligent power management methods to enhance power consumption optimization and minimize inefficiencies. This study identifies and briefly discusses the main technological issues and emerging trends in each of these important technological fields.*

**Keywords:** Power systems, challenges, growth, power-density, efficiency demands, contemporary computer, networking, telecom equipment

## INTRODUCTION

Power conversion equipment used in computer and communications power systems has faced steadily rising power density and efficiency issues ever since the dawn of the miniaturization era, sparked by the microelectronics revolution in the late 1950s and early 1960s. Prior to the late 1960s, the introduction of high-voltage bipolar junction power transistors opened up a significant opportunity to decrease the size and weight while improving the efficiency of power conversion circuits. This breakthrough enabled the replacement of linear power supplies with high-frequency switch-mode power supplies.

Linear power supply technology frequently does not give any meaningful prospects for weight and size reduction because the line-frequency transformer and heatsink are primarily responsible. Additionally, due to the efficiency of linear processes, there are extremely few chances to increase efficiency.

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In general, the efficiency and size optimization of switch-mode power supply is dependent on determining a switching frequency that optimizes the trade-off between conduction and switching losses.

Although switch-mode power supply technology based on bipolar-junction transistors has dramatically improved power density compared to

 

linear power supply technology, more power density enhancements were made possible by the development of power MOSFET (metal oxide semiconductor field effect transistor) devices in the early and mid-1970s. Power magnetics improvements and MOSFET technology allowed for a considerable rise in switching frequency and a consequent decrease in magnetic component size. Early switch mode power sources using bipolar junction power semiconductors had a frequency range of only a few kilohertz.

Switching frequencies can now reach the 100-kilohertz and even megahertz range thanks to MOSFET technology. The maximum switching frequency of a power converter is determined by factors such as its output power level, input voltage range, and the need for galvanic isolation, as depicted in Figure 1. As illustrated, the typical switching frequency range of DC-DC converters is higher than that of off-line converters. Current low-power, non-isolated voltage regulators (VRs) and point-of-load (POL) converters, as shown in Figure 1, operate at switching frequencies exceeding 1 MHz. In contrast, transformer-isolated AC-DC converters, which cater to RMS (root mean square) line voltages ranging from 90 to 265 V, usually operate at switching frequencies ranging from 70 to 200 kHz.

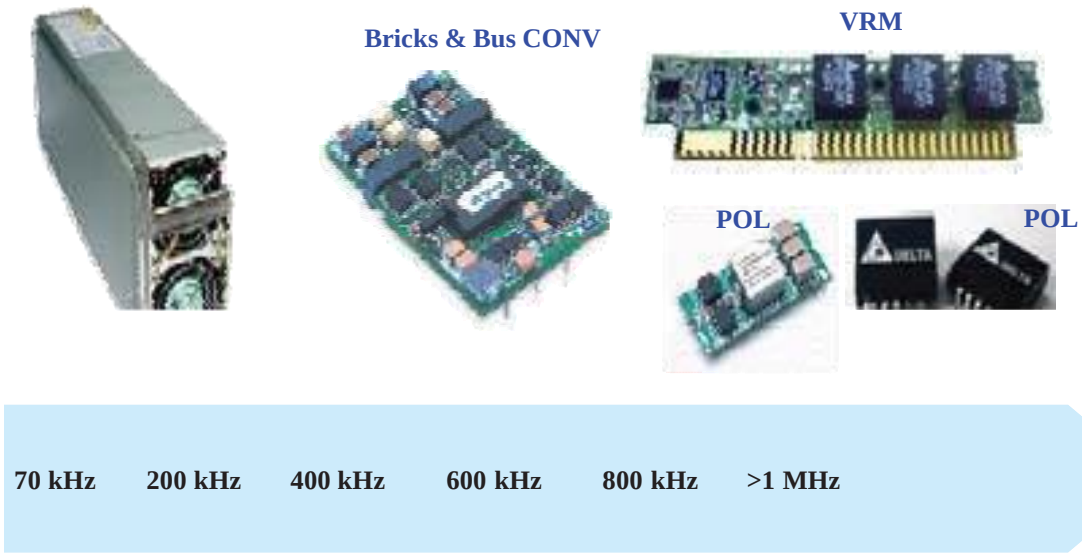


**Figure 1.** Typical switching frequency ranges of today's power converters. CONV, converter; POL, point-of-load; VRM, voltage regulator module.

The output to input voltage ratio alone determines the power supply. However, because it does not require huge line-frequency magnetics and decreases the size of heatsinks due to much higher efficiency than linear power supplies, switch-mode power supply technology offers a significant reduction in size and weight.

The first notable improvements in power densities in DC-DC converters were made in the middle of the 1980s when Vicor Corporation unveiled a range of high-frequency DC-DC modules. Vicor was able to increase the power density of 48-V input DC-DC modules, also known as "bricks," into an unprecedented range of 10 to 20 W/in$^3$ by using proprietary zero-current switching quasi-resonant technology and advanced packaging as shown in Figure 2 [1]. This trend of rising power density has persisted ever since, allowing for today's 3.3 off-line power supplies did not experience a significant change in power density until the internet began to expand quickly in the late 1990s. This unprecedented increase in the use of data-processing, networking, and storage equipment resulted in a high demand for equipment and, as a result, for power supplies with significantly higher power densities. The power density of AC/DC power supplies, such as notebook adapters, multiple-output power supplies, and server front ends for distributed power systems, has greatly increased over the previous 7 to 8 years, as

 

shown in Figure 3. For example, a decade ago, the power density of a server's front-end power supply was typically in the 5 W/in$^3$ range, the power density of supplies today is in the range of 20 to 30 W/in$^3$.

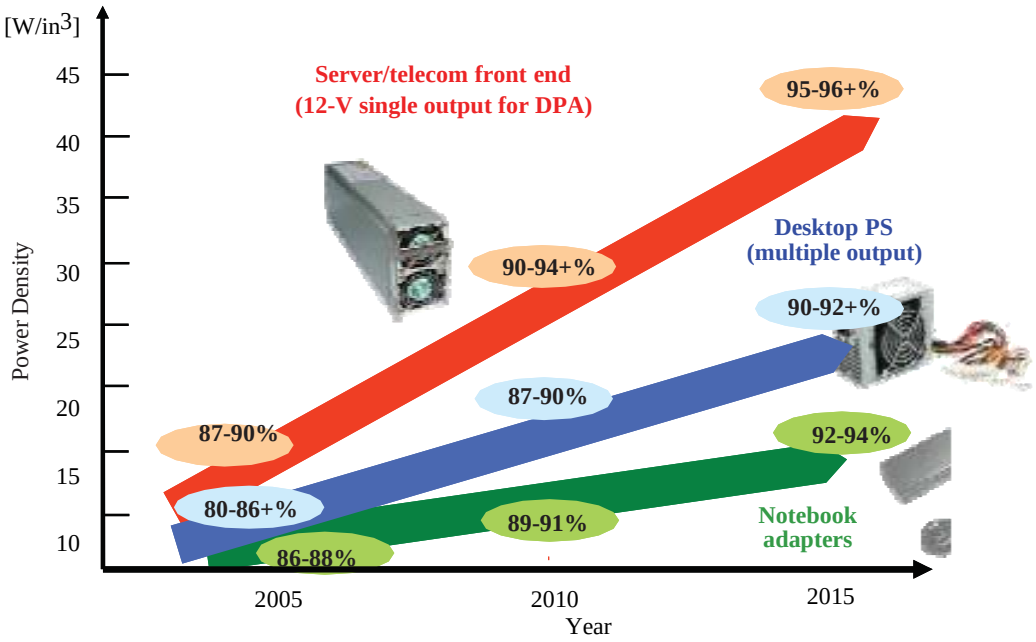


**Figure 2.** Past, present, and projected output current capability of DC/DC bricks. Data given for bricks with 3.3-V output and 36- to 75-V input voltage range.

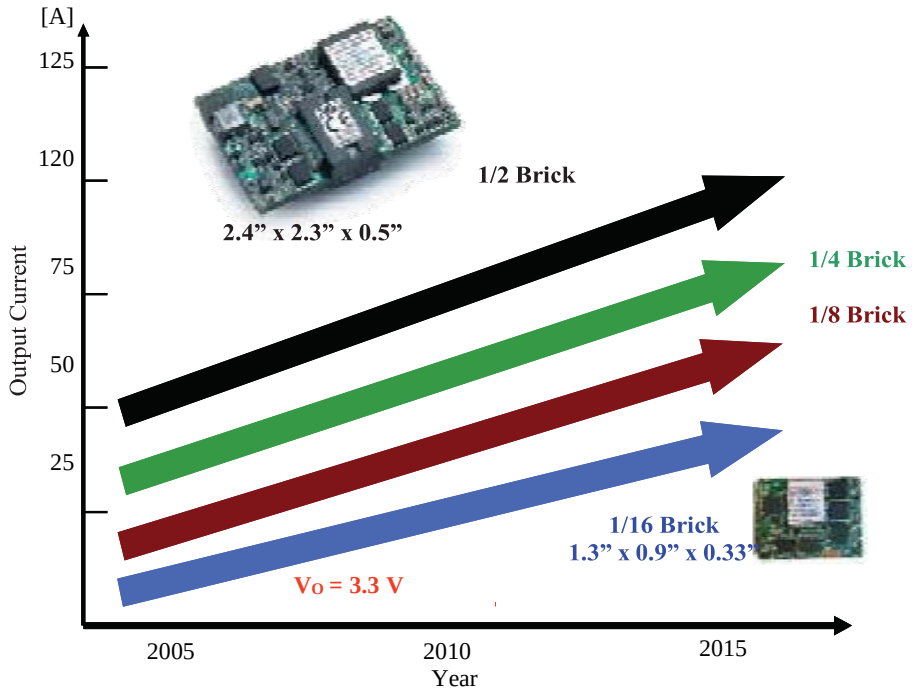


**Figure 3.** Past, present, and projected power densities and efficiencies of AC/DC notebook adapters, multiple-output power supplies, and server front ends for distributed power systems.

As this trend continues, power supplies in excess of 40 W/in$^3$ will be available in a few years. The remarkable advancements in power density can be attributed to several factors, including the availability of improved components, an enhanced comprehension of design optimization trade-offs leading to increased efficiency, and the adoption of contemporary packaging techniques.

 

## PARADIGM SHIFT

Up until recently, power density requirements dictated the majority of efficiency increases for power conversion circuits because higher power densities are only possible with appropriate incremental gains in full-load efficiency that do not negatively impact thermal and acoustic performance. As a result, improving full-load efficiency has always been a design goal. But in the early 1990s, the rapid development of consumer electronics and data-processing technology had led to the introduction of a number of specifications, largely voluntary, designed to reduce idle-mode, or light-load, power usage. Power supply manufacturers have significant design hurdles in order to meet these ever-stricter light-load efficiency criteria, most notably those outlined in German Blue Angle, U.S. Energy Star, Japan Top Runner, and ECoC (European Code of Conduct) specifications [2]. As a result, both power supply manufacturers have invested a lot of money in research and development, and control IC providers to developing technologies to comply with these specifications [2–5].

Consequently, enhancing full-load efficiency has consistently remained a key objective in design, prioritized by customers' performance expectations. This emphasis on efficiency stems from economic considerations and environmental issues arising from the rapid and extensive expansion of the internet infrastructure, coupled with the relatively low energy efficiency of power delivery systems in large-scale internet equipment hosting facilities Referring to Figure 4, which presents a block diagram of a standard power delivery system in a large data center (server farm/hotel), it is evident that approximately 2 W are wasted in power conversion and cooling for every watt utilized in data processing. As datacom equipment prices continue to decline, the lifetime electricity expenses have become a significant portion of the initial purchase cost. Presently, the expenditure on power and cooling surpasses the acquisition cost within approximately 3 years [6]. With the increasing influence of energy costs on the total ownership expenses, efficiency factors have started to significantly affect equipment procurement decisions.

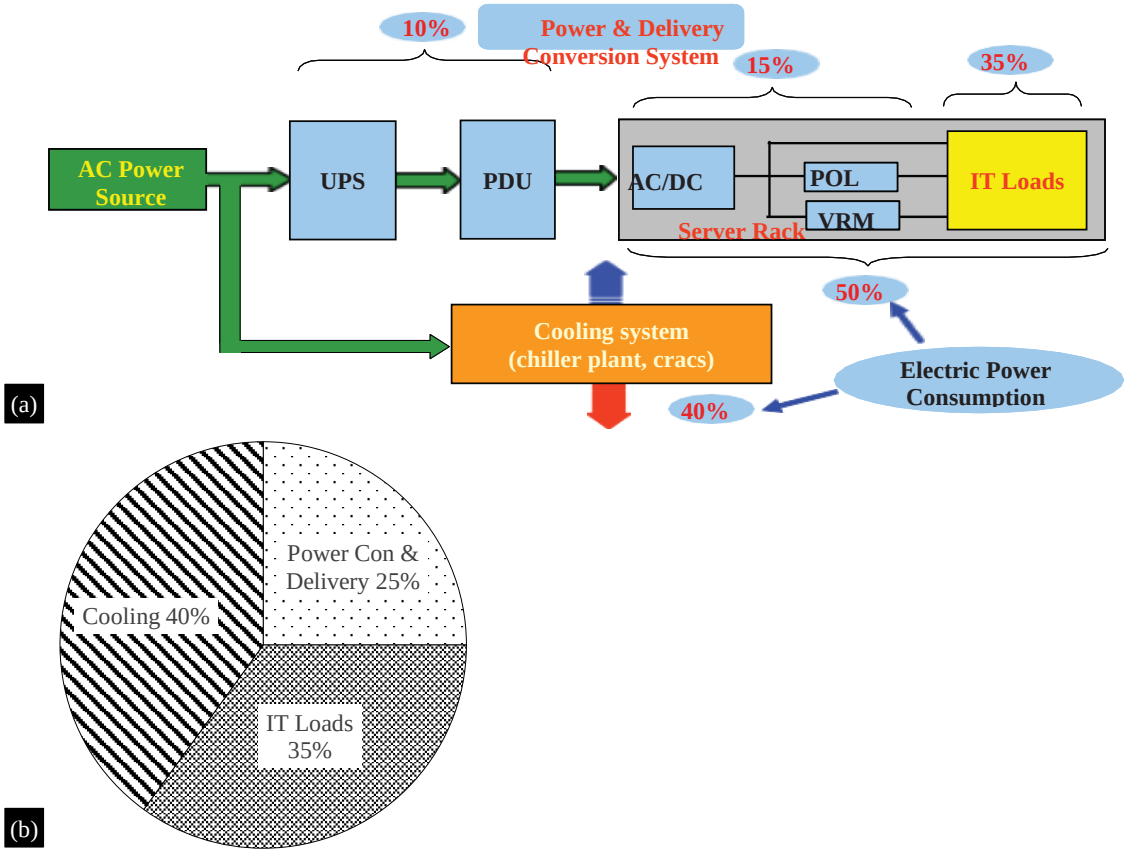


**Figure 4.** Power delivery system for large data centers (server farms/hotels): (a) block diagram; (b) power consumption breakdown of typical large data center.

 

Furthermore, the escalating power consumption of IT equipment, especially in rapidly expanding large data center facilities, is beginning to pose significant environmental consequences. It is estimated that 5% of today's global energy consumption can be attributed to computing services which is responsible for approximately 1.4 trillion tons of $CO_2$ emission, which is far more than the environmental impact of the entire aviation industry [7]. With projected future annual power consumption increases of data centers in the 10% to 15% range, the environmental concerns have prompted various initiatives to compel makers of IT equipment to increase the power conversion efficiency of their equipment. In fact, the efficiency targets for AC/DC server power supplies defined in 80Plus [8] and the Climate Saver Computing Initiative (CSCI) [9] specifications have already become de facto industry standards. These four-tier specifications define target efficiencies at 100%, 50%, and 20% load for each tier (bronze, silver, gold, and platinum). The highest tier, 80Plus platinum level, requires that minimum efficiencies of a 12-V-output server AC/DC power supply measured at the line voltage of 230 V be at least 91%, 94%, and 90% at 100%, 50%, and 20% load, respectively.

Recently, in addition to the efficiency requirements, the 80Plus and CSCI documents also have included power-factor specifications. Moreover, it is reasonable to expect that in the near future, the specifications will be extended down to 10% of the load. The 80Plus specifications are also being gradually incorporated into U.S. Environmental Protection Agency's (EPA) Energy Star specifications [10].

It does, however, necessitate major technological breakthroughs in the power conversion and delivery sector, as well as in the cooling system and the power consumption of the data-processing circuits themselves, in order to reduce the amount of electricity wasted in large data centers. The major CPU (central processing unit) manufacturers are constantly developing technology targeted at lowering power consumption without compromising performance. Some of the most recent techniques for reducing power consumption at the component and equipment level include technologies like load-dependent CPU speeds, native multi-core processors, and internal memory controllers [11, 12]. Software methods are being developed at the system level to decrease the power consumption of data centers through dynamic optimization of data processing capacity utilization [13]. These "server virtualization" solutions use less energy. Cooling equipment manufacturers and system designers are also working on technologies to improve the cooling efficiency of data centers. The optimization of fans/blowers, cooling medium, and data center floor layout are currently the areas of major focus. System-level techniques such as system-integrated intelligent cooling that is based on actual thermal load and predicted demand are also being rapidly developed [13].

## TECHNOLOGY CONSIDERATIONS

The major activities aimed at improving the performance of the power conversion and delivery system of data-processing and telecom equipment are always focused on four key technology areas, as shown in Figure 5.

Future efficiency and power density improvements are anticipated to be primarily driven by system architecture and power management optimization, as well as by advancements in packaging and thermal management techniques, whereas the major performance improvements in the past had been primarily driven by refinements in power converter topologies and advancements in semiconductors and magnetic materials. Because of this, current research and development (R&D) efforts are being directed towards system-level architectural optimization and the deployment of load-activity-based power management rather than converter-level topology optimisation [14, 15]. The digital power management bus has already been standardized by PMBus Implementers Forum [16] in recognition of the fact that power management (PM) capabilities will be a necessary and essential component of future power systems. Products that are PMBus compliant have recently been released by a number of IC providers for power conversion applications [17–21]. The majority of these ICs provide digital control in addition to PMBus compliance [17–21].

 

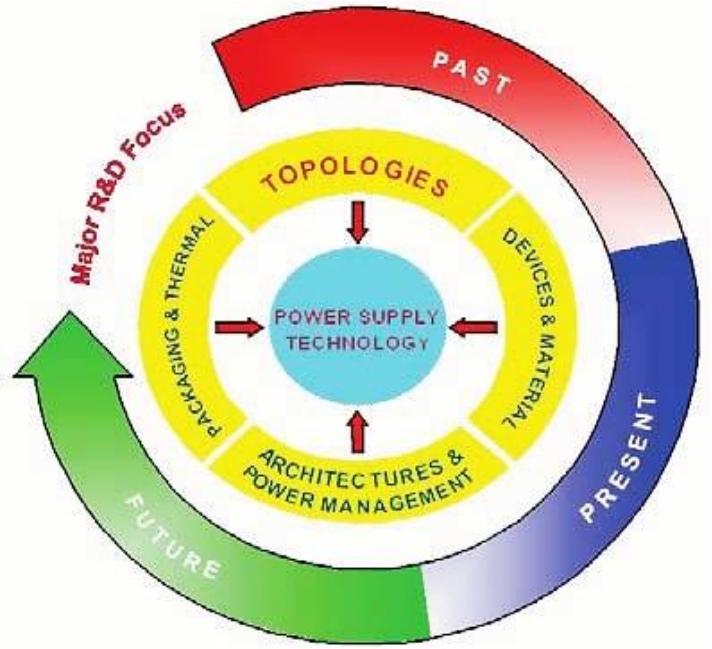


**Figure 5.** Major power supply technology areas: past, present, and future focus.

The incorporation of adaptive control algorithms that are dependent on the load and the implementation of adaptive dead-time regulation for switches allows digital control to facilitate efficiency optimization of converters across the entire load spectrum. Additionally, digital power management enables performance optimization at the system level [19]. Additionally, with the advent of digital technology, the customization of control, monitoring, protection, and housekeeping features of power converters has been moved from hardware to software. This significantly reduces the time required for product design, lowers the cost, and also enables simple parameter adjustment (tweaking) even after the product has been put into use.

**Architectures**

The two main types of power delivery architectures for data processing and telecommunications equipment are centralized and distributed power architectures (DPA). Because of the spread nature of the load, power delivery systems used in data centers and telecom facilities are naturally distributed. Data centers employ AC-bus distribution for DPA, as shown in Figure 4, while telecom facilities use -48-V DPA with DC-bus distribution, as shown in Figure 6.

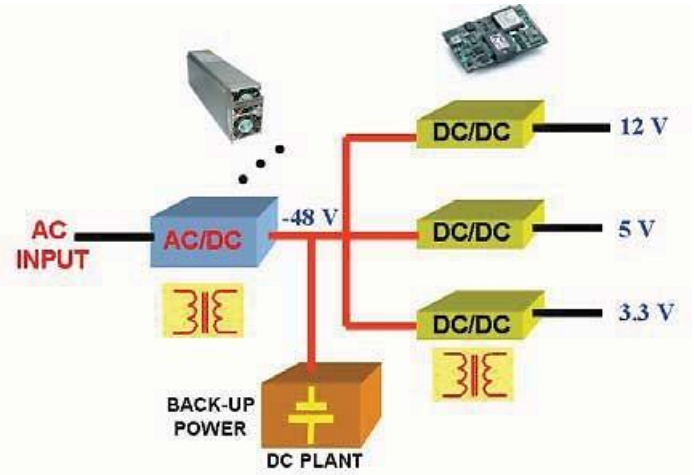


**Figure 6.** Distributed power architecture (DPA) in telecom systems.

 

At the equipment level, centralized power architecture (CPA) has only been used in cost-sensitive, low- to medium-power applications like personal computers and workstations, whereas DC-bus distributed power architecture has been used in high-power systems like mainframe computers and high-end servers, as well as in networking equipment. At higher frequencies, a higher DC-bus voltage is typically recommended to lower the distribution losses at higher powers. As a result, a high-voltage bus with a typical voltage of 350 V is used to implement the DPA in mainframe computers, which typically consume tens of kilowatts of power. The 12-V DC bus is used to construct the power systems of high-end servers, whose power consumption is typically restricted to several kilowatts. Finally, the 48-V DC bus is used by the DPAs in networking devices like routers and modems.

Additionally, the development of the intermediate-bus architecture (IBA), depicted in Figure 7, which has been widely used in networking applications, was made possible by the availability of cost-effective POLs. In the IBA, an AC/DC front-end converts the AC-line voltage to a 48-V DC voltage, which is subsequently stepped-down to a lower intermediate-bus voltage (IBV) in the 8- to 12-V range by an isolated bus converter (BC). IBV is changed to the desired load voltages using non-isolated POL regulators. In order to maximize the power system's conversion efficiency, the IBV value, or step-down ratio of the BC, is often established. POLs provide output voltage regulation, thus the IBV, or bus fluctuations, do not require strict regulation.

It should be noted that in applications that do not use a 48-V battery back-up, or do not require a 48-V bus for any other reason, the IBA might not be the optimal architecture. Namely, in the IBA, the number of conversion stages is not minimal since power is processed by two cascaded isolated converters.

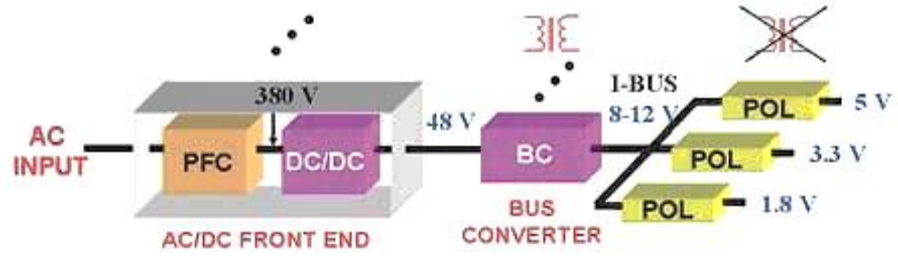


**Figure 7.** Intermediate-bus architecture (IBA).

As can be seen in Figure 7, first the front-end converter DC/DC stage, Reduces the 380-V output of the PFC (power factor controller) to 48 V, and BC then steps down this voltage to the final IBV value. The number of conversion stages can be reduced by using a high-voltage (HV) BC to step the 380-V PFC output voltage directly to the necessary IBV value, as shown in Figure 8. The HV DC-bus IBA and low-voltage (LV) DC-bus DPA are obtained depending on the system partition, or whether the HV BC is left on the board or is integrated into the front-end, as shown in Figure 8(a) and (b), respectively. These two architectures' marginally varying distribution losses are the cause of the modest performance variation between them. The vast majority of today’s servers are supplied from single-phase AC lines.

The most recent R&D effort is concentrated on the examination of architectures with two distinct LV DC buses in order to further increase the power conversion efficiency of high-end equipment, which normally demands rather huge power [22]. According to the preliminary evaluation findings, this dual-bus architecture using semi-regulated BCs may provide greater efficiency than the traditional single-bus implementation.

While optimizing the power system architecture and increasing conversion efficiency at the equipment level undoubtedly help reduce power consumption in large data centers, even more significant energy savings might be possible by improving the facilities' power conversion and distribution systems. As shown in Figure 4(a), large data centers employ redundant AC uninterruptible

 

power supplies (UPSs) service in case of power blackouts. On-line operation of UPSs is preferred over off-line operation because of a significantly better reliability. However, due to continuous power processing, the on-line UPS back-up approach is less efficient than the off-line approach.

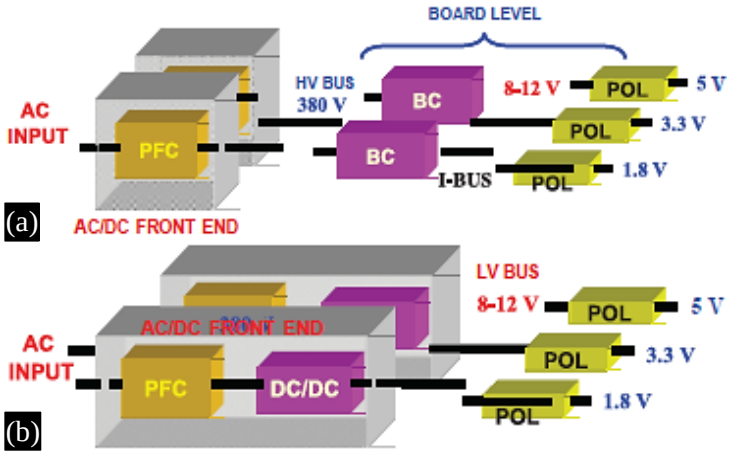


**Figure 8.** AC/DC DPA system architectures with minimal number of conversion steps: (a) high-voltage (HV) distribution bus IBA; (b) low- voltage (LV) DPA

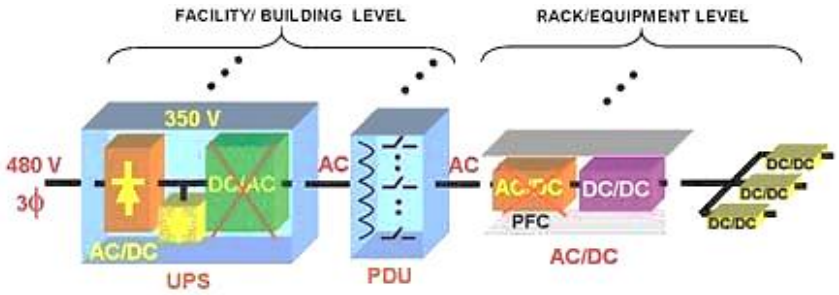


**Figure 9.** Simplified block diagram of data center power conversion and delivery system.

As shown in Figure 9, the on-line AC-UPS backed-up power delivery system does not appear to be suitable because the number of conversion stages are not decreased. The conversion of the DC/AC in the UPS and the AC/DC in the PFC stage of the equipment's AC/DC power supply, in particular, seems unnecessary. In fact, these two conversion stages can be eliminated using the HV DC-bus distribution shown in Figure 10. This HV DC-UPS power system not only outperforms AC-UPS power systems in terms of efficiency, but also offers a degree of reliability comparable to a telecom -48-V DC-bus system. The HV DC-bus is a universal-current bus in that AC/DC converters can operate on it.

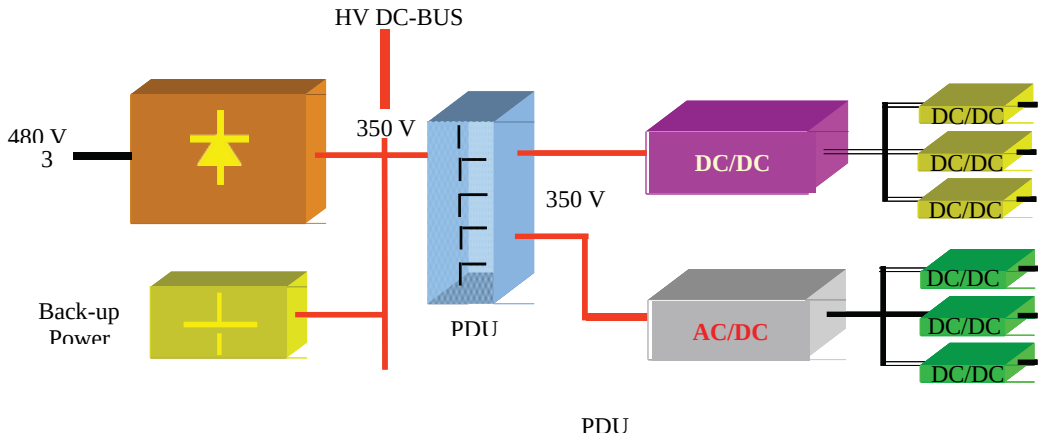


**Figure 10.** High-voltage DC-bus data center power system.

 

Integration of alternative energy sources into power-distribution systems is also making the HV DC-bus architecture more appealing than the conventional AC-distribution architecture. In fact, photovoltaic and fuel-cell energy sources that are intrinsically DC sources can be connected to the DC-bus with minimal amount of power conditioning.

A number of HV DC-bus architecture implementations have been under consideration [23]. Generally, the implementations that use a non-isolated AC/DC stage [23–27], that is, direct line rectification, exhibit higher conversion efficiencies compared to the implementations that employ isolated AC/DC front end to generate the HV bus [26–29]. However, the use of non- isolated rectifiers raises a number of concerns related to the safety of distributing high voltage around the data center so that isolated rectifiers seem more suitable for this application. Another major issue in the HV DC-UPS architecture that has yet to be completely resolved is related to the fault removal, specifically to the availability and performance of HV DC breakers that are required in HV DC-bus systems.

Depending on the AC/DC front-end implementation and the mix of DC and AC loads (equipment), it has been shown that the HV DC-UPS design delivers a 5% to 15% improvement in power system efficiency compared to the AC-UPS system The electric energy savings of HV DC-UPS over the corresponding AC-UPS counterpart are in the range of 10% to 25%, taking into account the power consumption of the cooling system. HV DC-bus architecture can increase the power density of the power conversion and delivery system by 20% to 30%, allowing for the installation of more equipment in already-existing data center facilities. This is due to improved efficiency and decreased heat dissipation.

**Topologies**

Ever since the introduction of switch-mode power supplies, the major R&D effort has been dedicated to finding topologies that offer improved conversion efficiencies and power densities.

During the late 1970s and early to mid-1980s, as MOSFET technology progressed, there emerged a significant prospect of reducing the size of power converters by augmenting the switching frequency. This led to a concentration of topology development and optimization efforts on mitigating switching losses of semiconductor devices, which were regarded as a primary bottleneck hindering the achievement of high-frequency operation in "hard" switched pulse-width modulated (PWM) converters.

Generally, this extensive R&D effort was centered around resonant power conversion that eventually led to the development of new families of resonant converters such as zero-current-switching (ZCS) and zero-voltage-switching (ZVS) quasi-resonant (QR) and multi-resonant (MR) converters, as well as class-E converters. By 1988, power converter prototypes operating in the megahertz range and achieving power densities over 20 $W/in^3$ were reported. However, despite the initial keen interest in these technologies, the power supply industry has generally failed to cost-effectively incorporate them in their products. The only exception has been Vicor Corp., the company that did pioneering work in the development of ZCS QR technology, which has been the only power supply manufacturer to offer a line of high-density DC/DC converters employing this technology [1].

The interleaving technology has been extensively used in applications like POL and VRM. In reality, the only method that can continue to offer the required efficiency, power density, and transient-response performance in VRM applications is the interleaved synchronous-buck converter. The interleaving method is also widely used in low-profile converters because it allows for the use of smaller magnetic cores by equally dispersing the magnetic components. High-power boost PFC front ends for AC/DC converters are increasingly being constructed using interleaving technology. It is reasonable to assume that when digital technology is used more widely in the future and makes interleaving control implementation significantly simpler, the use of the interleaving approach will increase.

Nevertheless, the development of QR and MR converters has been an important milestone in the advancement of high-frequency switch-mode power supply technology because it resulted in a much

 

better understanding of the effects of parasitics on switching losses. This knowledge has been key to the development of components with minimized parasitics that eventually led to significant performance improvements of conventional "hard"-switched PWM converters at higher switching frequencies.

Recognizing that increasing the switching frequency and power density must be done without performance degradation, the focus of R&D effort in the late eighties has shifted to finding topologies that offer a favorable trade-off between switching and conduction losses.

Specifically, numerous topologies that combine the desirable features of square-wave PWM converters such as constant-frequency operation and minimal component stress and conduction loss with soft switching of resonant converters have been introduced. The most prominent member among these topologies, known as soft- switched topologies, is the full-bridge (FB) ZVS PWM converter that employs constant-frequency phase-shift control. This topology, shown in Figure 11, has been extensively used in high-power server, telecom, and networking power supplies because of its excellent performance and scalability. Also, a number of soft-switched boost converters that are used in PFC implementations have found wide acceptance in commercial AC/DC power supplies. The main feature of these boost converters is the reduction of reverse-recovery- related losses by soft switching of the boost rectifier. However, since the introduction of silicon carbide (SiC) rectifiers that exhibit virtually no reverse-recovery charge, the employment of these soft-switching boost converters has been rapidly declining.

Given the demanding contemporary demands of simultaneously maximizing overall load range efficiency and power density, the primary objective of current topology optimization endeavors is to identify circuit configurations capable of operating at considerably higher switching frequencies while achieving high levels of efficiency. As a result, resonant techniques are presently being revisited because advancements in semiconductor and magnetic devices, introduction of DPAs, changes in power supply specifications, and improved design optimization tools and knowledge are all making the resonant topologies more attractive now than 10 to 20 years ago. For example, due to a relatively constant bus voltage in DPAs, the resonant converters are suitable for use in BCs, especially in unregulated BC (DC/DC transformer) implementations because of constant frequency operation. Currently, BCs employing the LLC (inductor-inductor-capacitor) series-resonant converter shown in Figure 12 that operate in the megahertz range are available.

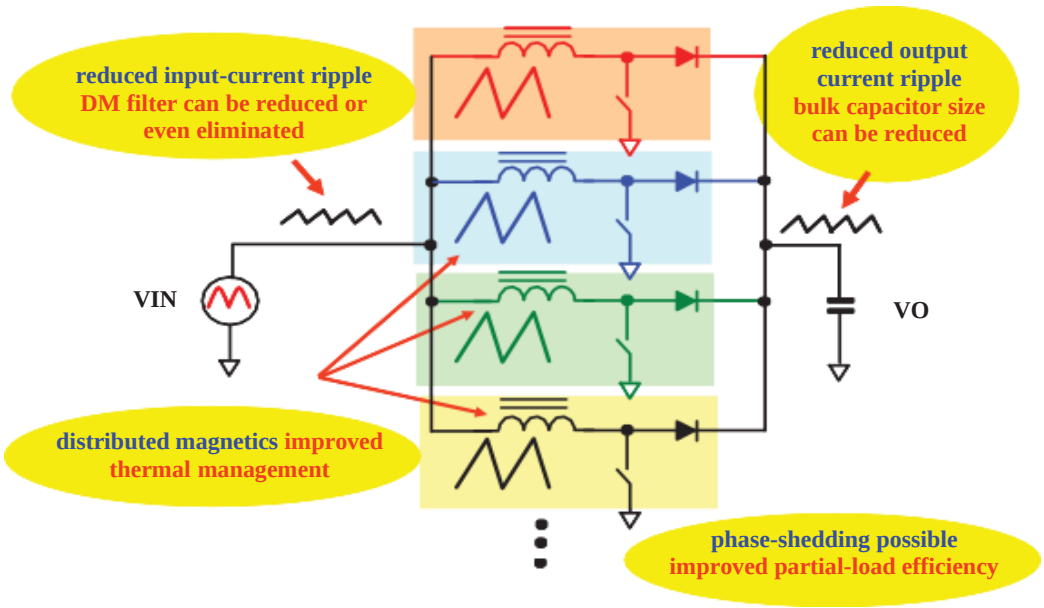


**Figure 11.** Interleaving technique benefits.

 

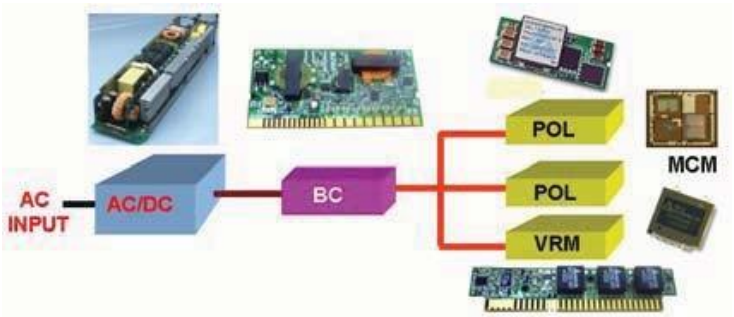


**Figure 12.** Current packaging of AC/DC power supplies and DC/DC converters.

Similar to this, the PFC front end, which acts as a pre-regulator to the output DC/DC stage in AC/DC power supplies, has improved the input-voltage conditions for the use of resonant converters. As a result, high-density, high-efficiency notebook adapters and server power supplies have found use for the resonant approach, notably the LLC topology. Last but not least, the widespread usage of synchronous rectifiers has also significantly rekindled interest in resonant power conversion, particularly in the LLC topology. In particular, the ZCS of the secondary side rectifiers is provided by the LLC topology, which is the preferred switching condition for synchronous rectifiers since it minimizes/eliminates switching losses brought on by the body diode's sluggish recovery property.

Another approach of getting power-density and performance benefits of increased switching frequencies without compromising the efficiency is the interleaving technique. Generally, interleaving offers a size reduction of magnetic components and other performance benefits by processing power in a number of power-conversion stages that are connected in parallel and operate at lower frequencies, The apparent switching frequency of the converter is increased by phase shifting (interleaving) the switching instances of the parallel modules by the number of interleaved modules. Besides the size reduction of magnetic components, the interleaving technique offers reduced input current and output-filter capacitor current due to a ripple-cancellation effect, which reduces the size of the input filter and the number and size of output-filter capacitors. In addition, the interleaving technique makes it possible to implement the phase-shedding control method that can improve a partial-load efficiency by progressively turning off phases of an interleaved converter as the load gets lighter.

The interleaving technology has been extensively used in applications like POL and VRM. In reality, the only method that can continue to offer the required efficiency, power density, and transient-response performance in VRM applications is the interleaved synchronous-buck converter. The interleaving method is also widely used in low-profile converters because it allows for the use of smaller magnetic cores by equally dispersing the magnetic components. High-power boost PFC front ends for AC/DC converters are increasingly being constructed using interleaving technology. It is reasonable to assume that when digital technology is used more widely in the future and makes interleaving control implementation significantly simpler, the use of the interleaving approach will increase.

Variations will continue to be employed in an overwhelming majority of power supplies. However, due to the increasing use of synchronous rectifiers in low-output-voltage applications, major development effort will be dedicated to the implementation and performance optimization issues of synchronous rectifiers in these topologies. Specifically, the lack of adequate synchronous-rectifier drivers is still one of the major obstacles in further improvement of efficiency of high-frequency isolated power converters.

Finally, in AC/DC power supplies, the front-end PFC converter and its associated electromagnetic interference (EMI) filter and energy-storage (bulk) capacitor will be the key design optimization emphasis. The main R&D effort has been focused on further minimizing the conduction losses by integrating the rectifier and boost functions and minimizing the number of semiconductors in the power

 

processing path. SiC rectifiers are now commercially available, virtually eliminating the reverse-recovery-related switching losses. High-end single-phase, AC/DC power supply, particularly those that must achieve efficiencies above 95%, are slowly adopting these so-called "bridgeless" PFCs. The size of the energy-storage (bulk) capacitor and the EMI filter are another significant obstacle in the design optimization of AC/DC front ends and are now important obstacles to increasing the power.

**Components and Materials**

Generally, advancements in semiconductor technology have always been the major thrust behind efficiency and power density improvements in power conversion circuits. Specifically, the dramatic improvements in AC/DC power supply performance that have been achieved in the past decade or so have been primarily brought about by extraordinary reduction of the on-resistance of high-voltage MOSFETs and equally impressive improvements in reverse-recovery characteristics of high-voltage silicon (Si) rectifiers. For example, the super-junction technology has enabled a reduction of the on-resistance of today's 600-V MOSFETS down to 45 mohm, which is approximately 10 times lower compared to the on-resistance of state-of-the-art 600-V devices available in the 1990s. Similarly, today's high-voltage Si rectifiers exhibit a significantly lower reverse-recovery charge, which has improved efficiency and simplified the design of the boost PFC front end in AC/DC power supplies.

Continued reductions in the on-resistance of low-voltage MOSFETs used as synchronous rectifiers in applications with low output voltage have enabled additional efficiency gains. Modern 20- to 30-V synchronous rectifiers have an on-resistance of less than 2 mohm, whereas the best 100-V synchronous rectifiers have an on-resistance of only a few milliohms. Due to the need for packaging methods that provide an ultra-low package resistance such that the package resistance does not significantly affect the total component resistance, such minuscule on-resistances present a significant packaging problem.

By phase shifting (interleaving) the switching instances of the parallel modules by a number proportionate to the interleaved modules, the apparent switching frequency of the converter can be enhanced.SiC Schottky rectifiers at high voltages that do not A greater use of SiC and GaN technology is planned. Once SiC and GaN MOSFETs become readily available, which may happen in 3 to 5 years. In fact, 1200-V SiC MOSFET has just been introduced and engineering samples of GaN MOSFET up to 600-V rating are now available. With SiC and GaN MOSFETs that are projected to have much lower terminal capacitances and on- resistances of an order of magnitude lower than their Si counterparts, operation at much higher switching frequencies will be possible without efficiency degradation. This would make it possible to further reduce the size of magnetic components and boost the corresponding power density, particularly in non-isolated converters like those used in VRM and PFC applications. Due to efficiency degradation at higher switching frequencies brought on by switching losses in super junction devices caused by their increased terminal capacitances, the current design approach used in PFC front-end boost converters of pairing SiC rectifiers and super junction MOSFETs has generally failed to bring about significant improvements in power density. The conventional design approach to performance optimization of AC/DC power supplies is to lower the switching frequency because today's demands for optimum efficiency are driven by economic and environmental considerations. The performance of SiC rectifiers at low frequencies is only somewhat better than that of tailored fast rectifiers.

In general, advances in capacitor and magnetic technology have lagged behind those in semiconductor technology. In essence, there hasn't been any innovation in power magnetic materials for power transformers and inductors in a while. The primary focus of magnetics makers has been on the improvement of already available materials in specific frequency ranges and the diversification of core forms and sizes, especially low-profile planar cores. While better magnetic materials would undoubtedly aid in further optimizing the performance of power supplies, the primary basic barrier in high-frequency magnetic components is the copper loss owing to proximity and skin effects. In actuality, the main barrier to raising the switching frequencies of isolated converters is these losses, together with the switching losses of semiconductor devices.

 

Unlike the switching losses of semiconductor devices that can be reduced and even virtually eliminated through circuit techniques such as ZVS and ZCS, the skin- and proximity-effect losses can only be minimized to a certain extent through winding optimization techniques.

The use of SiC and GaN MOSFETs will not have a substantial impact on the power densities of isolated power supplies due to the limiting effect of transformer copper losses on pushing switching frequencies of isolated DC/DC converters significantly beyond their current ranges. Because SiC and GaN MOSFETs have lower on-resistances and terminal capacitances than Si technology, they will be able to achieve incremental efficiency gains that will result in a reduction in heat-sink space, which will directly impact power density. However, the substantially lower parasitic capacitances of SiC and GaN MOSFETs would notably benefit from switching frequencies remaining in the relatively low range, that is, approximately 100 kHz for high-voltage DC/DC converters utilized as the output stage in AC/DC converters.

Primarily driven by VRM requirements for smaller and better filter capacitors, low-voltage capacitor technology has made major advancements in the past decade. The most notable improvements have been made in the area of multilayer ceramic (MLC) and solid electrolytic chip (POS) capacitors mainly by increasing their capacitance and reducing their equivalent-series resistance (ESR). However, no comparable substantial advances in high-voltage electrolytic capacitors employed as energy-storage (bulk) capacitors have been observed. In fact, their volumetric efficiencies (capacitance/volume) are not much better than a decade ago. As the size of bulk capacitors continues to emerge as a major limitation to increasing the power density in applications with a hold-up time requirement, the capacitor manufactures are expected to focus their future effort in improving the volumetric efficiency of high-voltage electrolytic capacitors.

**Packaging**

Advancements in packaging technology and thermal management will be of paramount importance for future power-density improvements. In fact, the packaging and thermal issues are already the major hindrance to attaining higher power densities.

Generally, packaging and thermal concerns need to be addressed at each and every level, that is, from the component level to the board and power-supply box level, all the way up to the system level. Of course, at different levels the optimization focus is on different packaging and thermal aspects. For example, while at the device level the focus is on the minimization of package parasitics and thermal impedance, at the system level it may be the power density and cooling efficiency.

Off-line AC/DC power supplies have always used different packaging methods than DC/DC converters because of higher power levels, stricter safety and EMI regulations, and cost pressure, as seen in typically, through-hole and SMT (surface-mount technology) components, wire-wound magnetics, semiconductor devices in TO-220 and TO-247 packages mounted on heatsinks vertical to the main board, and electrolytic capacitors have been used to construct AC/DC power supplies. Contrarily, DC/DC converter modules have traditionally been constructed using only SMT parts, planar magnetics with multilayer board-integrated windings, horizontally positioned semiconductor components in small packages (SOIC, DPAK, and similar), and chip capacitors. Additionally, some of the low-power POLs of today are already constructed using monolithic integration of semiconductor components and multi-chip module (MCM) packaging techniques. One of the basic forms of packing methods is emerging: component integration, both functionally and physically. Switches, drivers, and control circuits are examples of semiconductor components that are increasingly used at the physical level through monolithic integration and/or chip co-packaging. In the future, this trend will undoubtedly pick up speed as more options become number of these integrated devices continue to grow. However, there have not been any analogous noteworthy developments in high-voltage electrolytic capacitors used as energy-storage (bulk) capacitors. Moreover, it is just a matter of time before advancement in packaging technology make integration of energy storage capacitors into the substrate/PCB (printed

 

circuit board) a reality. This will certainly create new opportunities for power density improvements such as, for example, the integration of the EMI filter.

The package optimization goal for DC/DC converters is to reduce board area, particularly the space occupied by low power protection, monitoring, and control circuitry. Either component integration or the use of microcontrollers and the firmware implementation of the functions can be used to achieve this. After the board area is reduced, the packaging density can be further boosted by stacking low-power passive or active components in three dimensions.

Monolithic integration and/or power micro electromechanical systems (MEMS) technology are already used in low-power POLs as the ultimate 3D packaging technologies, despite the possibility of using the package-on-package (PoP) approach to implement 3D packaging and increase the power density at higher power levels. The MCM technique is becoming a potential remedy for the range between these two power levels, as seen in Figure 13. As these two packaging technologies continue to advance, it may be anticipated that MCM and monolithic integration will be used at ever higher power levels.

In AC/DC power supplies, the major objective of the packaging/thermal R&D effort is to improve the cooling efficiency.

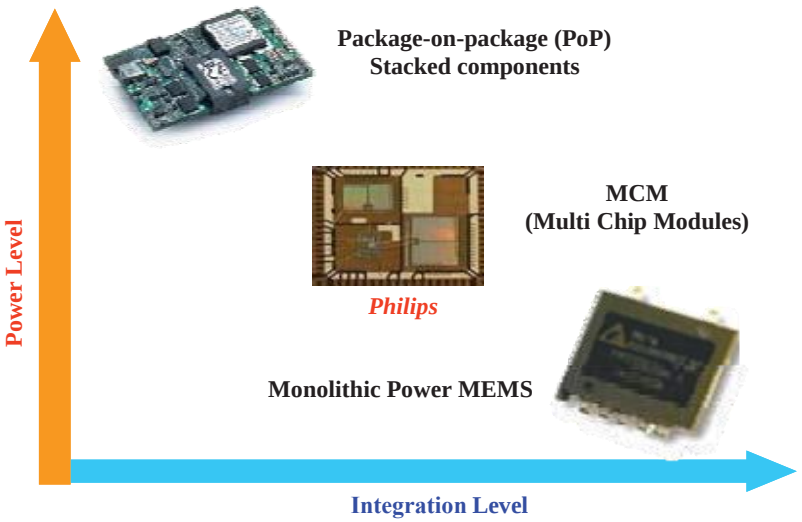


**Figure 13.** Packaging integration level and power level relationship.

Due to the higher volume utilization, or the increased volume of the power supply taken up by the components, the power supply decreases, and the airflow impedance rises. If cooling efficiency is not increased when the airflow impedance rises, the fan speed must be increased, which also raises the acoustic noise. To maximize volume utilization without significantly degrading acoustic noise performance is therefore the main problem in packaging and thermal design at the box level.

## SUMMARY

Efficiency optimization across the entire load range has been elevated to the forefront of today's datacom equipment performance requirements due to the sustained, aggressive growth of the internet infrastructure, the relatively low energy efficiency of the power delivery systems of internet equipment, as well as the rising cost of energy and environmental concerns. The only way to do this exceedingly difficult task, which is made even more difficult by the constant need for larger power densities, is through future significant advancements in power supply technology. Future efficiency and power density improvements are anticipated to primarily come from system architecture optimization and power management, as well as from advancements in semiconductor and magnetic component

 

performance, whereas the major performance improvements had previously been primarily achieved by topology refinements and improvements in performance of semiconductor and magnetic components.

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