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Design of Optimized Full Adder Using Noise-mitigation Techniques and Power Gating

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Abstract

With the advent of nanoscale technology, a new era of power consumption, speed, and reliability challenges for traditional static Complementary MOS (CMOS) logic has begun. To solve these problems, dynamic logic families—particularly domino logic—have emerged as potent substitutes that offer quicker processing speeds and lower power consumption. The design and optimization of a full adder circuit using domino logic is shown in this study. A dynamic domino logic technique is used to build the proposed full adder architecture, utilizing the benefits of the pre-charge and evaluation phases to improve performance. This work investigates the design and optimization of a complete adder circuit utilizing the domino logic dynamic logic paradigm, which stands out for having distinct pre-charge and evaluate stages. To maximize the inherent advantages of domino logic, our design integrates cutting-edge noise-mitigation techniques like power gating, noise-margin analysis, and synchronous clocking. Apart from capitalizing on the intrinsic benefits of domino logic, the suggested architecture integrates power gating, noise-margin analysis, and synchronous clocking to tackle issues related to noise and power usage. A significant percentage of noise and power reduction is noticed.

Keywords: Full adder, domino circuit, dynamic logic, noise-margin, power gating, synchronous clocking, power consumption, CMOS

INTRODUCTION

Selecting the right logic style is essential in the never-ending quest to improve the functionality and efficiency of digital circuits. The new age of power consumption, speed, and reliability difficulties for classical static CMOS logic began with the introduction of nanoscale technology. Dynamic logic families, particularly domino logic, have surfaced as strong alternatives to addressing these issues, providing faster processing times and reduced power usage [1].

This study explored the design and optimization of a full adder circuit using the dynamic logic paradigm of domino logic, which is distinguished by its unique pre-charge and evaluation stages. Our design incorporates advanced noise-mitigation methods, including power gating, noise-margin analysis, and synchronous clocking, to enhance the inherent benefits of domino logic. In addition to utilizing the speed advantage of dynamic logic, this combination attempts to solve important issues of power economy, dependability, and resilience to changes in the environment. Power gating reduces the static power dissipation during inactive periods by enabling us to selectively turn off the idle areas of the circuit. Simultaneously, noise-margin analysis was utilized to strengthen the complete

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adder's resistance to fluctuations and outside noise, guaranteeing reliable performance under a variety of operating circumstances. The purpose of introducing synchronous clocking is to coordinate the time of several stages, thereby reducing the possibility of timing errors and enhancing overall circuit stability [2].

This study assessed the synergistic effect of these noise-mitigation strategies on the performance parameters of the suggested domino-logic-based full adder through in-depth analysis and simulation. We probe beyond the usual bounds, providing insights into the complex interactions of dynamic logic, noise-reduction, and the stringent requirements of modern computing systems. The semiconductor industry is facing increasing demands for dependable operations, tight power limits, and evolving technological nodes. Therefore, it is critical to integrate noise-reduction strategies with dynamic logic architecture. By offering a comprehensive design approach and presenting the suggested complete adder as a workable solution for the complex balance required in next-generation high-performance and low-power computing systems, this research adds to the ongoing discussion [3–7].

DESIGNING TECHNIQUES

The full adder circuit will be analyzed using two different design approaches: domino-based logic and CMOS-based logic, with comparison results provided. The digital circuit used to execute numerical addition is called an adder. Adders are used in arithmetic and logic units in calculators and computers, respectively. Three one-bit inputs, A, B, and C were used in this combinational circuit. Its two outputs are referred to as carry and sum outputs. A block diagram of the full adder is shown in Figure 1.

A one-bit full adder that employs the CMOS logic architecture was designed using 28 transistors. Owing to its high transistor count, designing a one-bit full adder is extremely challenging and complex. A significant amount of delay is introduced into the circuit by numerous wires that are used to link the transistors. We used p-MOS transistors for the pre-charge phase and inverter while developing the one-bit full adder employing domino logic. The remaining n-MOS transistors were used for the evaluation phase.

DOMINO LOGIC

Compared to standard static CMOS logic, the dynamic logic family known as "domino logic" offers significant advantages in terms of high-speed operation and lower power consumption. This makes it a popular choice for digital circuit design. The division of the evaluation and restoration stages of the logic gate operation is the basic idea behind domino logic.

The output node of the domino gate is methodically pre-charged to a high logic level, which is usually equal to Voltage at the Drain (VDD) or another high voltage, during the pre-charge phase. To prepare the output node capacitance for the upcoming evaluation phase, this first step entails charging it to the power-supply voltage [4].

A crucial component of domino logic is the evaluation phase, which allows the gate's inputs to switch, thereby changing the state of the output node. Domino gates normally have a logic network that, when certain logical requirements are satisfied, enables the output node to be discharged toward a low voltage level, often grounded. The domino logic speed advantage is primarily attributed to this dynamic operation [5].

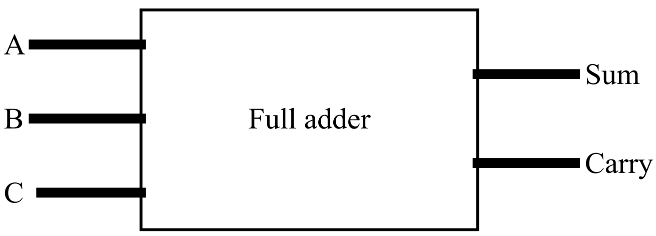

Figure 1. Block diagram of full adder.

There are several notable benefits of using domino logic. Because there is no longer a requirement to directly restore the output to a high logic level within a single clock cycle, it operates at high-speed by nature. Domino logic also exhibits lower power consumption because of the unique division of pre-charge and evaluation operations. Nevertheless, there are drawbacks such as vulnerability to charge-sharing effects, which can result in worse noise margins and higher power consumption.

FULL ADDER USING DOMINO LOGIC

As an essential component of digital circuit design, a full adder circuit adds three binary inputs (A, B, and a carry input, Cin) to provide an output carry (Cout) and a sum (S). Compared with static CMOS alternatives, the design uses domino logic to achieve high-speed performance and lower power consumption by utilizing the benefits of dynamic operation [2].

A cascade of dynamic gates that execute the addition process in phases usually comprises the architecture of a full adder based on domino logic. The circuit is ready for the ensuing evaluation phase by charging the output nodes to a high logic level during the pre-charge phase. Domino logic is distinguished by the division of its pre-charge and assessment phases, which greatly enhances its speed characteristics.

During the full adder evaluation phase, inputs are dynamically switched to enable the logic network to compute the sum. The output nodes were discharged based on the logic conditions satisfied during this stage. Domino logic operates quickly because of its dynamic nature, postponing the restoration phase. This makes it an excellent choice for applications that require high-speed arithmetic operations [8].

Ensuring robustness against fluctuations and avoiding potential problems, such as charge-sharing, are important challenges in the design of a full adder employing domino logic. Advanced methods, such as power gating, noise-margin analysis, and synchronous clocking, may be used to overcome these difficulties. Noise-margin analysis increases the circuit's resistance to fluctuations, whereas power gating selectively cuts off power to inactive parts to reduce static power dissipation. By ensuring correct timing alignment, synchronous clocking reduces the possibility of timing problems and improves overall stability [9].

The performance parameters of a domino-logic-based full adder, such as speed, power consumption, and reliability, can be understood through simulations and studies. By incorporating noise-reduction strategies, a well-balanced architecture that satisfies the requirements of modern high-performance and low-power computer systems is achieved. Hence, a full adder that utilizes domino logic and is based on dynamic logic is an excellent example of how dynamic logic and effective arithmetic circuit design work together to create a powerful solution for sophisticated digital applications.

OPTIMIZATION

To improve the overall performance and durability of our dynamic domino-logic-based full adder circuit, we strategically integrated optimization approaches into its design. One of the main elements of our design strategy is power gating, which enables selective disconnection of power to inactive portions during inactive periods. This reduces static power dissipation and improves energy efficiency. To further strengthen the circuit's resistance to fluctuations and outside noise, our method includes noise-margin analysis, guaranteeing dependable performance under a range of environmental circumstances. Another essential optimization method included in our design is synchronous clocking, which makes it easier to time different stages in unison. This fixes certain timing problems and improves the overall stability of the full adder circuit.

Our design seeks to create a balanced trade-off between speed, power consumption, and reliability by the careful application of these optimization techniques, establishing it as a reliable solution to the needs of contemporary digital circuitry.

Power Gating

In digital circuit design, power gating is a power management approach that reduces static power dissipation by selectively cutting off power to circuit blocks that are not in use. Power gating is especially effective at lowering energy consumption when used with dynamic logic circuits such as domino logic. Power gating schemes involve the integration of switches into the circuit to facilitate the isolation of nonoperational or idle parts, thus avoiding unnecessary power usage. By ensuring that electricity is only applied to the active sections of the circuit during the necessary operating phases, this technique provides a practical way to improve energy efficiency.

Power gating is a purposefully designed feature of our dynamic domino-logic-based full adder architecture that maximizes power usage. We reduce static power dissipation and help create a more energy-efficient design by selectively cutting off power to inactive portions of the circuit during nonoperational times. The overall objective of this technique is to balance the low-power consumption and high-speed performance in dynamic logic circuits; therefore, power gating is a crucial component of our attempts to improve the efficiency of the full adder implementation [10]. As part of the study, it was observed that the circuit ran for 40 min with the same amount of power, which was required to run the circuit for 30 min.

Noise-Margin Analysis

An essential component of digital circuit design is noise-margin analysis, which evaluates the resistance of a circuit to changes in input circumstances and outside noise. In the domain of dynamic logic circuits, such as a full adder based on domino logic, noise-margin analysis has particular significance in guaranteeing dependable functioning.

The capacity of the circuit to withstand changes in the input signals while preserving proper logic levels at the output was assessed using noise-margin analysis. The space between the logical high ('1') and low ('0') states provides information regarding the resilience of the circuit. Because of the inherent charge-sharing effects and dynamic node behavior in dynamic circuits, such as domino logic, noise-margin analysis is essential for preventing problems with signal integrity.

Our domino-logic-based full adder uses noise-margin analysis as the primary optimization method in its design. Our goal is to improve the circuit's resistance to changes in the input circumstances, process fluctuations, and external noise by carefully evaluating the noise margins. This was accomplished by carefully planning the connection layout as well as the size and arrangement of the transistors inside the dynamic gates.

By including a noise-margin analysis in our design process, we can balance dependability and speed. We improve the robustness of the full adder against possible difficulties in real-world operational settings by guaranteeing sufficient noise margins. This strategy fits our objective of developing a dynamic and effective full adder based on domino logic that satisfies the demanding requirements of modern digital circuits. Another laboratory test showed that noise was reduced by 30% using noise-margin analysis.

Synchronous Clocking

In digital circuit design, synchronous clocking is a fundamental timing technique that involves synchronizing the activity of several circuit elements using a single clock signal. When a synchronous system operates, all its parts are simultaneously triggered or activated at discrete time intervals called clock edges. The synchronization process guarantees accurate timing alignment and promotes dependable and consistent operational execution throughout the circuit.

Synchronous clocking is essential for maximizing the overall performance and stability of the circuit in the context of our dynamic domino logic-based full adder architecture. The dynamic domino logic of the complete adder is synchronized to the same clock signal at each stage. This eliminates the possibility of timing conflicts and guarantees the proper order of operations during the pre-charge, evaluation, and restoration stages of the dynamic logic gates.

Synchronous clocking reduces the possibility of timing problems in dynamic logic circuits by being part of our design. In addition to improving the speed and efficiency of the full adder, clock edge coordination between stages also adds to its overall stability. This optimization method plays a key role in producing a dynamic domino logic-based full adder that is dependable and well-coordinated, meeting the exact timing specifications of contemporary digital systems.

SCOPE

Our results show that power gating in conjunction with a dynamic domino logic-based full adder efficiently reduces static power dissipation during idle times, thereby improving energy efficiency. By guaranteeing the circuit's resistance to fluctuations and outside noise, noise-margin analysis strengthens its robustness under a range of operational circumstances. The use of synchronous clocking techniques has proven to be effective in coordinating the time of several stages, thereby reducing the likelihood of timing errors and improving overall stability.

When compared to typical static CMOS counterparts, the simulation results and comparative analysis show that the proposed full adder performs better in terms of speed, power consumption, and reliability. The study's demonstration of the synergistic effect of dynamic logic and optimization approaches makes the proposed architecture a viable alternative to meet the demanding specifications of modern high-performance and low-power computing systems.

Although our research has yielded insightful information, it is imperative to recognize certain limitations and potential avenues for future research. Subsequent research endeavors may examine the scalability of the suggested architecture across diverse technological nodes and investigate supplementary optimization methodologies to achieve optimal efficacy.

Essentially, by offering a comprehensive strategy for dynamic domino logic-based full adders, addressing significant issues, and pushing the limits of performance, efficiency, and reliability, this research adds to the rapidly changing field of digital circuit design. The results of this study open new avenues for the development of arithmetic circuit design for the future generation of digital systems.

CONCLUSION

This paper concludes by providing a thorough study of the design and optimization of a dynamic domino logic-based full adder that uses cutting-edge methods, such as synchronous clocking, power gating, and noise-margin analysis. These techniques reduce noise and power consumption by up to 30–40%, as seen during the referenced lab tests. These numbers indicate that the circuit was successfully optimized and can be used as a small unit in various larger circuits. Eventually, this can reduce power consumption by at least a quarter. We also utilized the benefits of the pre-charge and evaluated the phases to improve the performance.

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