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A Study on Polymer-Based FinFET Applications and Logic Circuit Implementation with FinFET

Saptarshi Chakraborty[1], Arpita Ghosh[2,*]

Abstract

Nano devices play a crucial role in the semiconductor industry and can work as the solution for problems like scaling of MOSFET. The FinFET can serve as the substitute of bulk CMOS in nanoscale. It mainly consists of two gate terminals which can be either shorted or kept independent. The shorted gate (SG-FinFET) configuration provides higher Ion and Ioff whereas the Independent Gate (IG-FinFET) configuration reduces the transistor count and also reduces the leakage current. Unique FinFET can be developed by proper choice of its parameters (number of fins, dimensions etc.), materials (for gate, substrate). Flexible electronics moreover has some other requirements that can be fulfilled by the polymer-based FinFET. Polymer can be used in FinFET design in two ways- as substrate and as gate material. This work elaborates the different polymer-based FinFET and their applications based on their characteristics. This paper also includes various FinFET(SG-FinFET and IG-FinFET) based basic logic circuit design such as NAND,NOR,2:1MUX,decoder ,simple Boolean simulated in LTSpice.

Keywords: FinFET, MOSFET, flexible electronics, polymer, substrate, logic circuit, nanodevice, scaling

INTRODUCTION

In standard MOSFET transistor the problem of scaling [1-3]. is increasing on a daily basis. The MOSFET performance gets effected by the severely due to the scaling down of the channel length in nanometer domain. To amend such problems nanodevice can be a good option. For that reason, the demand of such nanodevices has become much higher. There are several such nanodevices such as FinFETs [4-17], high electron mobility transistors [18-20], hetero bipolar transistors [21-23], resonant tunneling diodes [24-26], Single Electron Transistors[27-29] etc. Among these FinFETs are great replacements for bulk MOSFET in the nanoscale domain and it can be designed and fabricated at nanolevel. In 2001 the term FinFET i.e Fin Field Effect Transistor was coined by University of California from the group of scientists, Tsu-Jae King-liu, Chenning Hu and Jeffrey Bokor for presenting a non-planar, double-gate transistor designed on an SOI substrate. The channel of FinFET from source to drain is the main difference between FinFET and MOSFET. The channel width determines the drive strength of planner MOSFET but in FinFET channel width can be increased by incorporating more number of Fins. Due to fast switching, higher drive current is observed in FinFET which is greater than MOSFET. The leakage current is a normal phenomenon in switching device due to leakage voltage. As FinFET's leakage current is low so its power consumption cannot be more than MOSFET. The gate length of the FinFET has a notable impact on lowering leakage current which causes leakage power. The gate length is reasonably longer

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because it is covered by drain to source channel, so now when the gate is non-energized there will be no leakage current. FinFETs can be used as a substitute of the MOSFET in different analog and digital circuit applications, switching device in mechatronics [30], RF applications [31], memory design[32-36] etc.Different analogue[37] and digital logic circuit implementation using FinFET[38-41] is reported . Moreover, to fulfil the demand of flexible electronics different polymer materials are used as the substrate material. But the graphene due to its 0 bandgap and semi-metallic characteristic restricts the clear cut on/off operation. It makes them useful for the analogue RF applications. This present study includes such two-stage FinFET based OpAmp design for RF applications. Again polymer-gate based FinFET are used as multiple gas sensors. The study includes these applications of polymer-based FinFETs. Here in this study some of the logic circuit implementation with SG-FinFET as well as IG-FinFET is presented along with the simulated waveforms.

LITERATURE SURVEY

In 1989 the FinFET transistor was introduced as "Depleted Lean-channel Transistor" or "DELTA"[42] transistor. Hisamoto, T. Kaga, Y. Kawamoto and E. Takeda first fabricated Fin-FET in Japan by Hitachi Central Research Laboratory .Sai et.al[39] in their work used 22nm technology for FinFET BSIM-CMG models and simulated using in Cadence Virtuoso tool. The simulated circuit performances were compared with 45nm based circuits in terms of their power dissipation and delay. The observation was the reduced power consumption in case of 22nm FinFET based circuit rather than the 45nm CMOS technology. Kajal and Kumar[43] in their work presented different FinFET circuits such as inverter, OAI,AOI and simulated with cadence virtuoso tool containing ASAP7 PDK and PTM models. Different leakage reducing techniques such as ONOFIC (ON/OFF logic IC), LCNT(Leakage Control NMOS Transistor) and LECTOR have been used in their work. In 2020 Madhavi and Tripathi[44] reviewed FinFET based on different materials such as dual KK-structure,InGaAs-on-Insulator, double Gate based n-FinFET using hafnium oxide, SOI-FinFETs, MuGFET (Multi gate), deeply Scaled CMOS, FinFET, selective epitaxial Si Growth in FinFET and Atomic Layer Deposition (ALD) .For better control in channel carrier transport multi-independent gate controlled FinFET technology is used if critical dimensions are scaled down to nano meter scale. Compared to traditional FinFET ,this multi independent gate can provide a variety of different mode to meet different needs of high speed,lower power, and other potential applications.To avoid barriers like sub-threshold leakage,short channel effects researchers has come with a new nano device transistor known as FinFET.Sevilla et. al.[45][46] in 2014 proposed a three dimensional non-planar-FinFET. It was based on SOP(Silicon on polymer)in sub 20nm range for the computational purpose inspired by brain structure. Suman et. al. in 2022[47] proposed 2-stage OP-Amp with polymer-based FinFET (trigate) in Nanoscale. Mehrdad and Ahangari in 2022 [48] proposed CPG(conducting-polymer-gate) FinFET based multiple gas (Methanol,Iso-Propanol ,Chloroform)sensor.

Further subsequent headings

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BASIC STRUCTURE OF FINFET

The basic structure [49-51] of a singleFinFET device is very similar to FET(Field Effect Transistor).In FET device the structure the gate is above the channel whereas flow of leakage current flows from source to drain even if the gate is off. In FinFET it consist of one source , one drain and a gate attached to it shown in Figure 1-2. This gate which is attached to the drain controls the flow of current. FinFET consists of Fin. Fin is the channel between source and drain. It is like a three dimensional bar on the top of the silicon substrate.

Around the channel gate electrode is wrapped because of that it is observed that there are several gate electrode around the FinFET. These gate electrodes are capable of reducing leakage effects and enhanced drive current.

Mainly there are two types of FinFET Shorted-Gate(SG)[52]FinFET and Independent Gate(IG)[53-54]FinFET. FinFET having short-circuited front and back gates with one terminal is known as shorted

gate FinFET(with three terminals -Source,drain,gate) shown in figure 3 (a) and (b). In this gate threshold voltage cannot be controlled externally. Independent Gate (four terminal) is frequently used in circuit designing technology because it has two separate gates. Each gate can be made function independently.

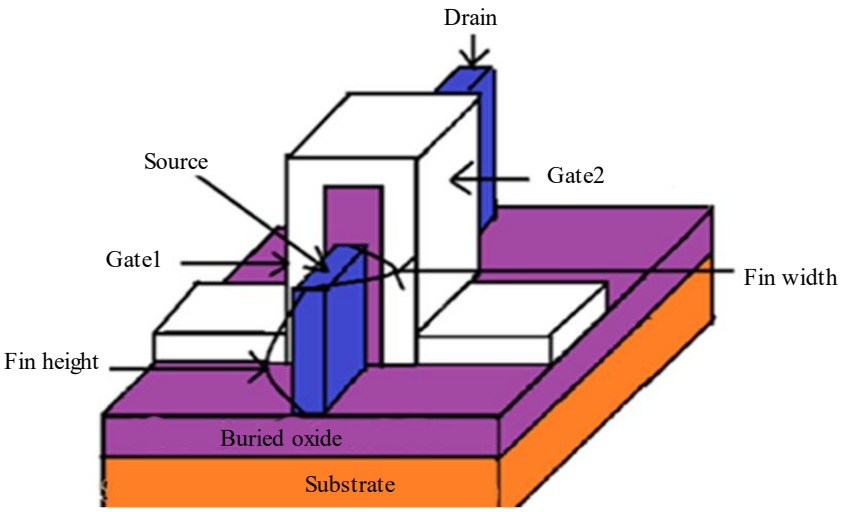


Figure 1. Basic Structure of FinFET

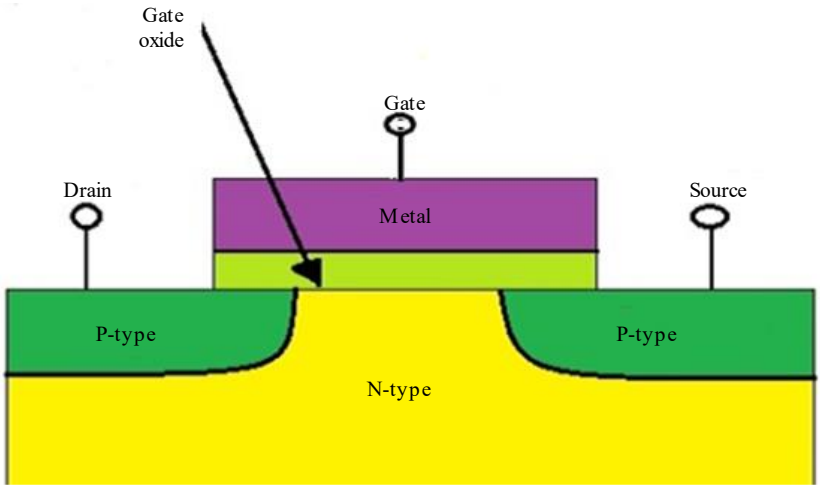


Figure 2. Basic Structure of MOSFET.

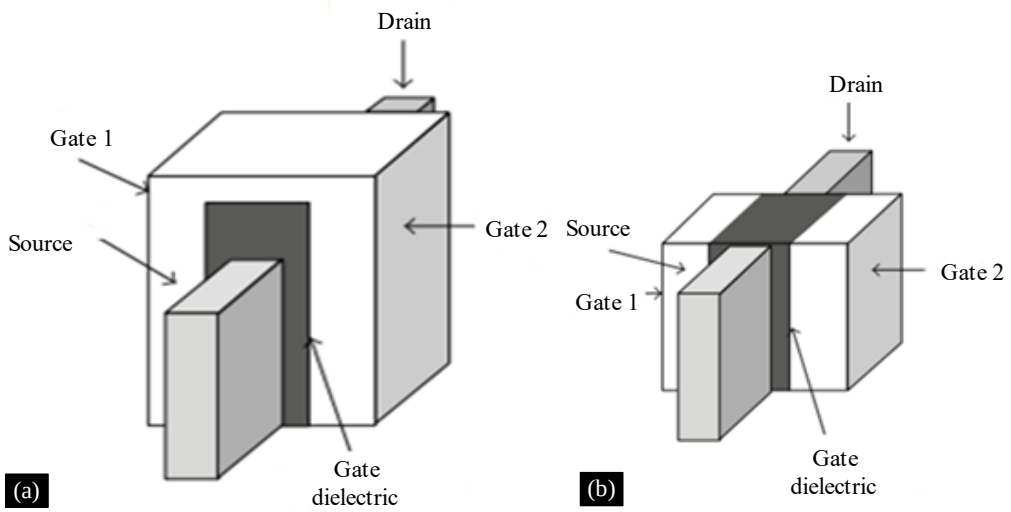


Figure 3. Structure of (a)Shorted Gate(SG) FinFET,(b)Independent gate (IG) FinFET

Polymer-based FinFET structures and applications

In two ways polymer is used for FinFET design. First as a substrate material through which FinFET can get the flexibility and second one as the gate material. Polymer substrate based FinFET makes it suitable for mainly the analogue application as it lacks of clearly identifiable on/off switching characteristics. In case of the conducting gate material polymer FinFET can be operated as a sensing device for multiple gases.

Though most of the electronics are Silicon based but for the wearable, computational and implantable electronics it's brittleness and low flexibility becomes the main drawback. On the other hand the polymer based electronics used for display and sensors suffer from thermal instability and inherent low carrier mobility. Sevilla et. al.[45] in their work demonstrated a flexible nano-dimensional polymer substrate based FinFET for which the electrical characterization was compared with the conventional rigid-FinFET (bulk-SOI substrate based traditional FinFET). They observed no performance degradation for the polymer based FinFET for different up and down direction bending radius compared to the rigid one. They used back etch method instead of back grinding method to achieve flexible (bending radius=0.5mm) through substrate thining process. Sevilla et. al.[46] reported a flexible FinFET three-dimensional non-planar FinFET based SOP(silicon-on-polymer) in sub 20nm range for the computational purpose inspired by brain likestructure. They proposed low-cost compact design of brain-structure for computation with plastic/polymer substrate and organic materials for fabricating different sensors, display supporting flexible electronics. The existing flexible displays suffer from thermal instability. Whereas these can be overcome with SWCNT(single-walled carbon nanotubes) and grapheme with atomic crystal structure. But integration of SWCNT is not feasible with silicon semiconductor processing. On the other hand grapheme due to its zero band-gap semi-metallic characteristics is not suitable for digital application as on/off is not clearly distinguishable. Only applicable for RF applications. J.A. Roger et. al[55] proposed combination of electrical and mechanical property of Silicon with polymer-substrate flexibility. They proposed FinFET high k/metal gate stacks (Figure4)

Suman et. al.[47] in their work proposed a polymer-based trigate FinFET where Electron integration (EI) related to underlap FinFET is also another important factor as it makes the FinFET less immune to parametric fluctuations and variability of device. They demonstrated a Common source polymer based amplifier design in 2 stage OP-Amp shown in figure 5(a) below.For designing a simple, low-cost 3D FinFET model by solving 3 dimensional poisson equation a combination of polymer is chosen as substrate and organic material. Trigate nanosize FinFET with polymer substrate was reported for OpAmp circuit design. Their design consisted of a differential amplifier, CS amplifier, compensation and biasing circuit shown in figure 5 (b).Here the polymer is mainly used as the substrate material for the FinFET.

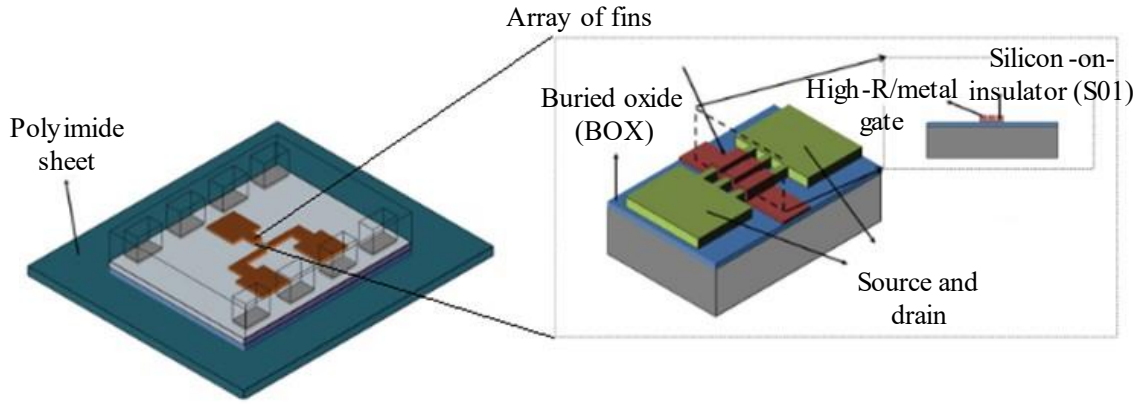


Figure 4. Structure of FinFET with polyimide substrate Ref [46].

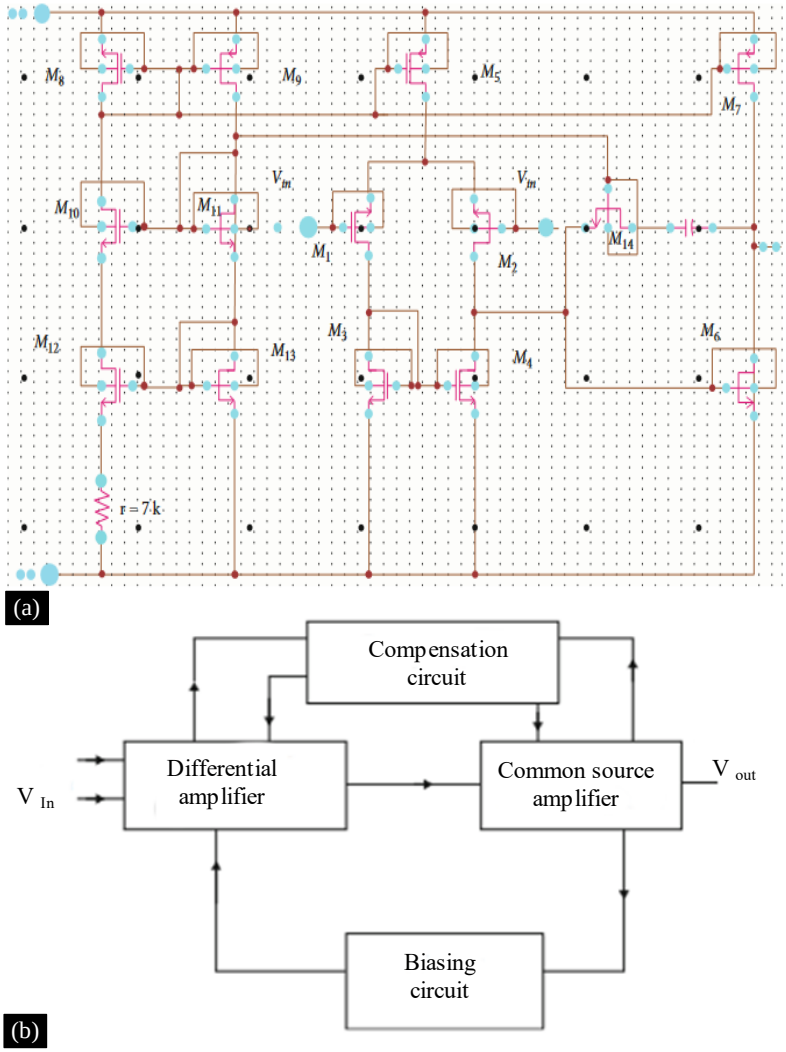


Figure5. Two Stage (a)Differential amplifier design (b) OpAmp Design with FinFET Ref [47].

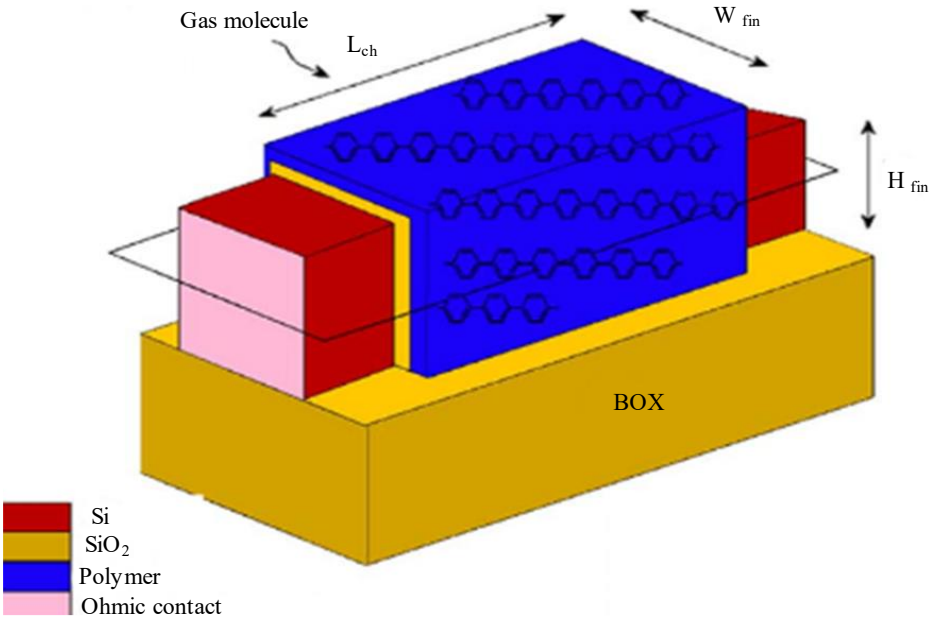


Figure 6. 3D view of multiple gas sensor with CPG FinFET from ref [47].

Mehrdad and Ahangari [48]. proposed a 3D structure of low-power conducting-gate-polymer(CPG) based multiple gas(Methanol,Iso-Propanol ,Chloroform) sensor using junctionless FinFET shown in Figure 6. The sensitivity and responsivity of the sensor is measured with the variation in off current and threshold voltage after and before gas absorption. For this a conducting (poly(p-phenylene)) polymer gate based FinFET gas sensor where gate material work function modulation upon gas absorption is the main concept . The gate wrapped around the channel gives high surface area for gas absorption. The device performance was assessed with the drift-diffusion model, band-gap narrowing model, mobility model and quantum confinement model. The main requirement for this proposed structure is the higher channel doping for efficient operation. The doping density in off-state current is dominant in comparison with gate work function which can reduce responsivity of sensor. Another important concern is the temperature variation.

LOGIC GATE IMPLEMENTATIONS WITH FINFET

A single FinFET structure can be designed by connecting to CMOS adjacently. NOT gate is designed by connecting two CMOS adjacently that make a pull up network(PUN) and another set of CMOS makes the pull down network(PDN). These two set of CMOS structures i.e two FinFET are connected in series which makes a NOT gate. The PUN is connected to the Vdd which is 1.2v and PDN is connected to the ground. The out Y is coming out from the center in between the PUN and PDN. The length and breadth of the both PMOS and NMOS is 130nm.Here the initial voltage (V initial) [v]=0,input voltage which is Vhigh(Von[v])=1.2v,time delay[Tdelay(S)]=0s, Rising Time(Trise)=500p;Time delay(Tdelay(s))=0s,Rising Time(Trise)=500p;Falling Time(Tfall)=500p,Ton=10n,Tperiod[time period]=20n. Transiesnt time=100n. Lib function command .include ibm130.lib is used to design the circuit using the specified technology. Input A is connected to gate. The output Y is connected to the junction of PUN and PDN.

Basic Logic Gate Implementation Using Finfet

NOT gate implementation

The NOT gate or inverter is a very important part of any digital logic circuit. Here the NOT gate is implemented using FinFET technology. The input is denoted with a and the output with y. The input and the output are complementary in nature. For simulation purpose LTspice[56] platform version XVII has been used. The implemented circuit is shown in Figure 7. pFinFET is implemented by connecting two pMOS parallelly and in the same way the nFinFET is implemented by connecting the two nMOS

in parallel fashion. The drain terminals and the source terminals of the two MOSFETs(for pFinFET 2 pMOS and for nFinFET 2 nMOS)are shorted and same input is applied to the gate terminals. Here two parallel connected pMOS(M1,M2) are used to form the pFinFET and two nMOS(M3,M4) are connected in parallel to form the nFinFET.For, a=0 M1 and M2 are on due to which the output is pulled up to 1.For a=1, due to the functioning of the pull down network the output is dragged down to 0. Two voltage sources are used here V1 and V2. V1 for DC power supply voltage which is 1.2V and V2 is the input(a) pulse waveform with logic 1 (1.2V) and logic 0(0V). The model file used for the MOSFETs is "ibm130.lib". The transient analysis for duration 100nS has been carried out in the LTSpice XVII.

The functioning of the circuit can be justified with the circuit simulation results shown in the Fig.8., that supports the truth table (Table 1). Fig 8(a) , (b) represents the simulated waveform of input , output of the FinFET based NOT gate respectively with Logic 1 at 1.2V , Logic 0 at 0V and frequency 50MHz The power consumption and delay of this inverter is 10.7699nW and 20.01ns respectively.

NAND gate implementation with FinFET

As per the truth table of two input NAND gate the only possibility of output y_NAND being high is when both the inputs (a and b) are high. The implementation of the same with SG-FinFET and IG-FinFET is elaborated.

a. Two input NAND SG/IG FinFET

The circuit implementation with SG FinFET is shown in figure 9(a). Here total 4 numbers of pMOS as well as nMOS are required to form the PUN and PDN. pFinFET1, pFinFET2 are comprised of M1,M2 and M3,M4 respectively. Similarly nFiFET1,nFinFET2 is comprised of M5,M6 and M7,M8 respectively. In this IG-FinFET based design (shown in Figure 9(b)) pFinFET is comprised of M1,M2.The nFinFET1,nFinFET2 is comprised of M3,M4 and M5,M6 respectively.

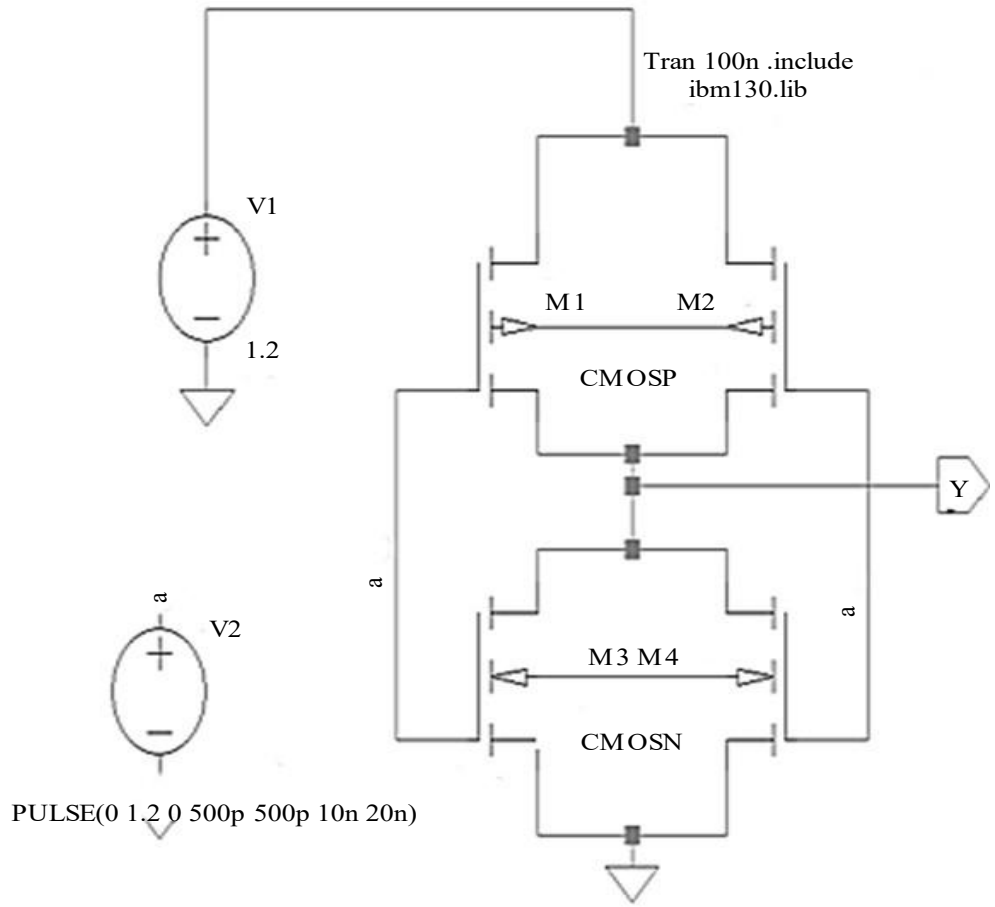


Figure 7. Circuit diagram of FinFET based NOT gate.

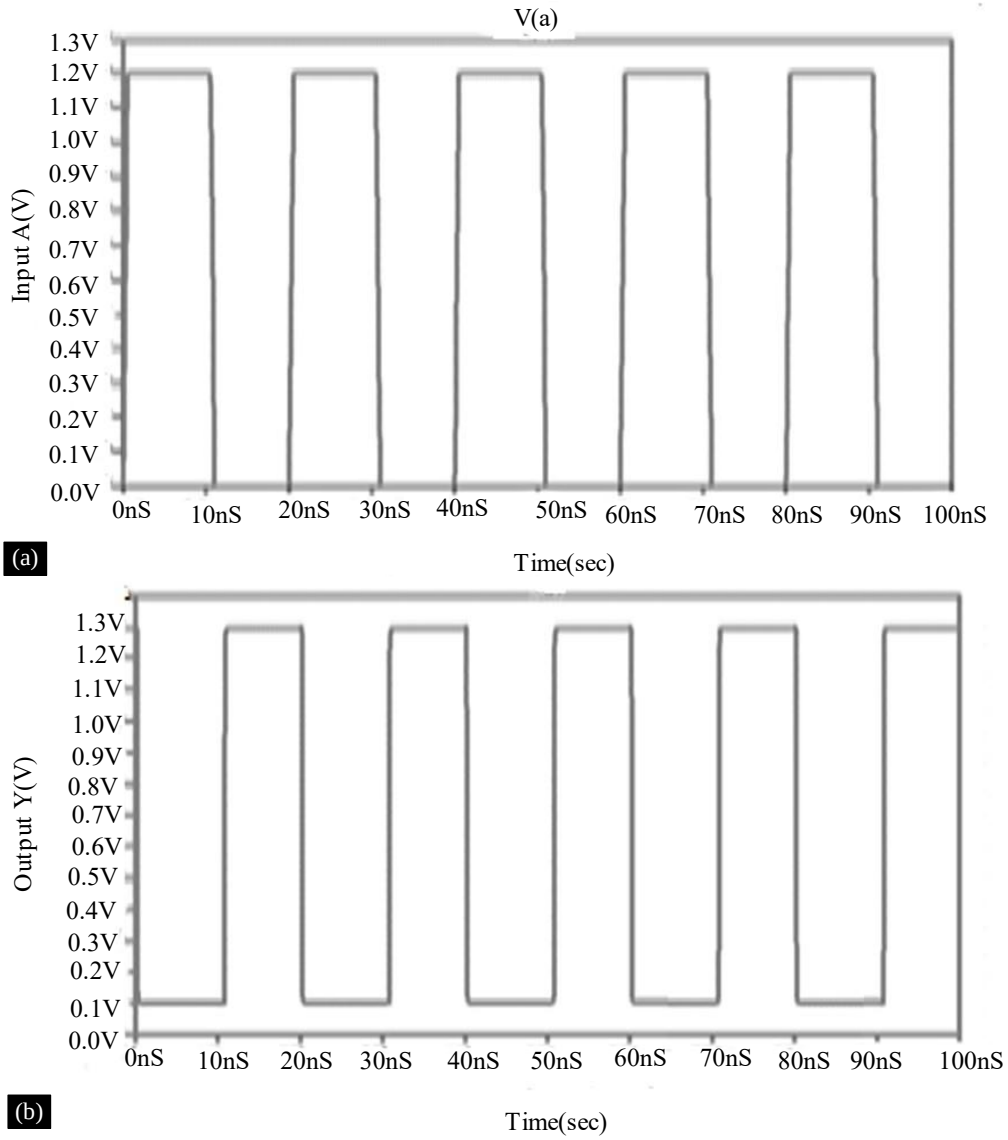
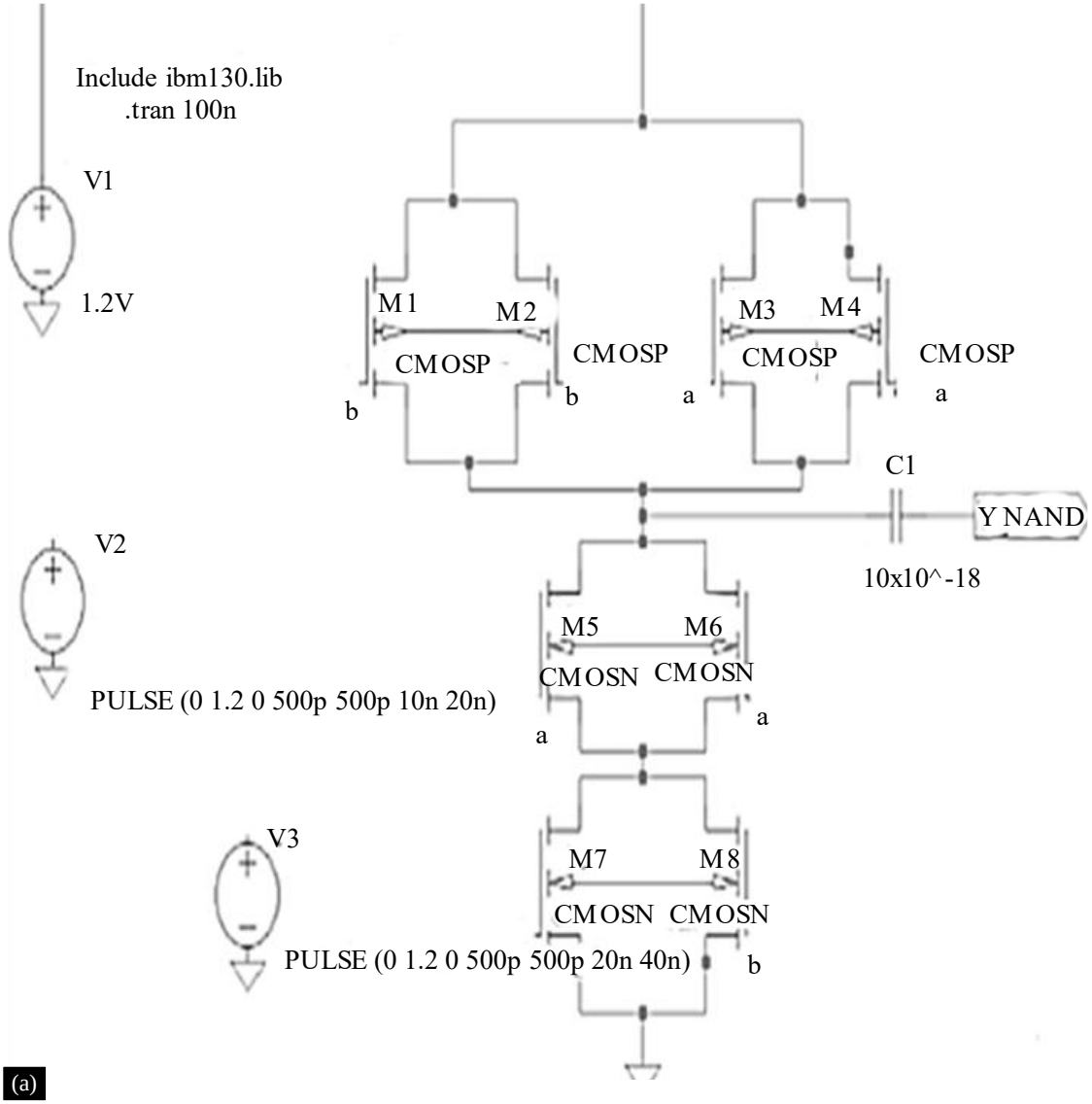
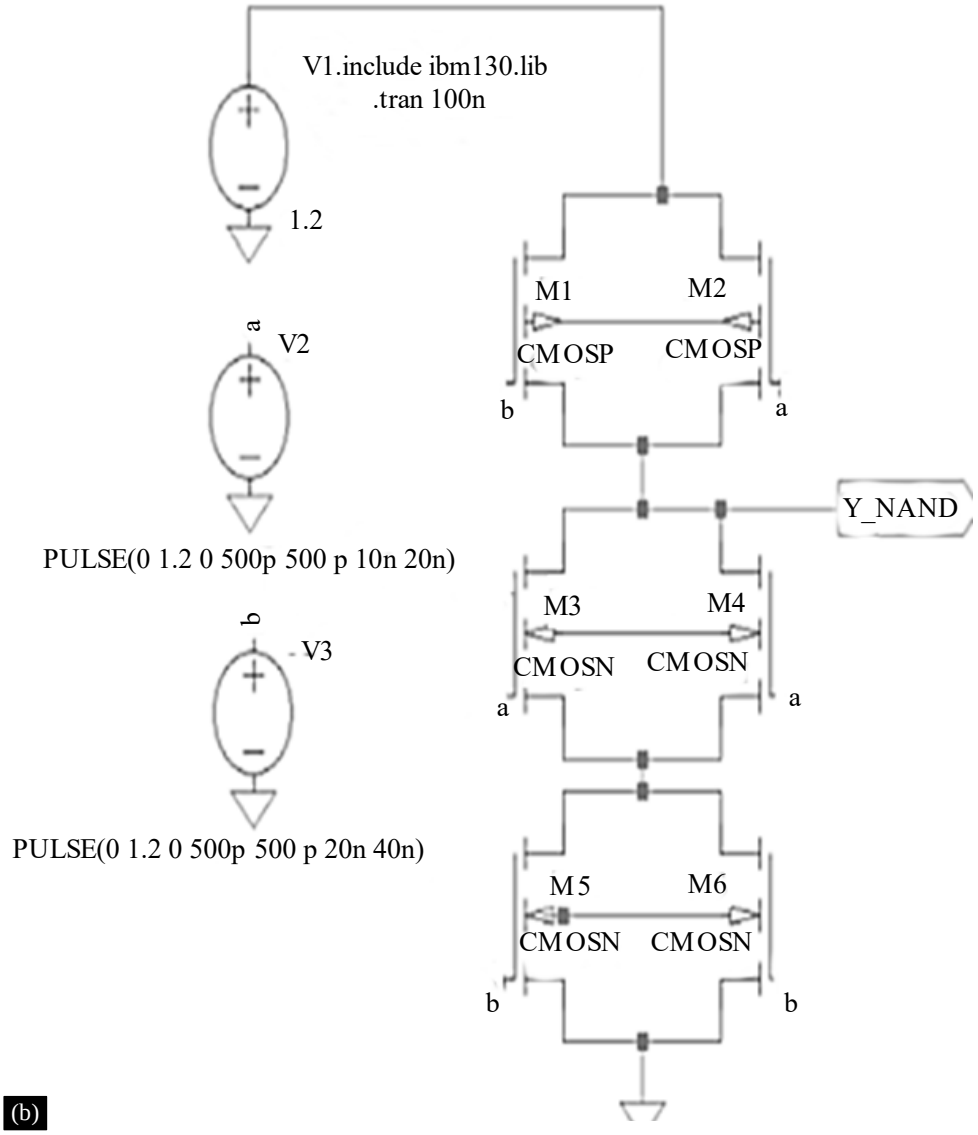


Figure 8. (a)Input a,(b) Output y of FinFET based NOT Gate.

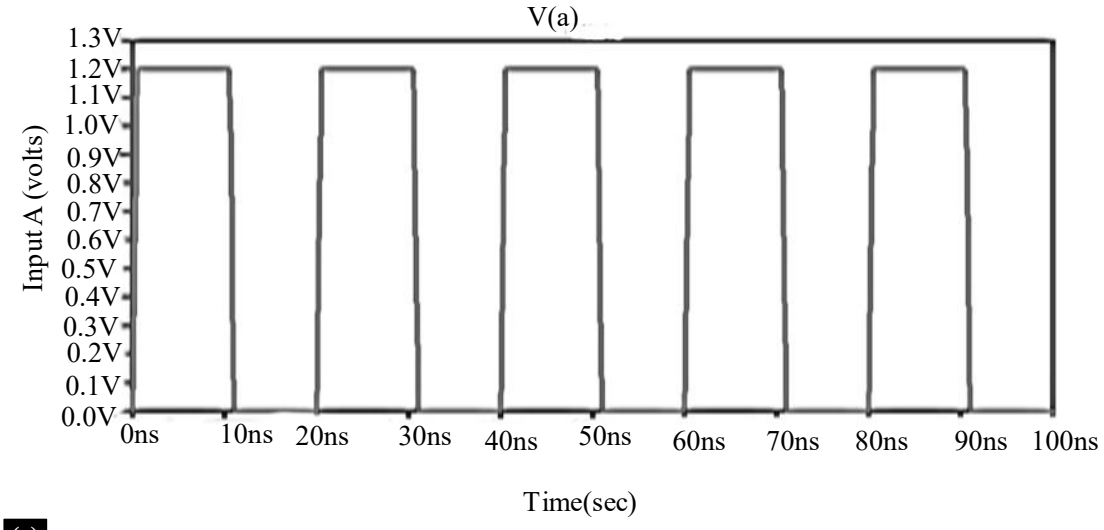


(a)



(b)

Figure 9. 2 input NAND Gate (a)SG-FinFET based (b)IG-FinFET based.



(a)

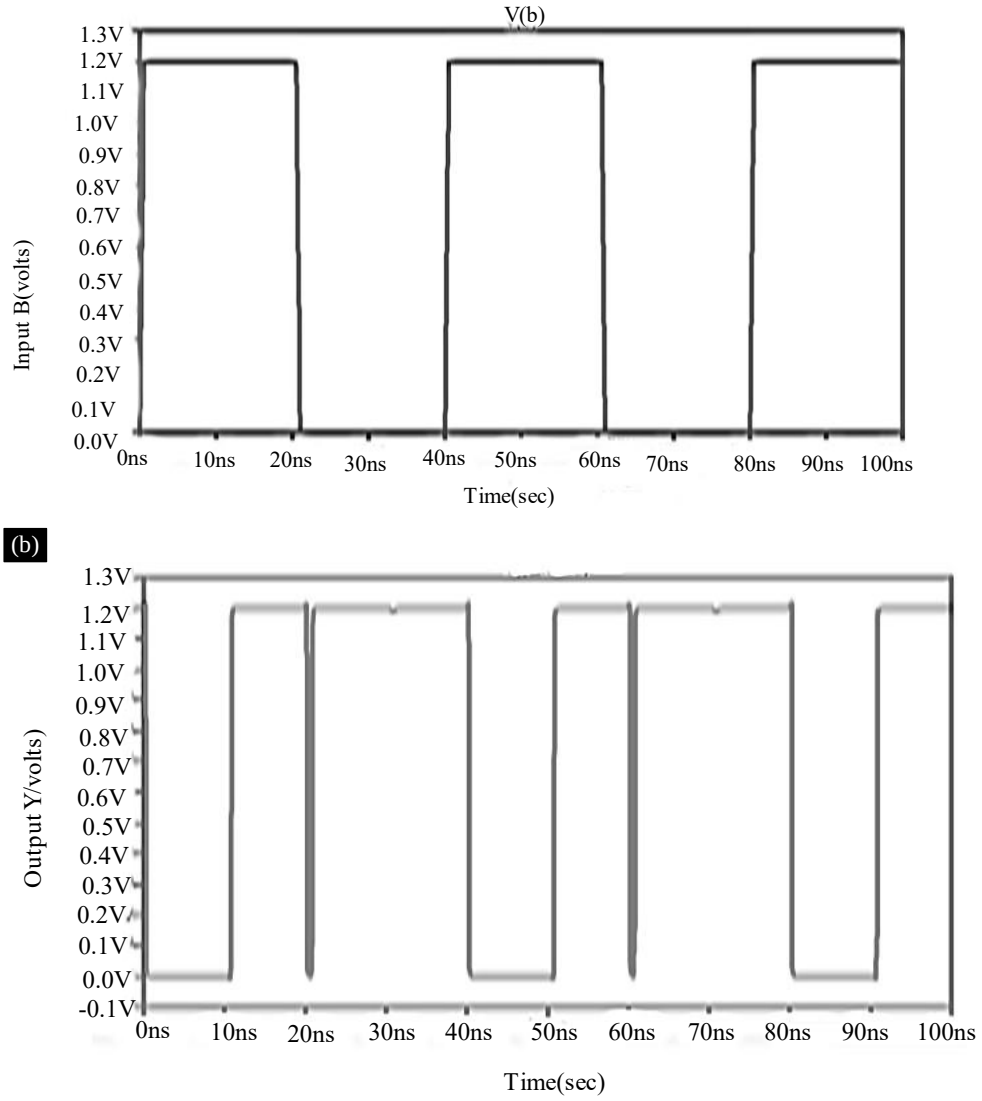


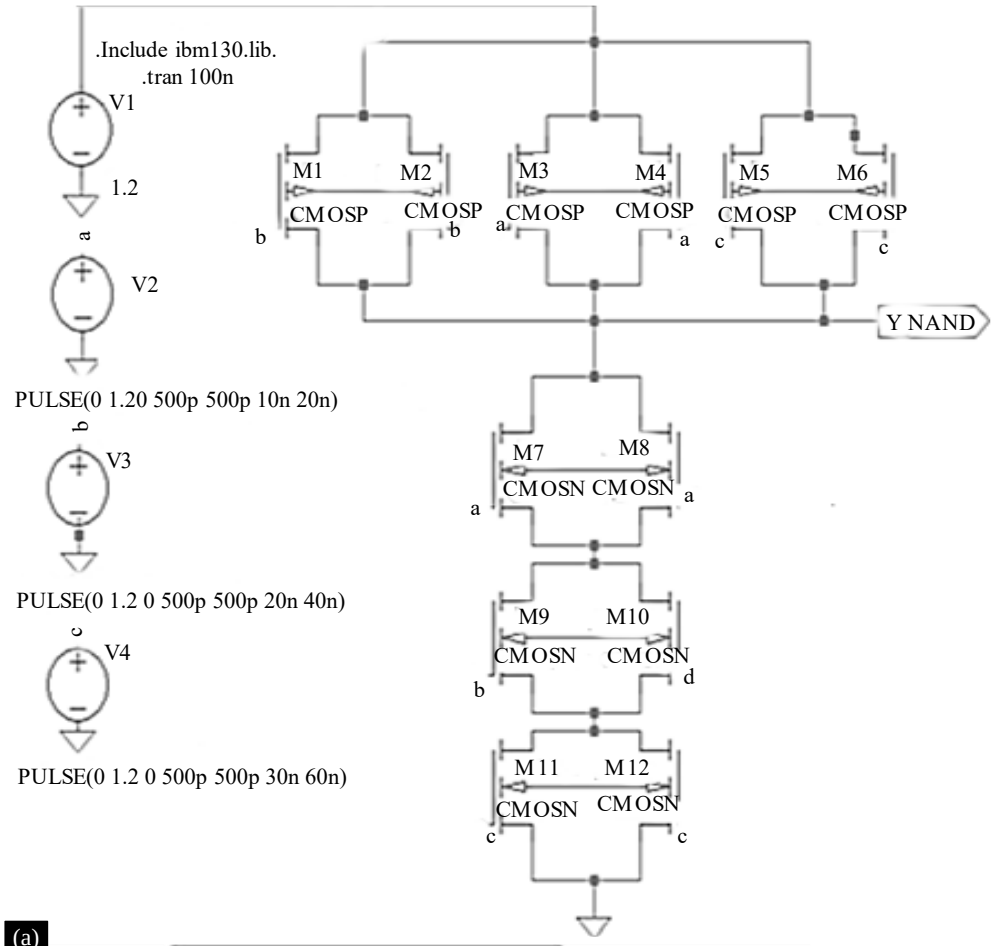
Figure 10. (a) Simulated waveform of a(input) ,(b) b (input) (c) y (output) of SG-FinFET based 2input NAND Gate.

Three voltage sources V1,V2,V3 are used among which V1 is 1.2V DC power supply, V2 and V3 are pulse waveforms for input a,b respectively. For Input a frequency is 50MHz and for b the frequency is kept at 25MHz. The input output waveforms in support of the proper functioning is shown in figure 10 (a),(b) and (c) respectively. The logical output satisfies the truth table shown in Table 2.

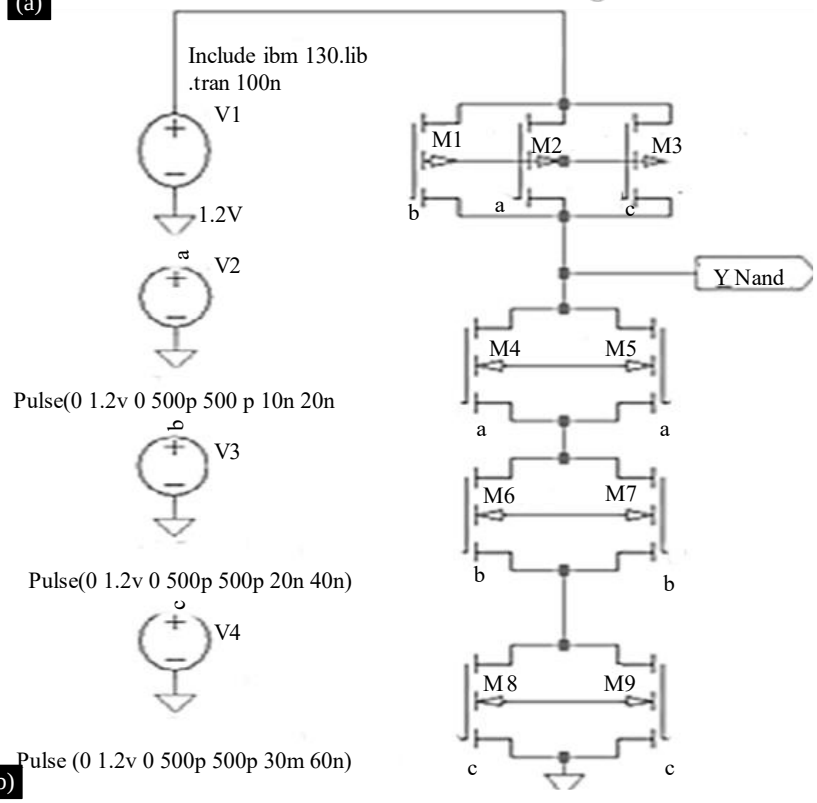
b. B.3 I/P NAND GATE SG/IG FinFET

In a similar way the three input SG and IG FinFET based NAND gate is implemented and simulated.

In SG-FinFET based design pull-up network(PUN) is designed with 3 pFinFET (3 pair of MOS M1,M2;M3,M4;and M5,M6).The pull-down network(PDN) is formed with 3 nFinFET (3 pair of nMOS M7, M8; M9, M10; M11, M12), Four voltage sources are used V1 for 1.2 V dc power supply and rest are for input a,b,c(Figure 11(a)). The IG-FinFET based circuit design is depicted in Figure 11(b), where PUN is formed with M1,M2,M3 and PDN is formed with M4,M5;M6,M7;M8,M9. The simulated waveforms in support of logical functioning is shown in Figure 12(a),(b),(c) and (d). Frequency of the input a,b,c is 50MHz,25MHz,16.67MHz respectively.



(a)



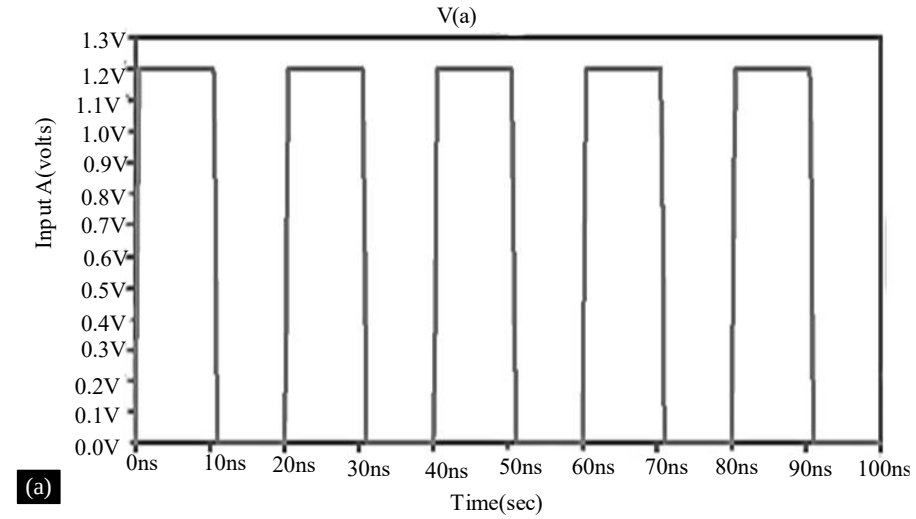
(b)

Figure 11. 3 input NAND Gate (a)SG-FinFET based (b) IG-FinFET based.

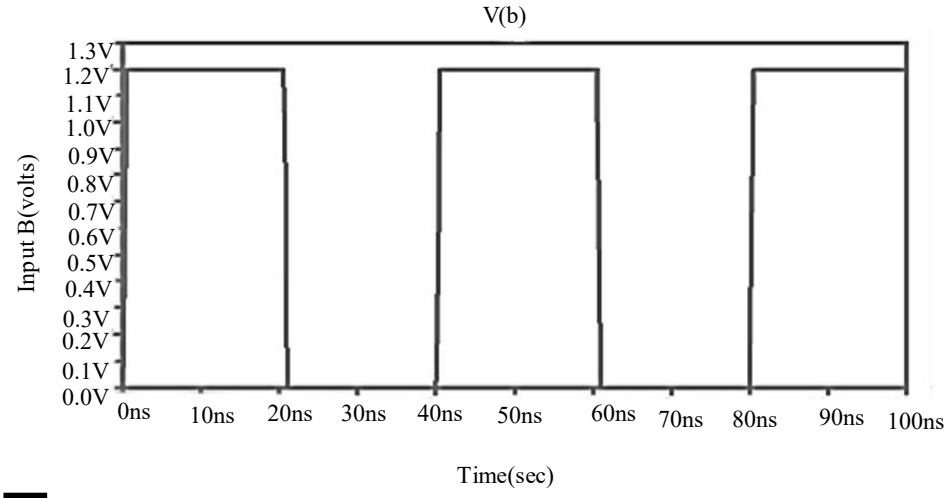
NOR GATE Implementation

A.2 input NOR with SG-FinFET

Figure 13(a) and (b) shows the SG-FinFET and IG-FinFET based two input NOR gate implementation. A ,B and Y are the inputs and the output waveforms respectively(depicted in figure 14(a),(b),(c)) maintaining the proper logical relation as per their truth table (where y_NOR is only high when both inputs(a and b) are low).



(a)



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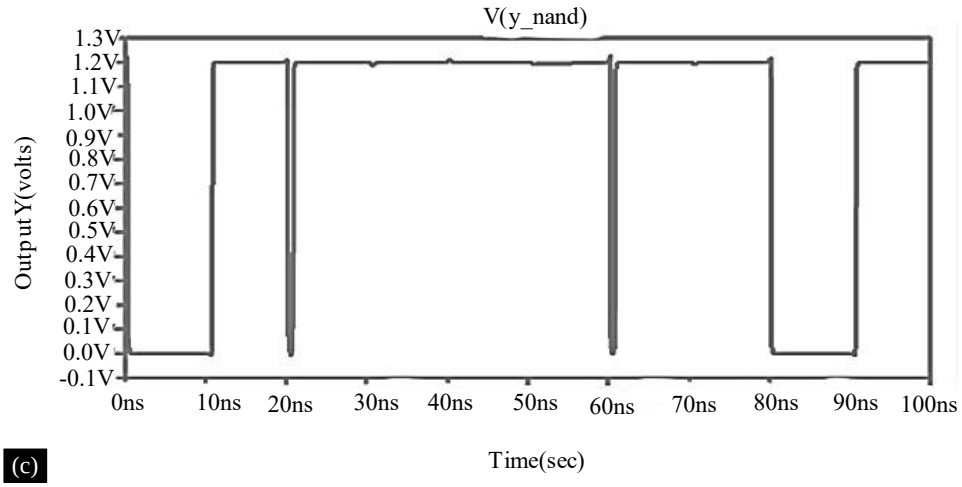
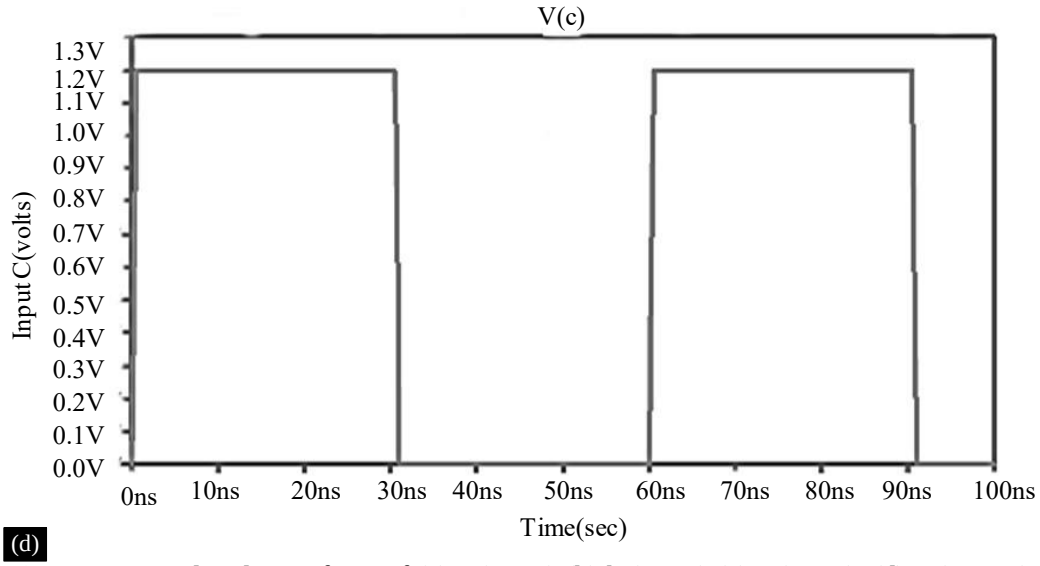


(c)

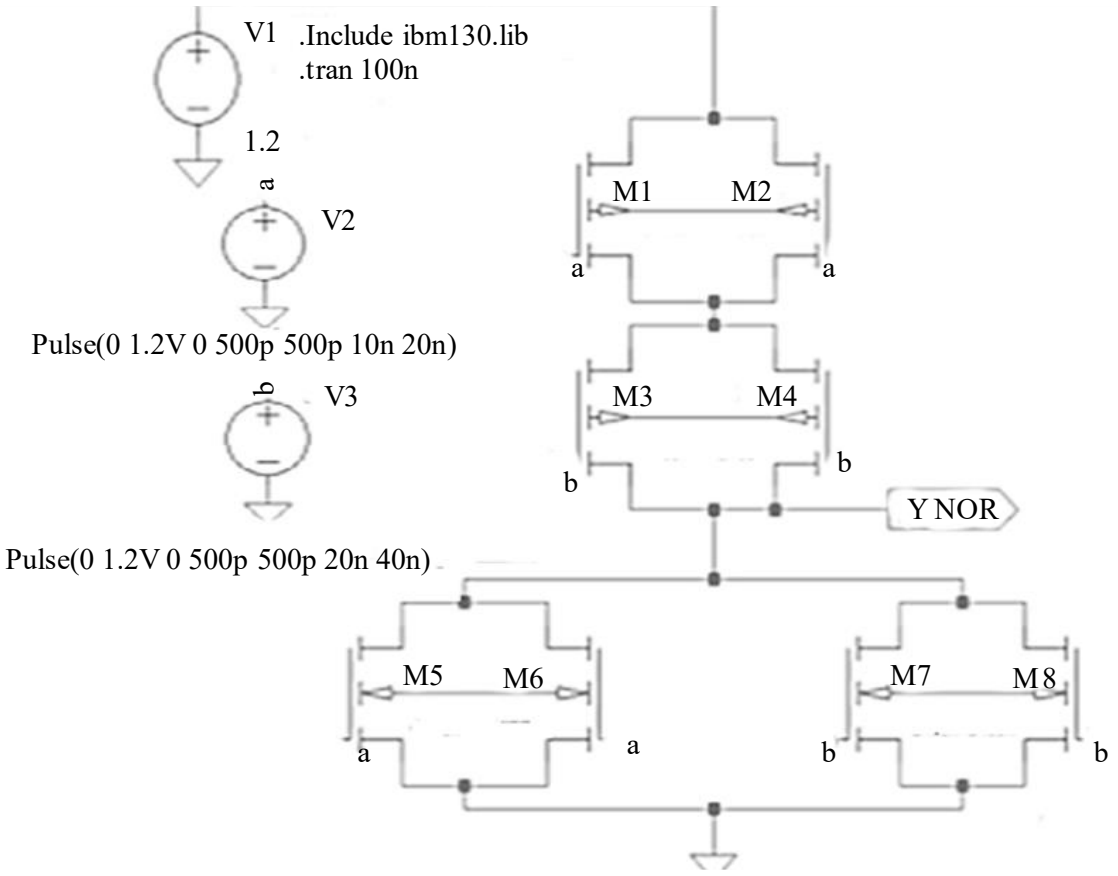


(d)

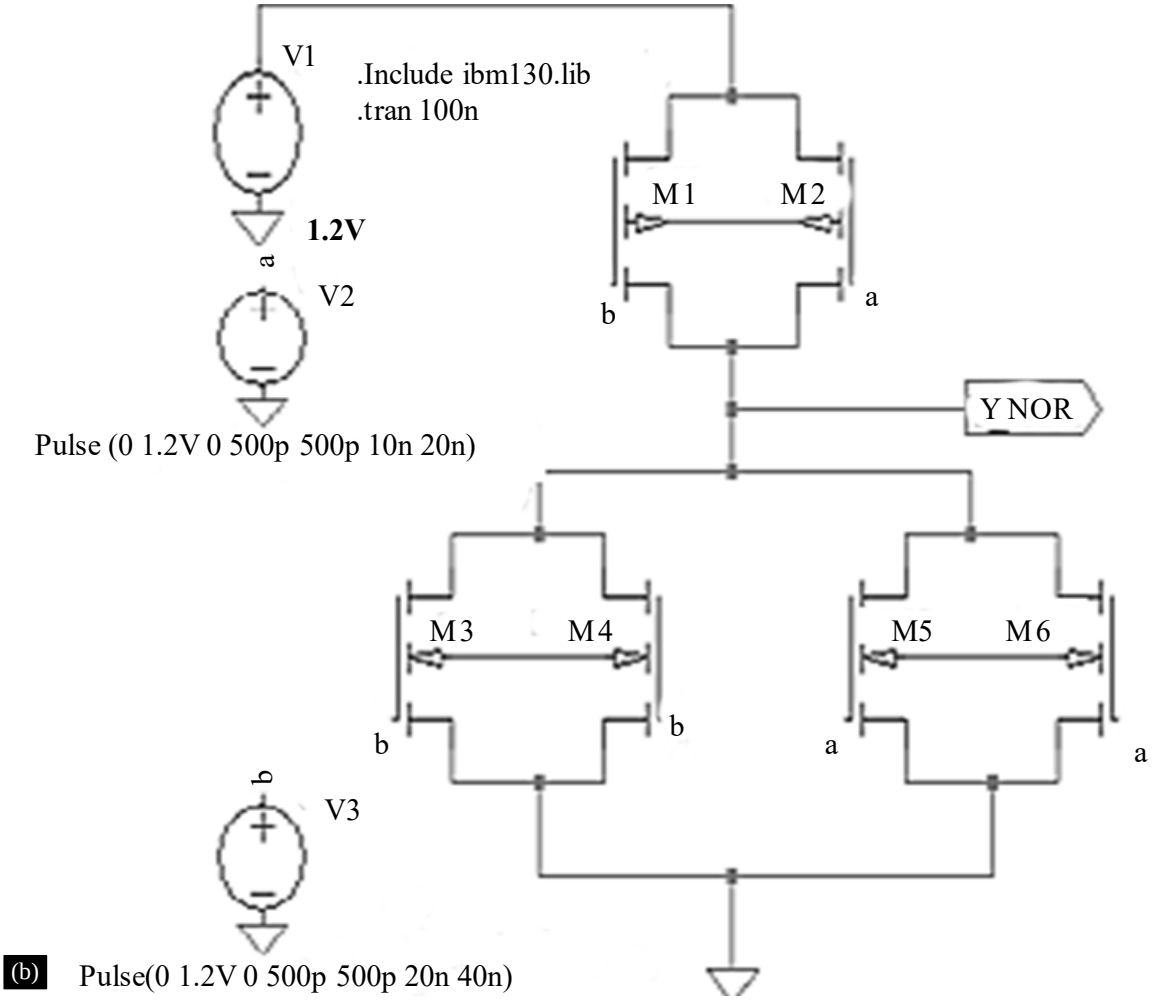
Figure12. Simulated waveform of (a) a (input) (b) b (input),(c) c (input) ,(d) y (output) of SG-FinFET based 3 input NAND Gate.

INPUT NOR WITH SG-FINFET

The circuit implementation of SG and IG FinFETbased three input NOR gate is depicted in Figure 15(a) and (b) respectively. Simulated output of the both is shown in Figure 16 with proper logic functioning as per their logical relation (output Z is high only all the inputs are low).

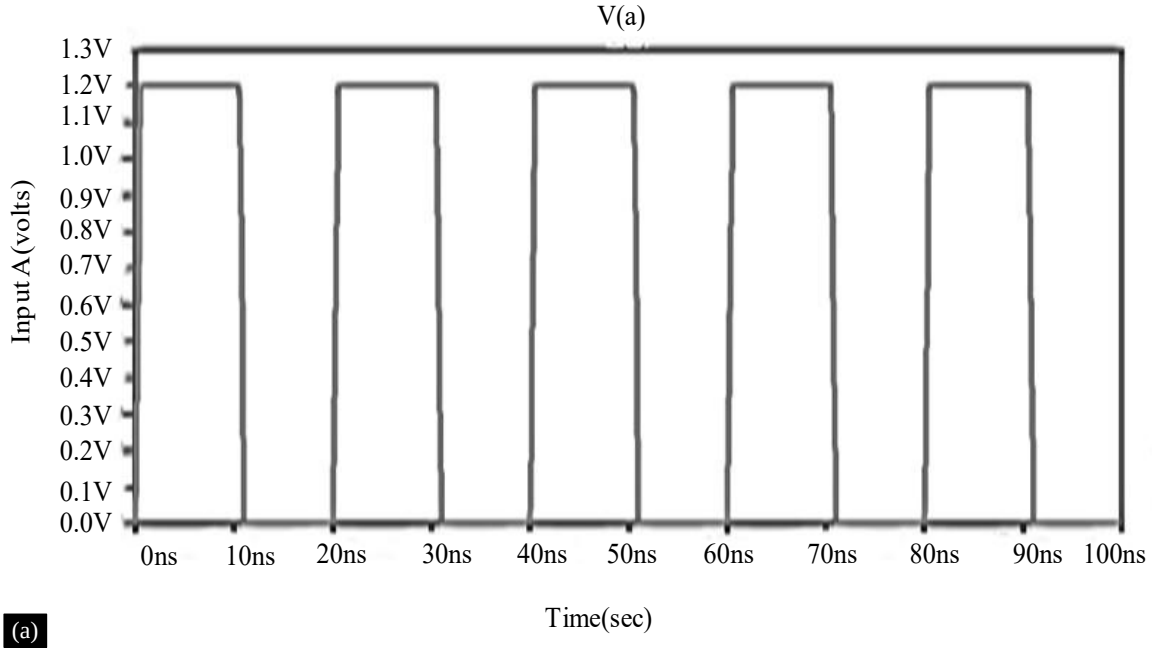


(a)

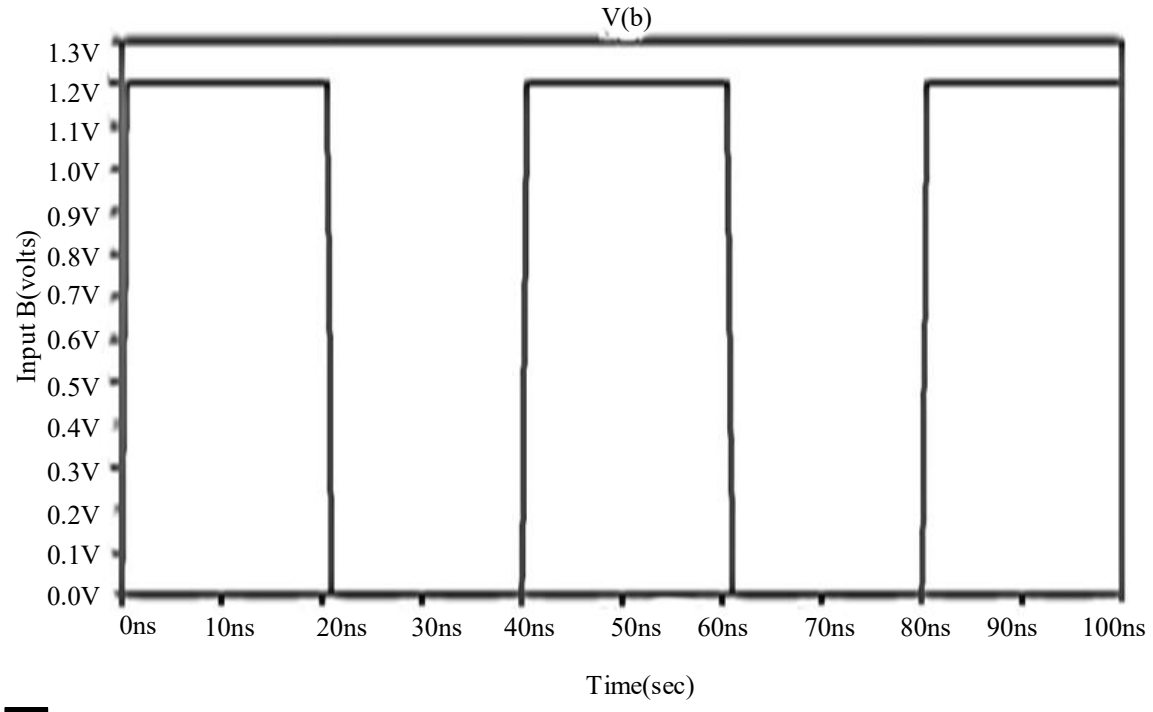


(b)

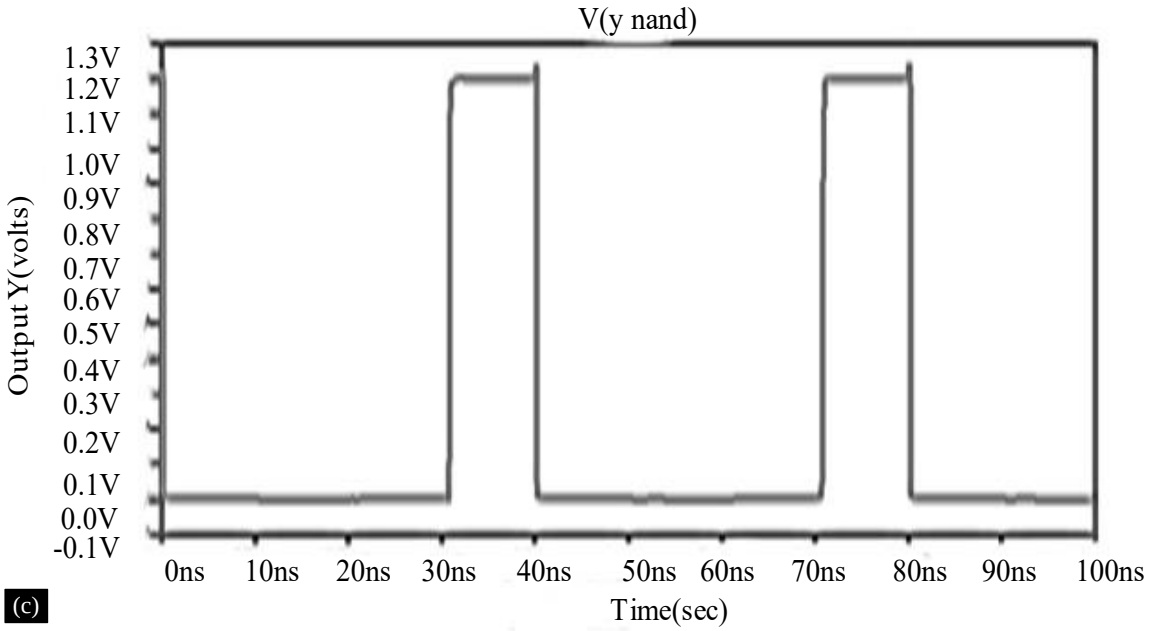
Figure 13. Two input NOR design with FinFET(a)SG-based (b)IG-based circuit.



(a)



(b)



(c)

Figure 14. Simulated waveform for (a) a (input),(b) b (input),(c) y (output)of SG/IG-FinFET based 2 input NOR Gate.

FUNCTION IMPLEMENTATION WITH FINFET

The following function shown in equation (1) is implemented usingFinFET where A,B,C,D,E are the input and F is the output.

$$F= AB'+C(D+E') \quad (1)$$

The SG and IG based FinFET circuit implementation is presented in Figure 17 (a) and (b) respectively. The simulated input(A,B,C,D,E) and output(Y) waveform is shown in Figure 18 (a),(b),(c),(d),(e),(f) respectively.

The truth Table for the function F is given below in Table 1.

Table1. Truth Table for function F.

A	B	C	D	E	AB'+C(D+E')
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Figure 19 on the other hand shows the implementation of the same circuit with CMOS. The simulated output waveform of the same is depicted in Figure 20 in support.

MUX USING FinFET

The 2:1 MUX is also implemented with the SG and IG FinFET. The expression of the 2:1 MUX is given below in equation (2), where S is the select lineD0,D1 are the inputs and Y is the output.

$$Y=S'D0+SD1 \quad (2)$$

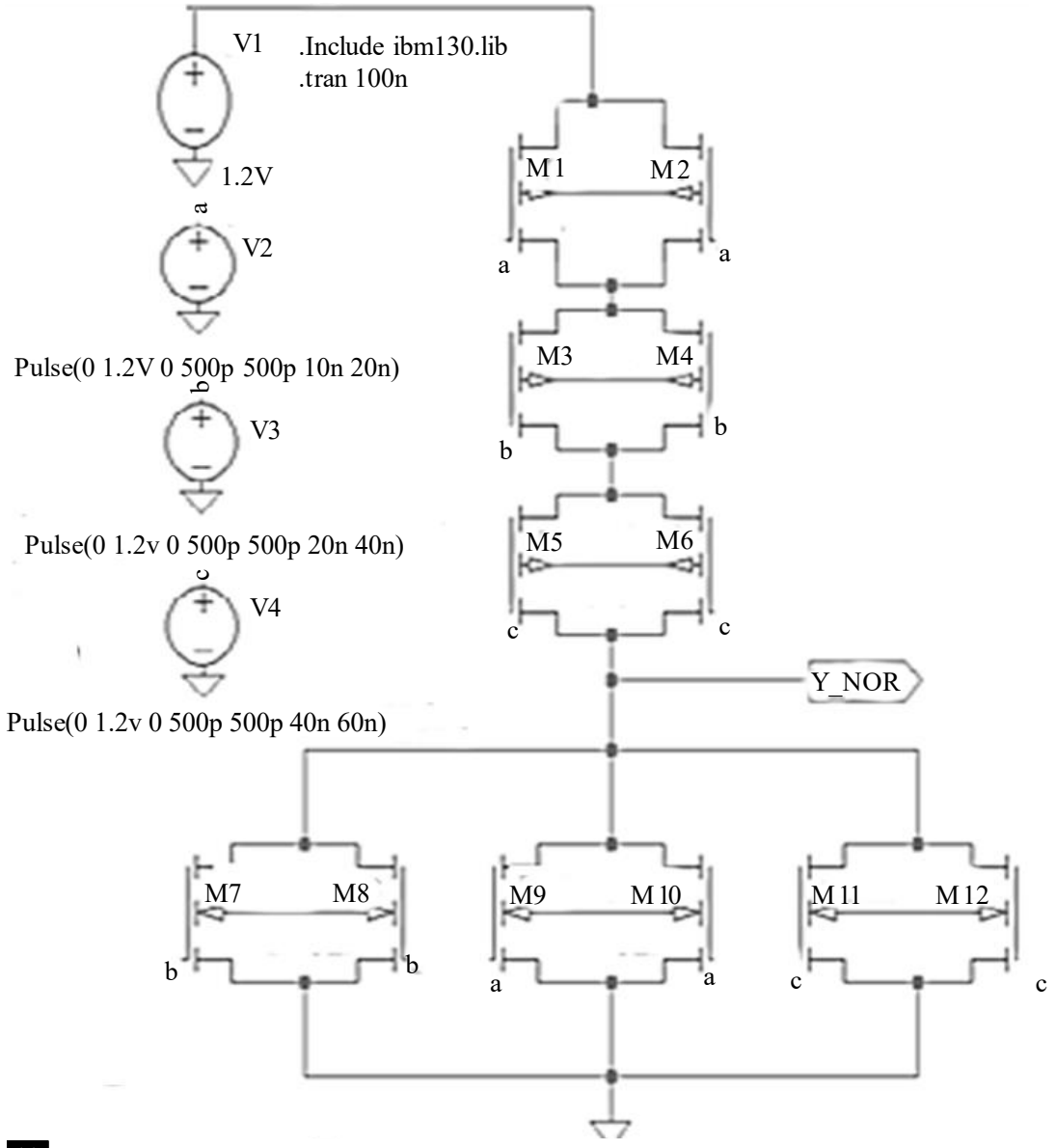
The truth table of the same is shown in the Table 2. The circuit implementation in LTSpice environment of the same is depicted in Figure 21 along with the simulated input output relationship (presented in the Table 3) in Figure 22.

DECODER USING FinFET

In a similar way the 2:4 decoder circuit with SG and IG FinFET is depicted in Figure 23 (a) and (b) respectively. The simulated waveforms in support of the truth Table 3 of the same circuit is presented in Figure 24.

Table2. Truth Table for 2:1 MUX.

S	D1	D0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



(a)

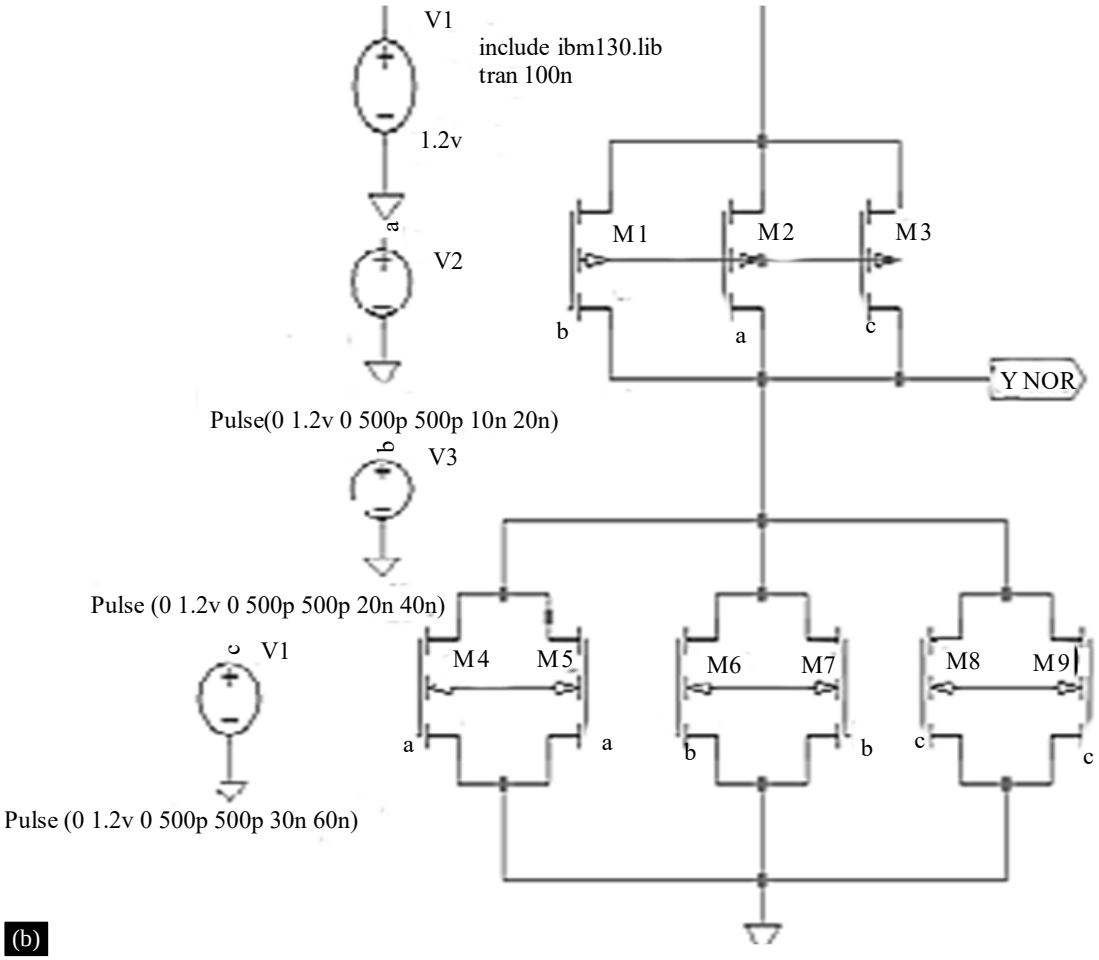


Figure 15. Three input NOR Gate design with (a)SG-FinFET (b)IG-FinFET.

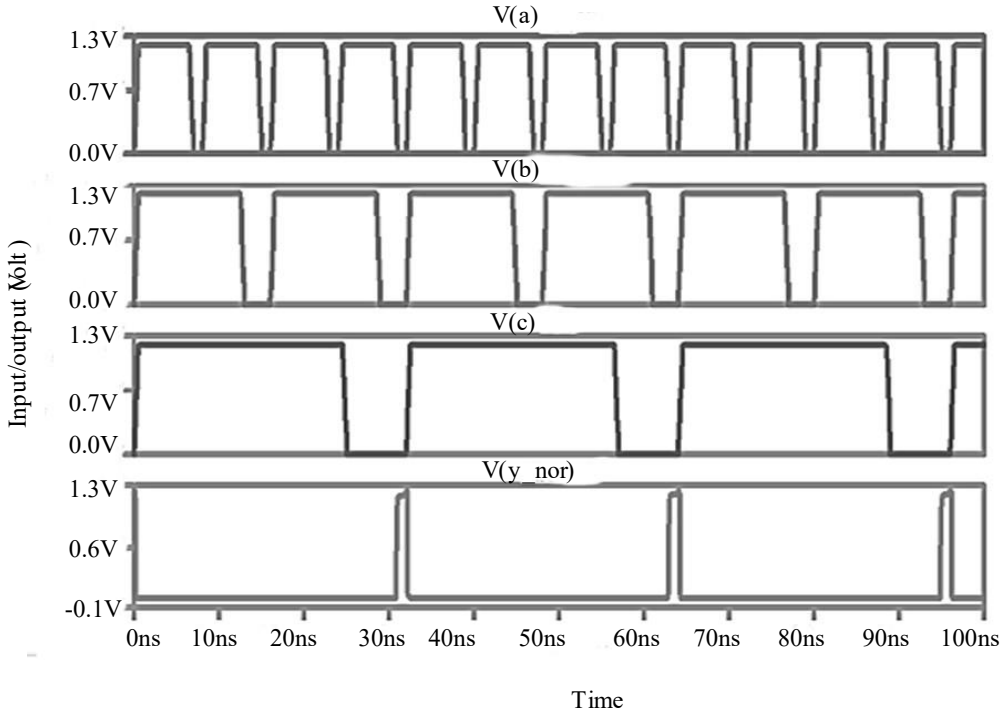
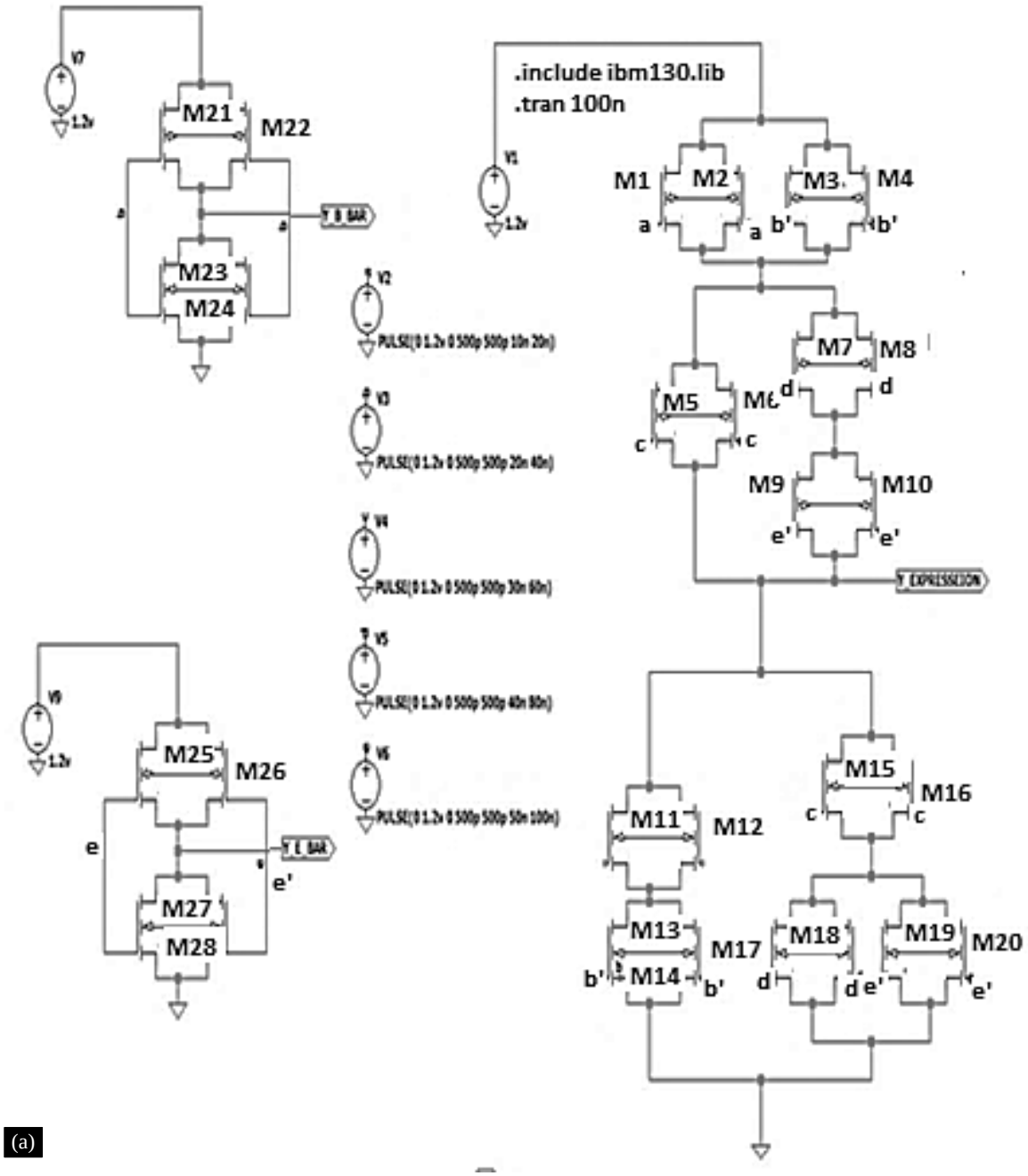


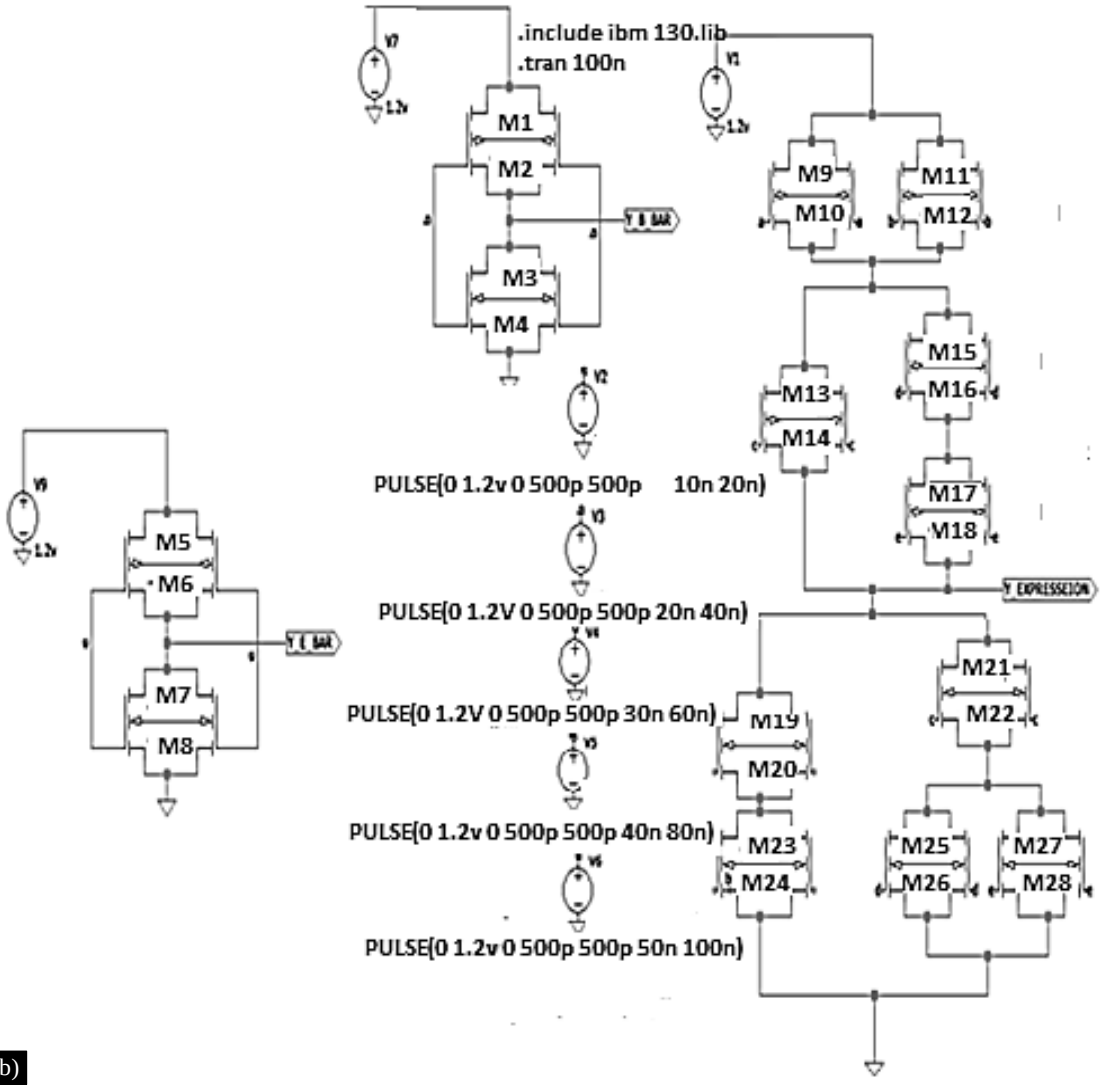
Figure 16. SG/IG-FinFET based 3 input NOR Gate Input output waveforms.

Table 3. Truth Table for 2:4 Decoder.

Input		Output			
A	***B***	***Q0***	***Q1***	***Q2***	***Q3***
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

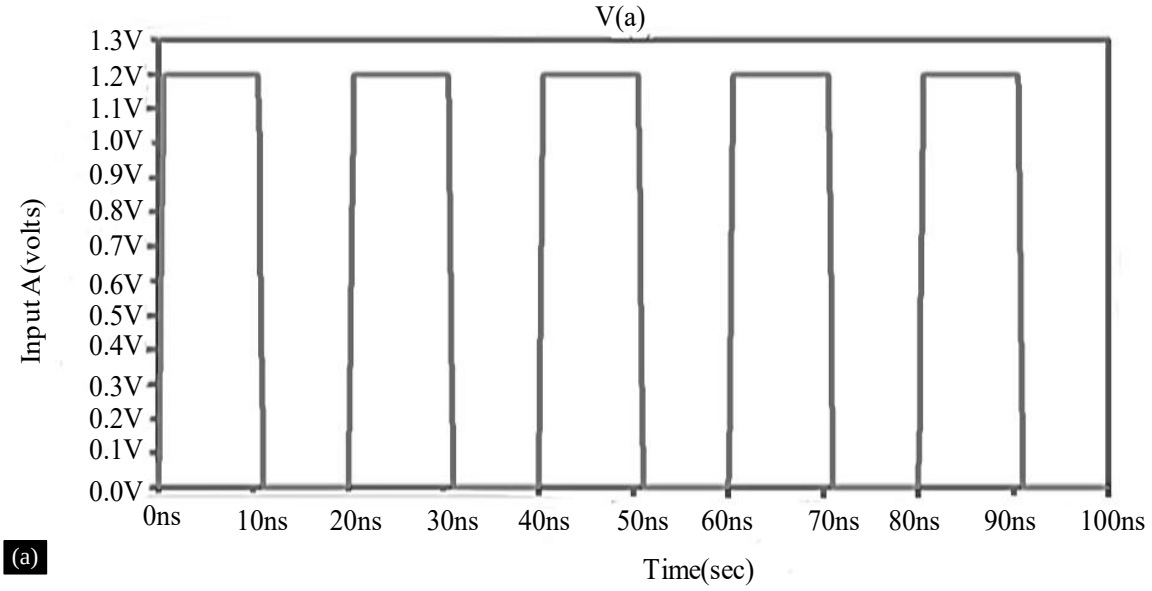


(a)

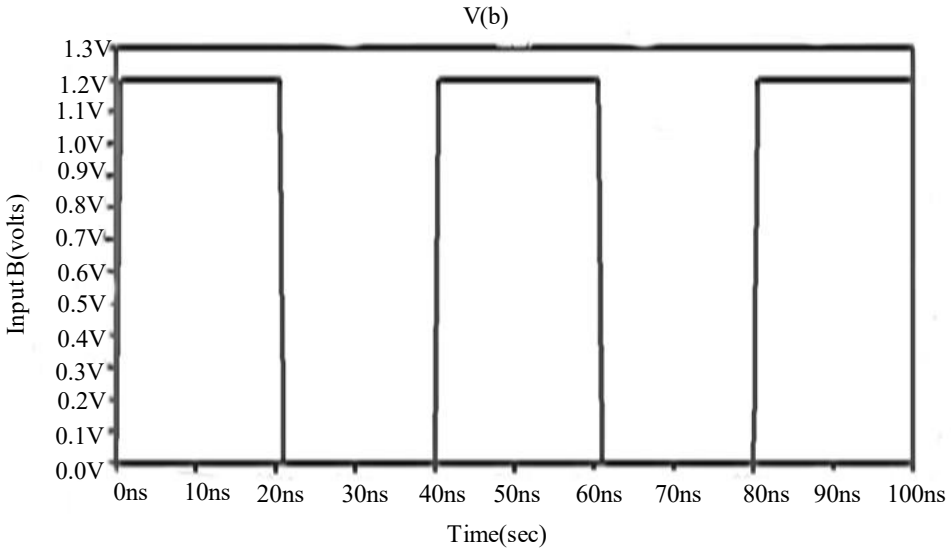


(b)

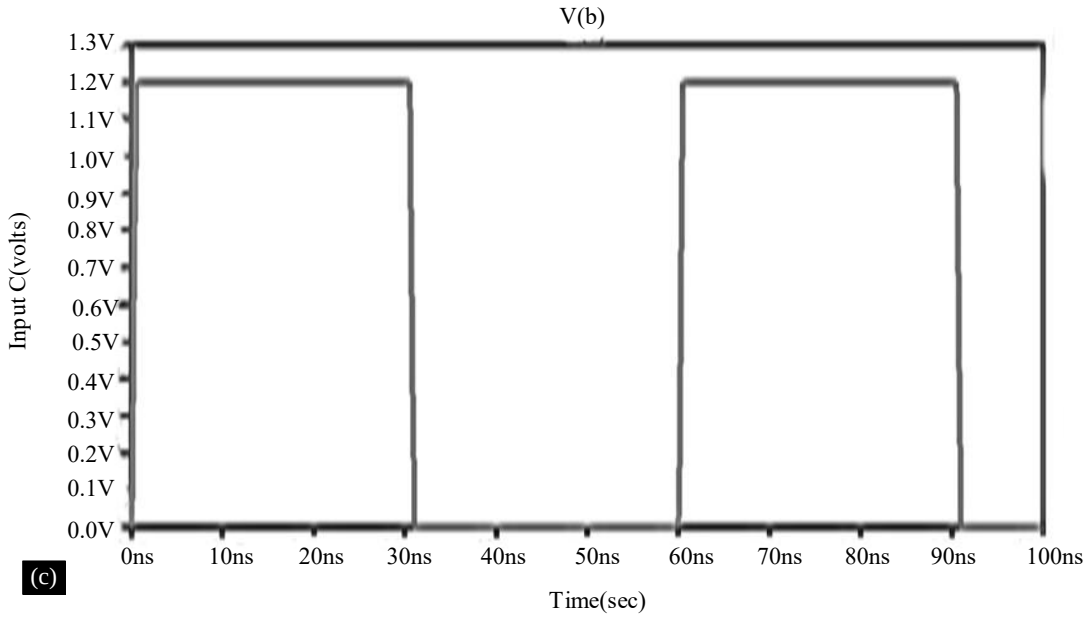
Figure 17. Function(AB'+C(D+E')) implementation with (a)SG-FinFET,(b)IG-FinFET.



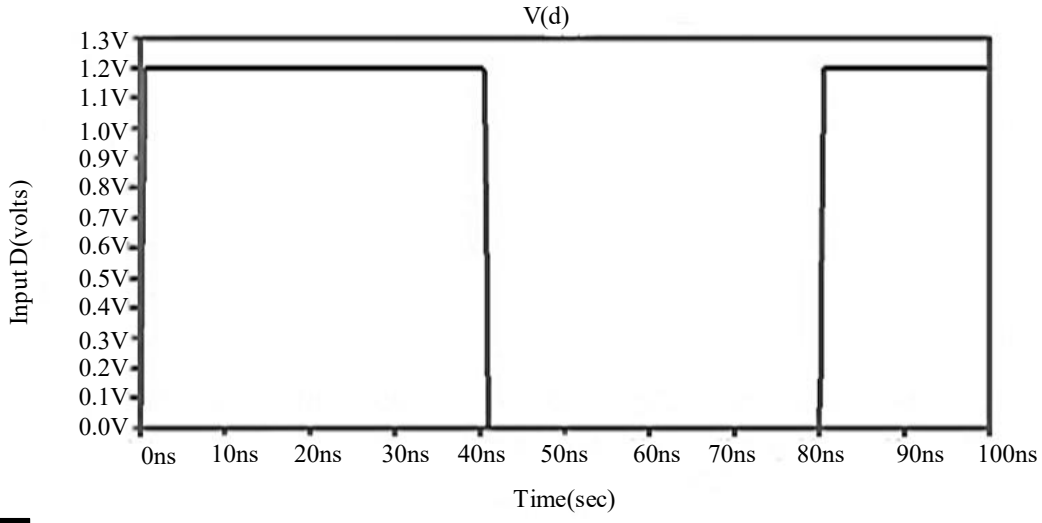
(a)



(b)



(c)



(d)

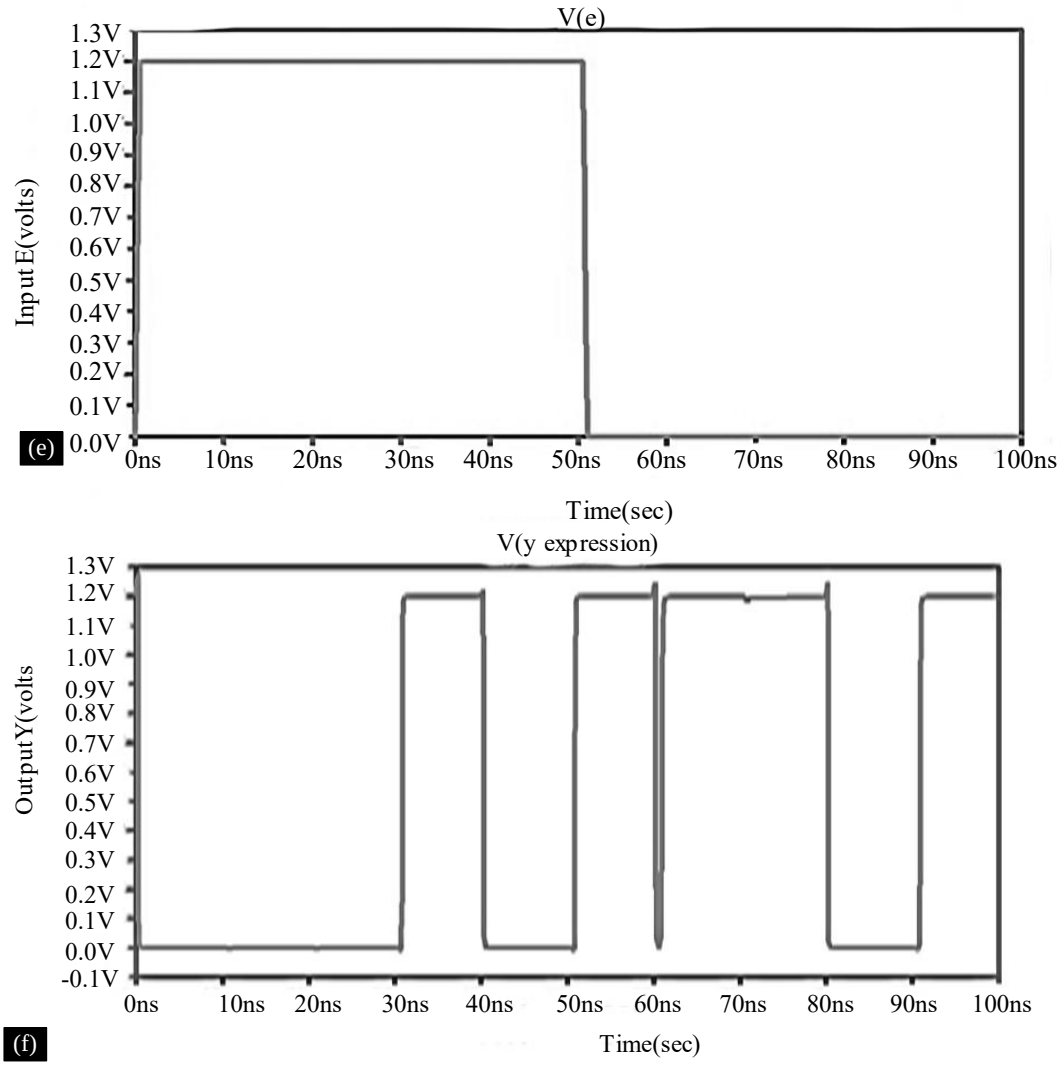


Figure 18. (a) Input A,(b) Input B,(c) Input C,(d)Input D (e)Input E (f) Output Yof SG/IG-FinFET based implementation of function F Gate.

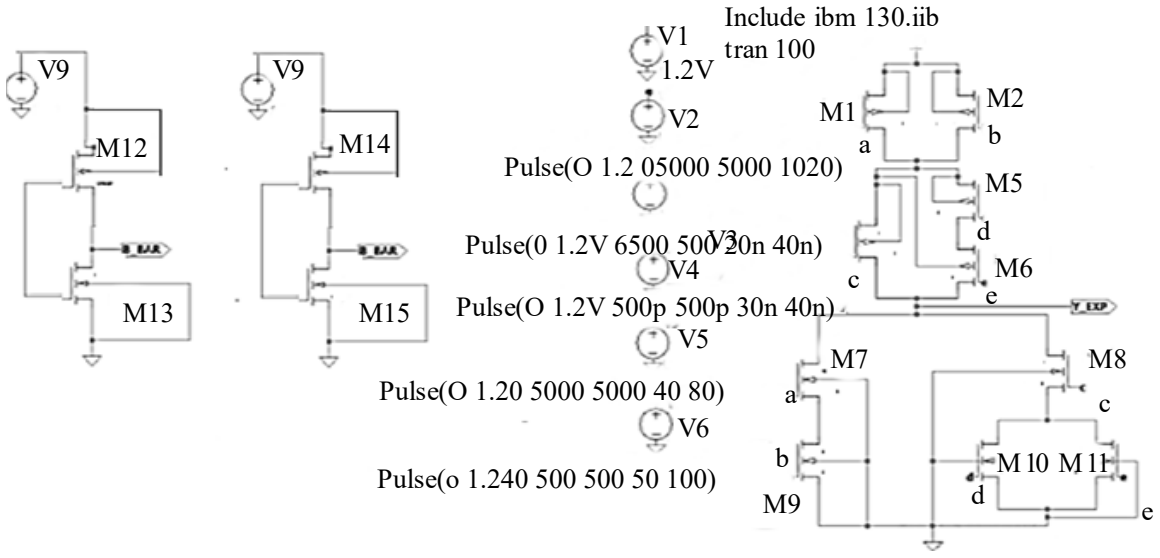


Figure 19. CMOS based implementation of Function F.

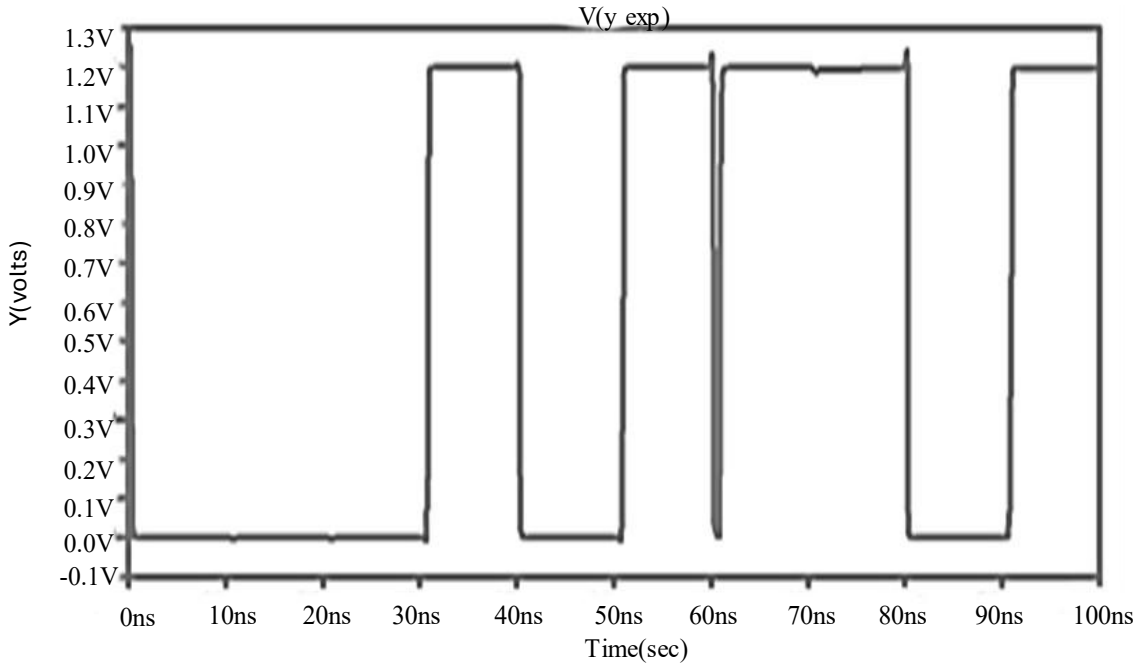


Figure 20. Output Y waveform of the CMOS based implementation of function F.

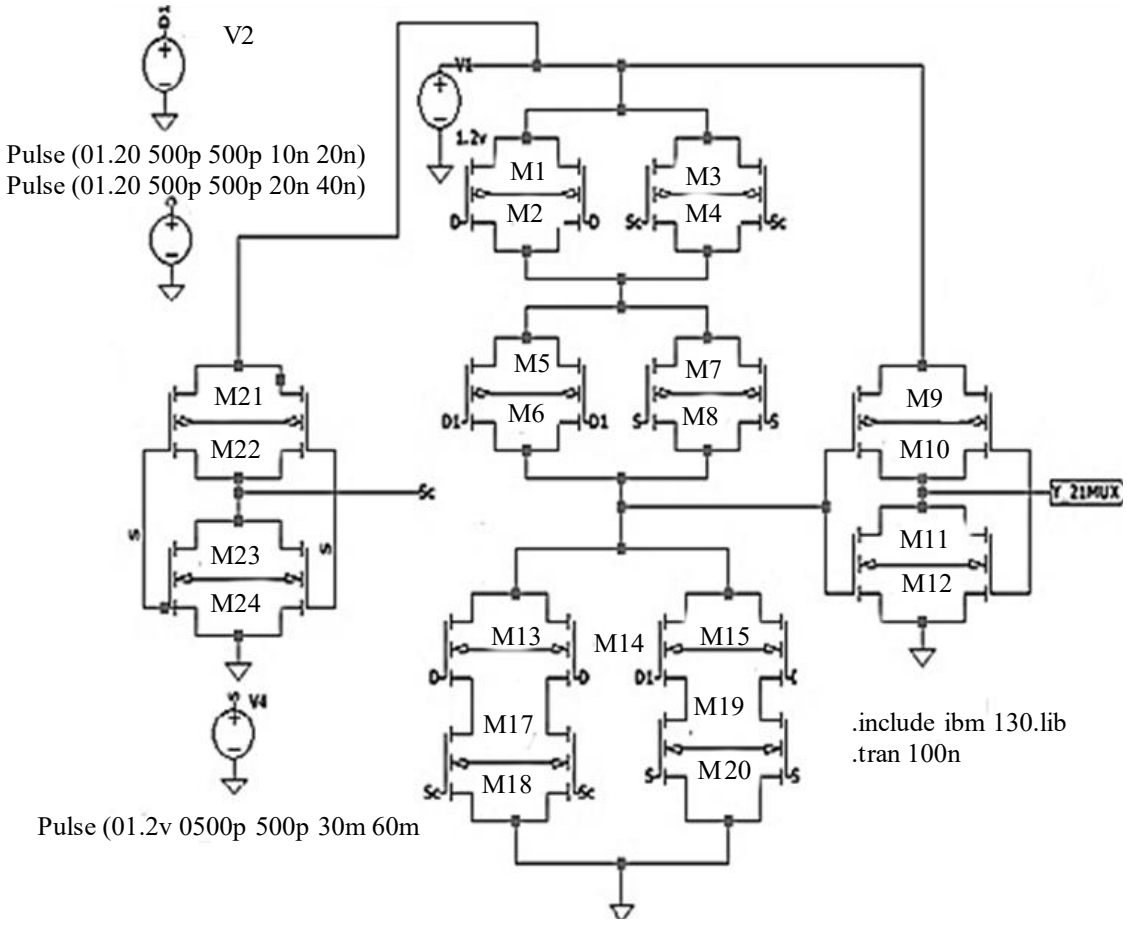


Figure 21. SG-FinFET based 2:1 MUX implementation.

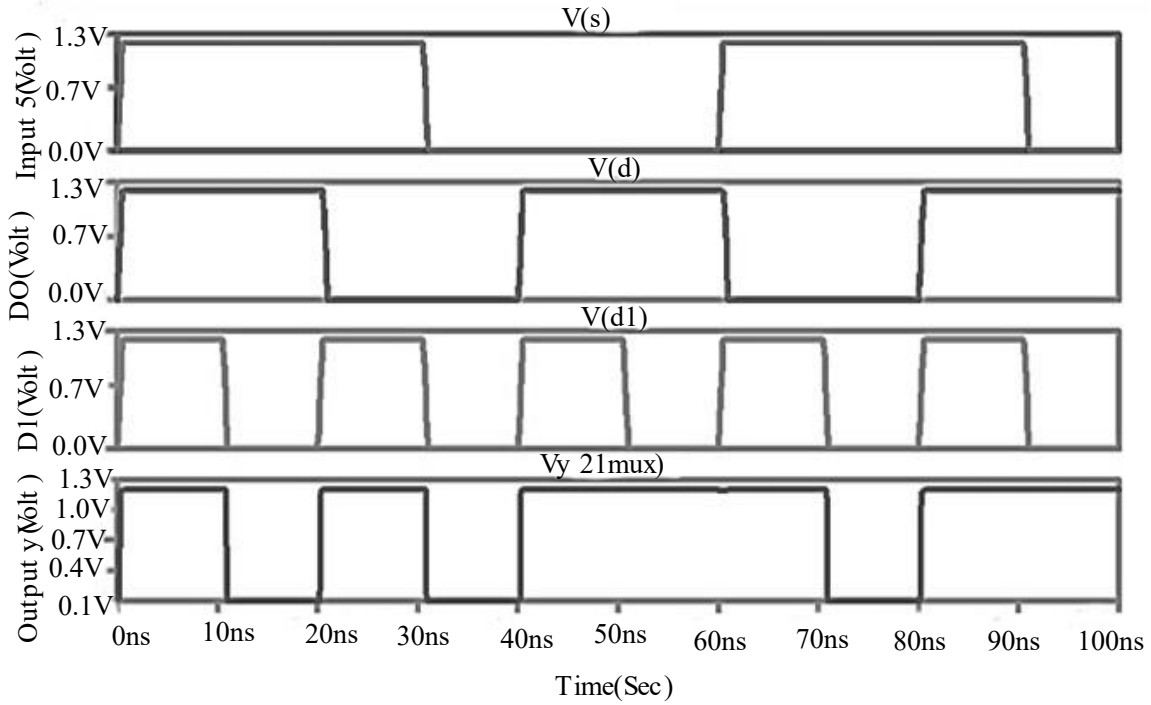
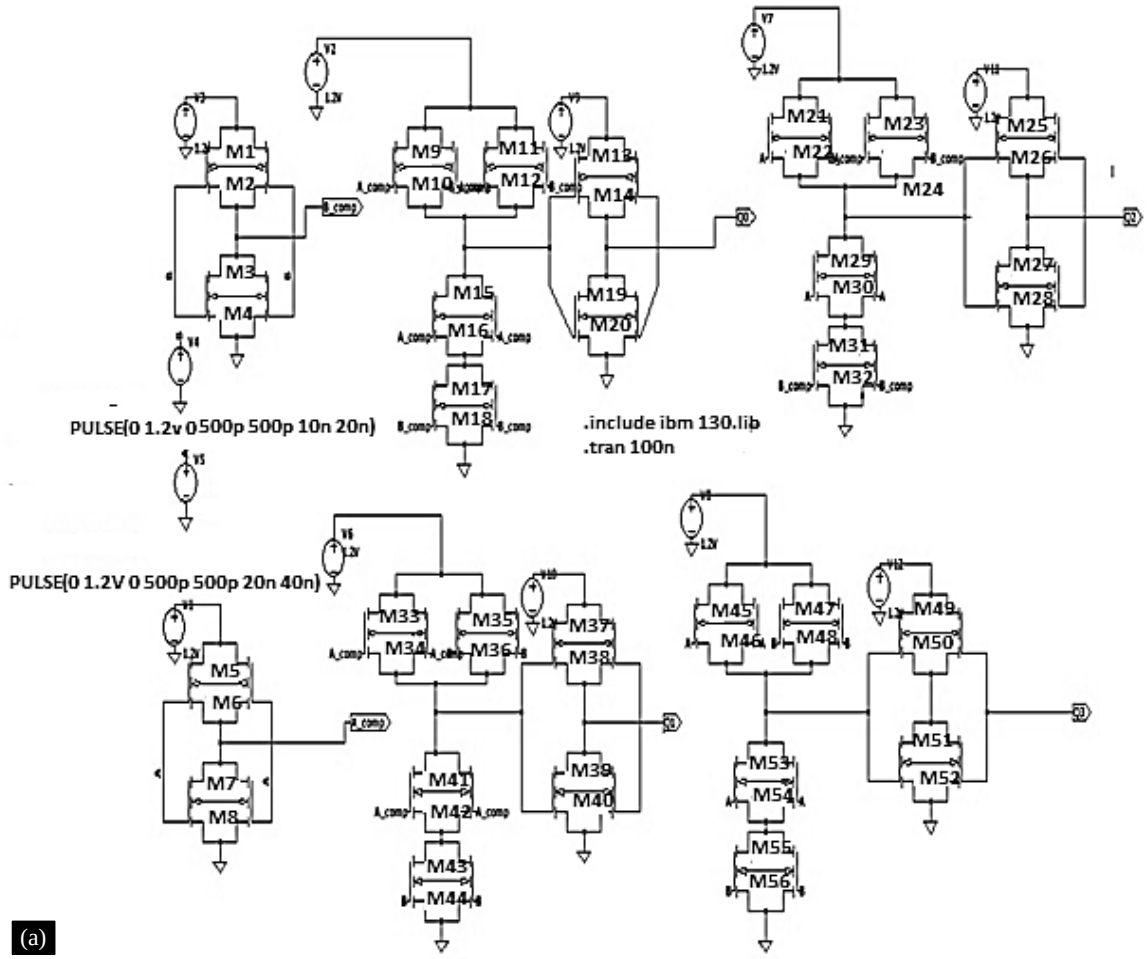
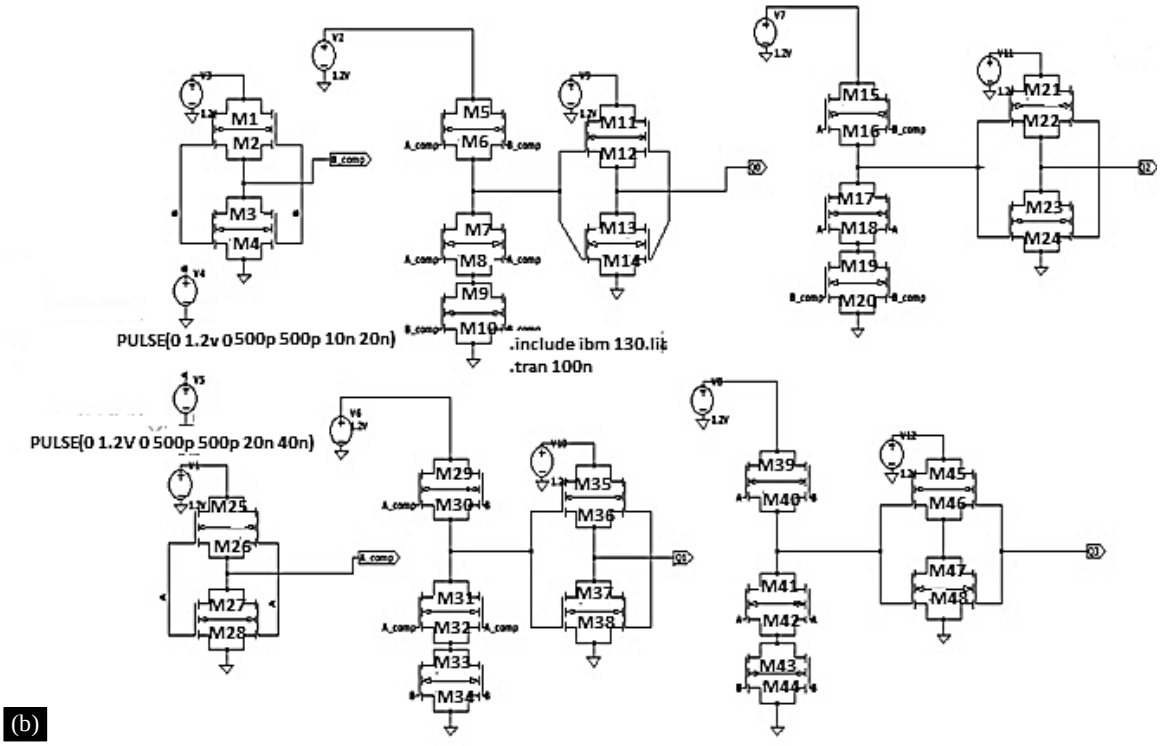


Figure 22. Input(S, D0, D1) and Output Y waveforms of the SG/IG FinFET based 2:1 MUX



(a)



(b)

Figure 23. 2:4 Decoder implementation using (a)SG-FinFET and(b) IG-FinFET.

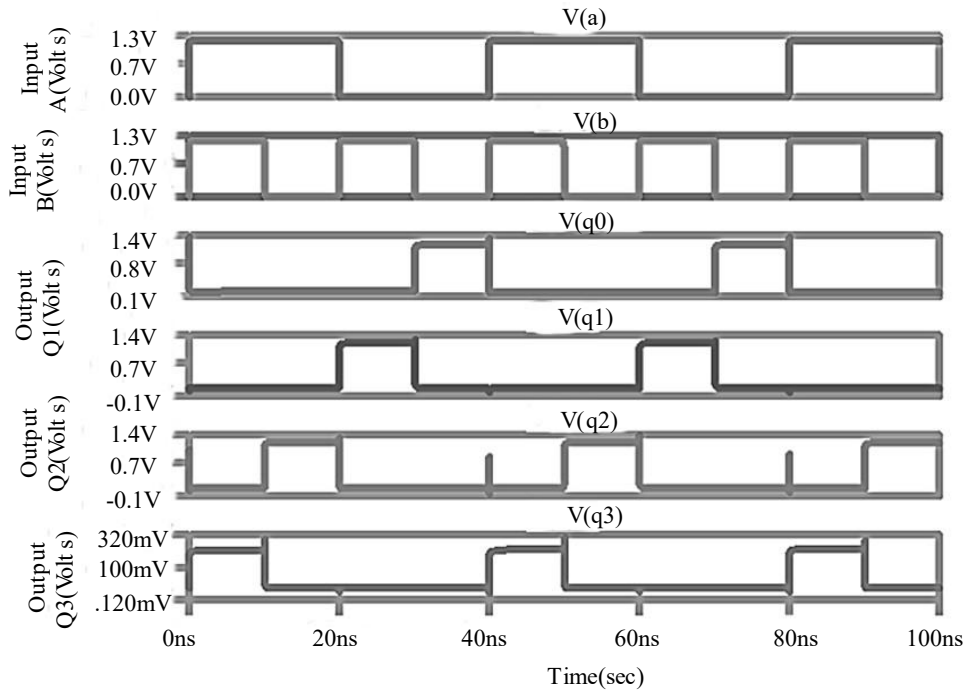


Figure 24. Input (A,B) and output (Q0,Q1,Q2,Q3) waveforms of SG/IG FinFET based2:4 decoder

CONCLUSIONS

The paper demonstrates detailed study of the polymer-based FinFET circuit for different applications. It mainly supports the requirements of flexible electronics when polymer is mainly used as the substrate material for the FinFET. Moreover polymer gate based FinFET can serve as multiple gas sensor. The work also encompasses different logic circuits using the SG-FinFET and IG-FinFET structure in the

LTSpice environment. The structural differences of the Shorted gate and Isolated Gate are studied and different circuits are being implemented such as NOT gate ,2 input NAND gate, 2 input NOR, 3 input NOR, 2:4 Decoder, 2:1 MUX, function implementation .All the simulated results are verified with the expected logical outputs in support. It has been observed that the IG based implementation of the same circuits reduces the number of transistors than that of the SG- based FinFET. Along with the reduced number the power consumption of the IG-FinFET circuits is also reduced.

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