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Performance and Reliability Analysis of NAND Flash Memory through Characterization

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Abstract

An extensive review of NAND flash memory technology is given in this study, with an emphasis on its design, guiding principles, and most recent developments. The importance of NAND flash memory in contemporary digital storage systems is discussed in general terms, emphasizing how widely used it is in everything from consumer electronics to business storage solutions. The underlying architecture of NAND flash memory, including the arrangement of memory cells, pages, blocks, and planes, is then explored, along with its basic concepts. The workings of NAND flash memory are further explained, covering important issues like longevity constraints and program disturbance in addition to ideas like programming, erasing, and reading operations. This study examines the recent historical trends in NAND Flash technology, emphasizing the development of its key characteristics and elucidating the factors that made it not only the most significant integrated solution for high-volume non-volatile storage but also a potent competitor that is steadily eating away at the market share of hard disk drives. We will pay particular attention to the scaling pattern that planar arrays follow and the main physical limitations that affect the dependability and performance of contemporary deca-nanometre technology. This will clarify why focusing all efforts on the integration of 3-D arrays can be deemed more advantageous than developing further planar nodes with feature sizes below ~15 nm, which represents the current state of the art. After that, the most potential 3-D architectures will be examined, with a focus on the advantages and disadvantages of each as well as the implications of the shifting integration paradigm for the main NAND applications.

Keywords: NAND flash, error correction, programming, storage, erasing, 3-D array, memory, CPU, control logic

INTRODUCTION

Many electronic devices rely on NAND Flash memory, a kind of non-volatile memory, including USB drives, memory cards, smartphones, smart TVs, computers, tablets, digital billboards, and traffic signal systems. NAND Flash technology offers affordable options for high-density storage. Electric circuits are used to store data in NAND flash, which is organised into blocks [1]. In NAND flash memory, data is preserved even after power is turned off because a metal-oxide semiconductor adds an extra charge to the memory cell [2]. A metal-oxide semiconductor called a floating-gate transistor (FGT) is usually used; it has a structure that is like that of NAND logic gates. NAND flash controller architecture is shown in Figure 1.

Control gates and floating gates are the two kinds of gates used by NAND memory cells. The two gates work together to control the flow of information [3]. A control gate that receives a

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voltage charge allows the programming of a single cell. Flash memory is a special kind of electronic erasable programmable read-only memory (EEPROM) chip. Two transistors, spaced apart by a thin oxide layer, are accommodated at each intersection of the flash circuit's grid, which is constructed using columns and rows [4]. There is a floating gate transistor and a control gate transistor placed at each junction. The floating gate is connected to its respective grid row by means of the control gate. Cells, strings, pages, and blocks make up the array element [5]. This cell is the bare minimum of what a NAND flash memory circuit has to provide in terms of storage capacity. The NAND Flash cells are structured within the strings, which also function as bit lines. Basic NAND flash memory cell and NAND flash memory structure are shown in Figures 2 and 3.

An additional layer of addressing is added to NAND flash memory compared to NOR flash memory by use of serially connected groups of memory cells. The NAND flash structure is hierarchical, beginning with cells that form five strings, moving on to pages, blocks, planes, and finally a die. The source of one cell is linked to the drain of the next in a string of NAND cells. Both the Word Line (WL) and the Bit Line (BL) make up this. Flash-based Solid-State Drives (SSDs) have enabled a revolution in mobile computing and are making deep inroads into data centres and high-performance computing. SSDs offer substantial performance improvements relative to disk, but cost is limiting adoption in cost-sensitive applications and reliability is limiting adoption in higher end machines. The hope of SSD manufactures is that improvements in flash density through silicon feature size scaling (shrinking the size of a transistor) and storing more bits per storage cell will drive down costs and increase their adoption. Unfortunately, trends in flash technology suggest that this is unlikely.

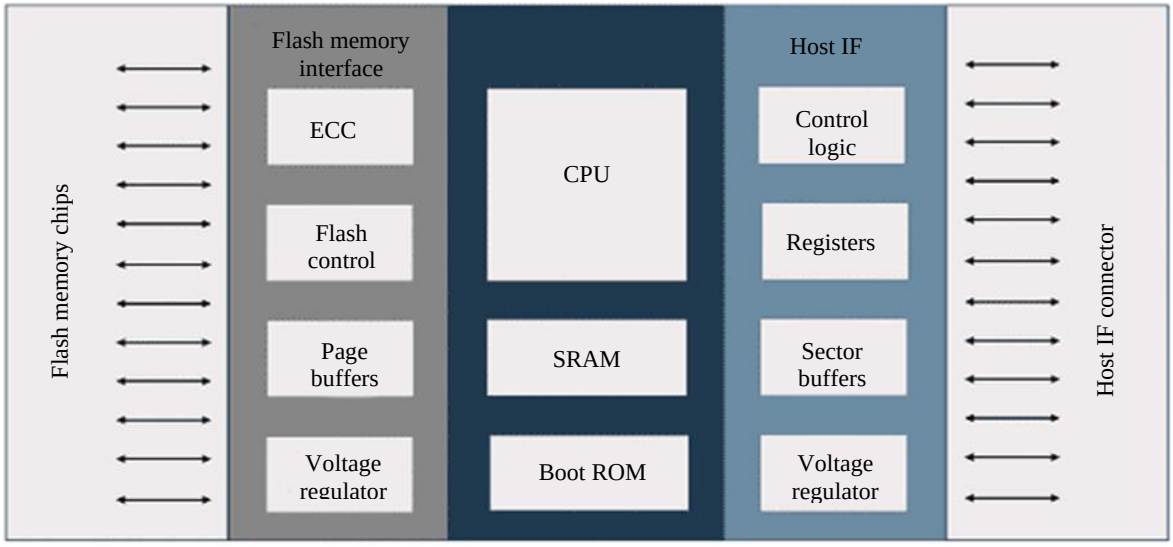

Figure 1. NAND flash controller architecture.

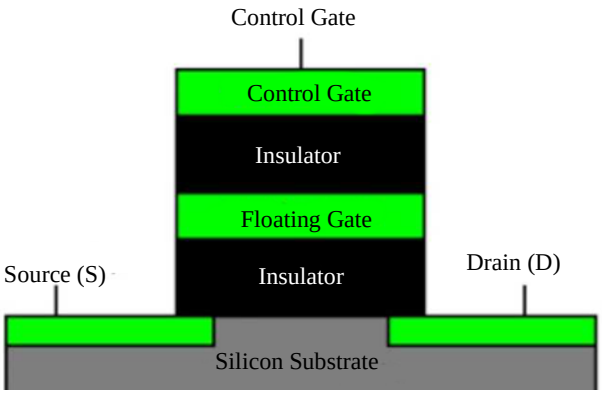

Figure 2. Basic NAND flash memory cell.

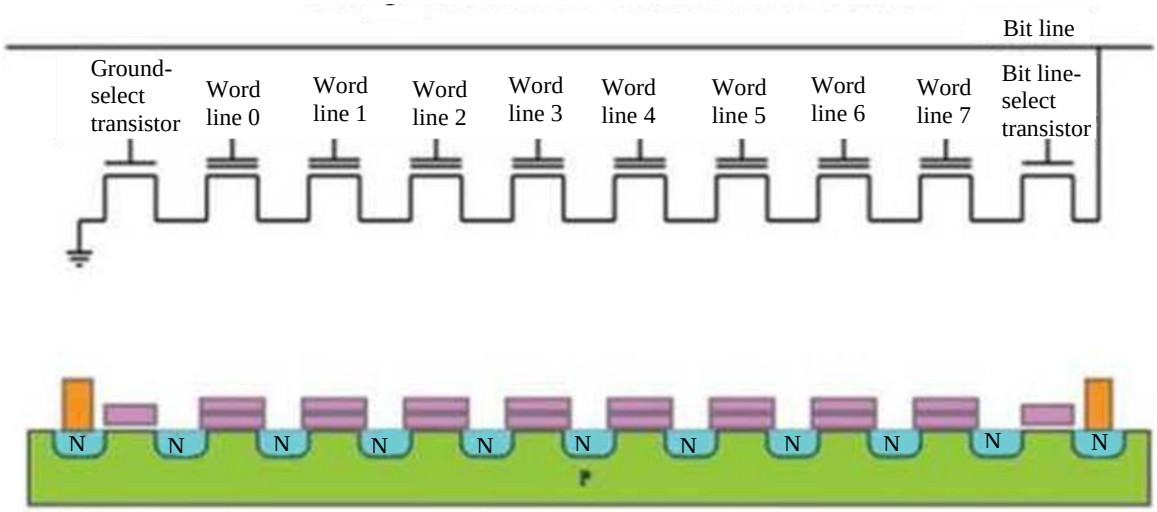

Figure 3. NAND flash memory structure.

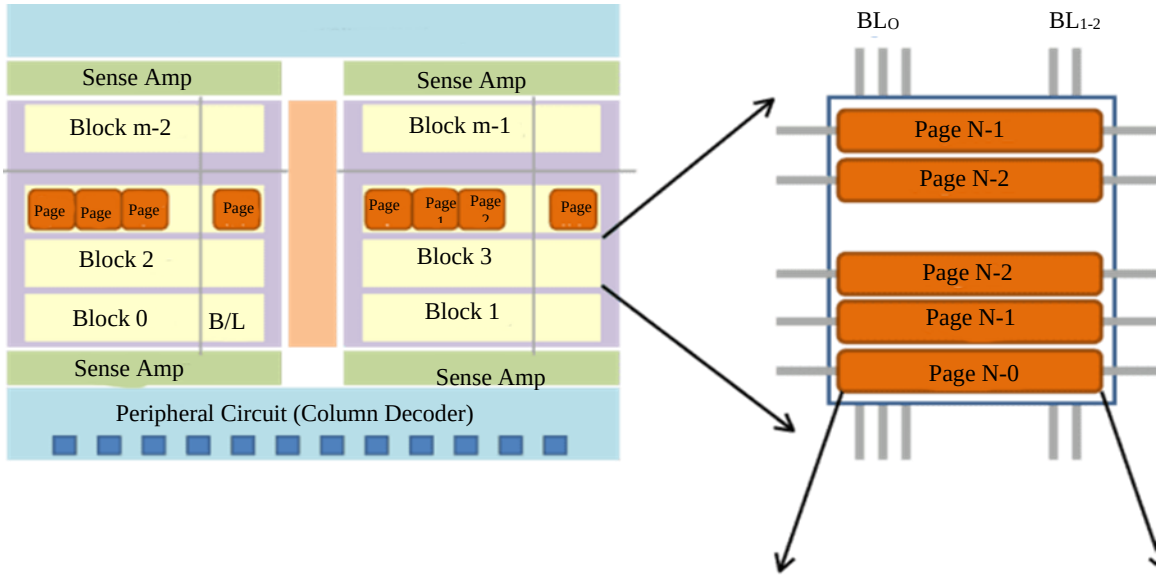

Figure 4. NAND flash memory cell structure.

MODELLING

A 2-dimensional matrix is formed in a block by rows (pages) and columns (strings). Multiplying the string count by the page count yields the total bit count for a block. Micron announced at the 2014 Flash Memory Summit that block sizes may exceed 8 Mbytes and that maximum pages per block are surpassing 512 [6].

Planar NAND Flash blocks are made up of a grid of cells connected by bit lines (BLs) and word lines (WLs). The data is read from the device page after page, with a total of about 16 kb of data. There is one page (SLC), two pages (MLC), or three pages (TLC) in every WL in the block. To make each WL hold 2/4/6 pages, it is possible to further interleave the pages inside a WL. NAND memory cell structure is shown in Figure 4.

Each page, shown as a row, is programmed at the lowest possible unit and shares the same word line. The minimum number of NAND cells required for their construction is 32,768; however, many of the more recent NAND devices include page sizes of 64K or 128K cells [7]. Terms like 2K, 4K, 8K, etc. describe the majority of page sizes. This is the number of bytes that make up the page. Consequently, a 4K page size is 4096 bytes, which is the same as 32,768 NAND cells (bits).

Data Storage and Retrieval Process

The adjustment of electric charges inside the memory cells is the basis of the data storage and retrieval operation in NAND flash memory. When data is written, the desired charge level is applied to the selected cell by the controller, altering its state to reflect the information being stored. High-speed data writes are made possible by this swift operation. The controller reads the data by measuring the charge level in the cell and interprets it as the stored data. NAND flash memory operations are shown in Figure 5.

It has been discovered that write operations in NAND flash memory are simpler than erase procedures. Erasing entails the clearing of entire blocks of cells, thereby preparing them for the writing of new data [8]. However, removing can only be done on empty blocks because of the inherent characteristics of memory in flash. In order to erase a block, the data from the block to be erased is moved by the controller to a different location. Once the block is empty, it is able to be erased, thus preparing it for the writing of new data. Types of NAND flash memory are shown in Figure 6.

Write operations involve the modification of the charge levels within the selected cells, with their state being altered to store the desired data. This procedure is carried out precisely and makes information retrieval and storage effective. Features of NAND flash memory are shown in Figure 7.

- Non-Volatile Memory;
- Reprogrammable;
- Faster Write and Erase Time;
- More Storage; and
- Low Manufacturing Cost.

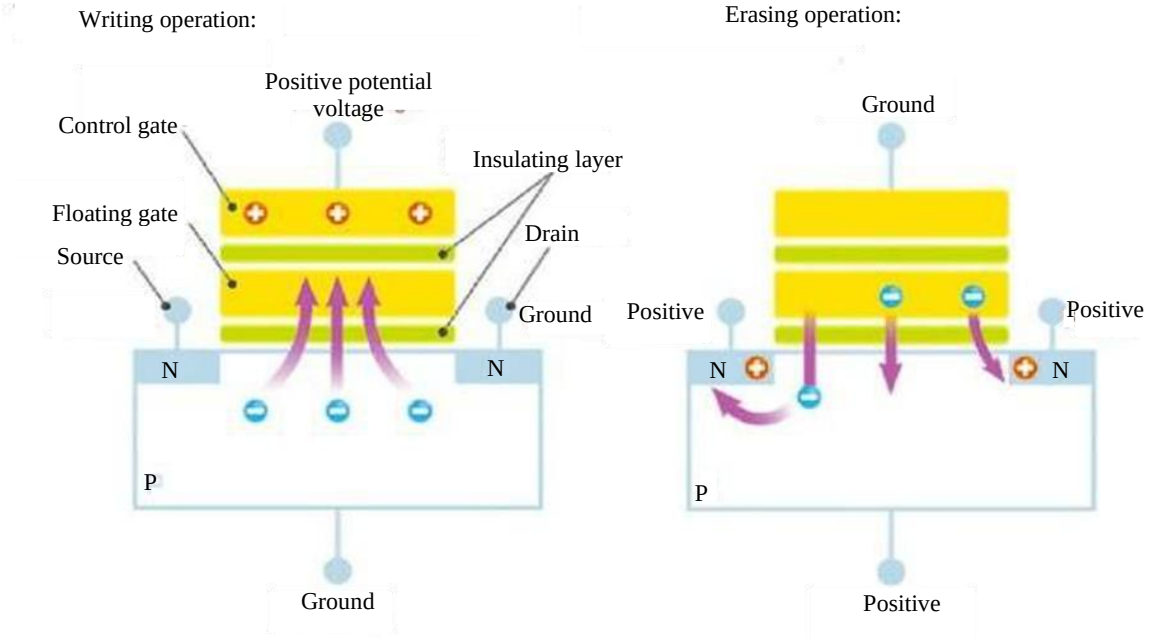

Figure 5. NAND Flash Memory Operations.

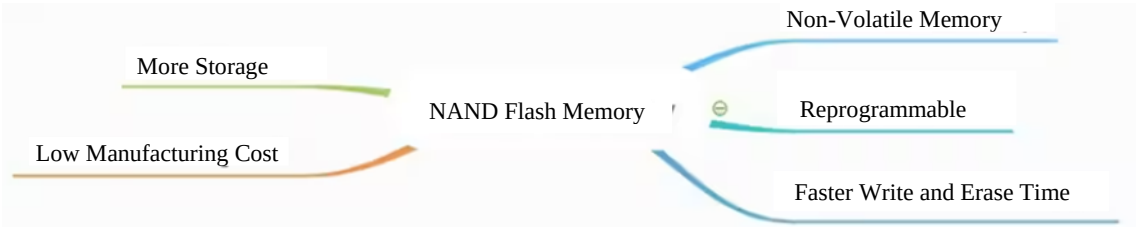

Figure 6. Features of NAND flash memory.

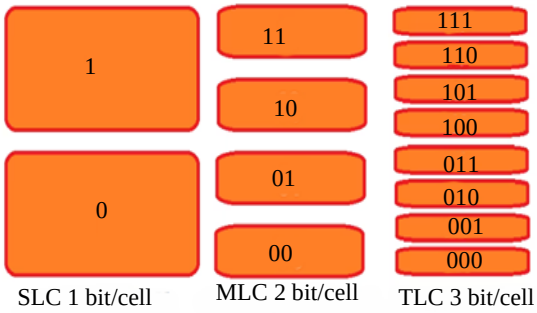

Figure 7. Types of NAND flash memory.

SLC

SLC is an abbreviation of single-level-cell. It is an old type of NAND Flash as each cell can represent just one bit, or binary digit.

MLC

Two bits can be represented by each Multi-Level Cell [5]. Because Write Cycles and ensure occur twice as frequently as SLCs, these cells are less durable than SLCs. TLC, or Triple-Level Cell, is its acronym. As the name suggests, each cell has three memory bits, allowing for greater data storage in the same amount of space. Enterprise and consumer level businesses are the main users of TLC drives.

QLC

As "quad" signifies "four", each Quad-Level cell can represent up to four bits. The technology that offers a lower cost per terabyte than a hard disc is called QLC memory.

NAND Flash Memory 2D

The storage cells in this type of memory are arranged in a two-dimensional matrix by stacking them horizontally. Because the horizontal cells in this form of memory and storage module require more physical space, which increases chip size, it is not produced in large quantities. As a result, 2D NAND Flash is scalable.

Compared to 3D NAND Flash, 2D NAND Flash is less expensive. Although 2D NAND Flash uses roughly 50% less power than 3D NAND, it has a higher latency time. Compared to 3D NAND Flash, this type of NAND Flash has greater Flash Control.

3D NAND Flash Memory

By building the memory cells vertically in a three-dimensional in nature matrix, 3D NAND flash saves space. A NAND Memory storage chip manufactured using this method requires less physical area, resulting in a smaller chip.

Additionally, it enables the producers to reduce the size of the chip and raise the memory capacity. The cost of 3D NAND Flash is higher than that of 2D flash memory for the following reasons. 3D NAND memory is incredibly expensive and complex to create, and a single mistake might render the entire memory chip useless. NAND Flash Memory working is shown in Figure 8.

NAND Millions of MOSFET-based charge trap memory cells comprise flash memory. Nanometre technology has been used to generate these cells. Electrons can be released or trapped by each Charge Trap flash memory cell (CTF). As a result, in the past, each cell could only represent one bit, either 0 or 1. The three working components of CTF are the Charge Trap, Channel, and Gate. These are all divided using a dielectric substance. The component known as a charge trap gets its name from its ability to either release or store electrons. The cell symbolises 1 if there are no trapped electrons, and 0 otherwise. More values can be stored in a single current CFT than in earlier ones.

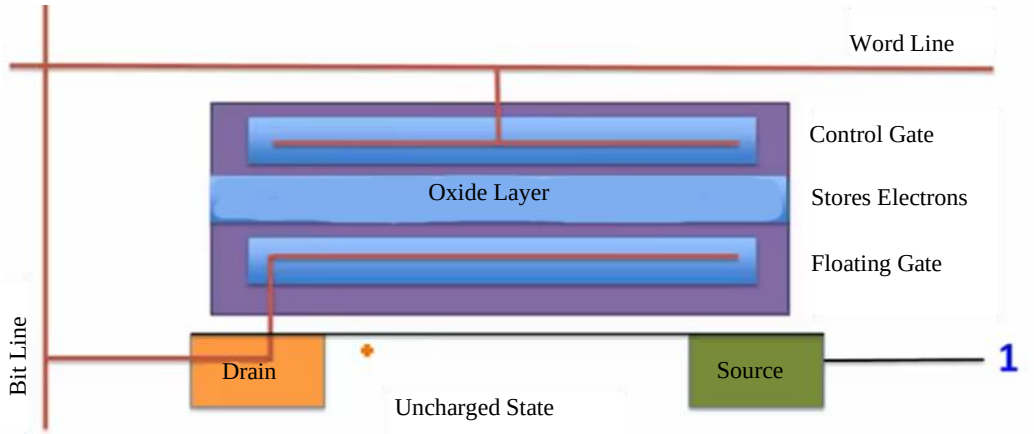

Figure 8. NAND Flash Memory working.

RESULT AND DISCUSSION

Enhancing the reliability of NAND flash memory involves implementing various techniques and technologies to mitigate potential issues such as data corruption, wear-out, and errors. Robust ECC method implementation aids in the detection and correction of potential mistakes that may arise during data storage and retrieval [9]. ECC algorithms add redundancy to the stored data, allowing the controller to identify and fix errors caused by factors like noise, interference, and wear.

NAND flash memory may develop bad blocks over time, which are blocks that contain defective memory cells. Bad block management techniques identify and mark bad blocks during manufacturing or operation, preventing them from being used to store data. The controller then reallocates data to good blocks, maintaining data integrity and reliability. NAND flash memory employs techniques such as wear levelling and error correction codes (ECC) to improve reliability and lifespan [10]. While ECC aids in the detection and correction of data storage and retrieval mistakes, wear levelling helps to distribute write and erase cycles uniformly across memory cells to delay wear-out.

CONCLUSION

A comprehensive overview of NAND flash memory circuits is provided by this study, with their crucial role in modern electronic devices being highlighted. From the fundamental operation principles to advanced architectures and challenges, various aspects of NAND flash memory technology are delved into by the study. By understanding these intricacies, NAND flash memory designs can be continued to be innovated and improved by researchers and engineers, paving the way for enhanced performance and reliability.

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