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# Design and Implementation of Low Noise Power Low and High Speed Three Stage Comparator Using 16nm Technology

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***Abstract***

*In order to meet the demands of quicker operation and reduced noise levels, this study proposes a new CMOS Three-based comparator version. Efficiency may be significantly improved by comparing the suggested model to existing ones. This is so because the suggested comparator would improve the efficiency of the current amplifier design. The suggested model drives the input pairs of the regenerator and the amplified stage, making for a quicker comparator. The structure allowed for significant time savings. To reduce noise, the suggested solution integrates an NMOS pair into a PMOS structure. The ARM architecture's positive feedback characteristic enables excellent comparison efficiency and low static power consumption with negligible leakage currents. There are a few limitations, nevertheless, that must be considered. Leakage current, which was previously mentioned about the latch's primary source current, is what restricts the comparators' speed. This leakage current originates from the pair in the input stage of the Strong ARM. The regeneration phase of the proposed model includes an additional signal to further increase the speed of the suggested circuit. The 16nm BSIM4 Model will be used to verify the proposed model's precision. According to the supplied model, a three-stage circuit may reduce noise by a factor of a few orders of magnitude while increasing speed by 34% compared to a two-stage circuit. Mentor Graphics' 16nm BSIM4 Technology was used to verify the suggested model.*

**Keywords:** CMOS, PMOS, NMOS, BSIM4 Model, Leakage current

## INTRODUCTION

CMOS comparators [1, 2] are becoming more important in the age of analog and digital engineering, even for tasks as fundamental as the first step of amp-like signal strength conversion. The precision, input offset, and resolution of A/D converters are all constrained by the architecture of their comparators. A high-end CMOS comparator architecture is required for improved resolution performance, reduced noise at the ADC's input stage, and finer tuning of the ADC's speed and offset. There are several different types of comparators used in digital and analog circuits. For many years, the Strong-Arm latch has played a crucial role [3, 4]. The positive feedback feature of the ARM architecture allows for low static power consumption and great comparison efficiency with minimum leakage currents. However, there are several constraints that need be considered. The speed of the comparators is limited by leakage current, which was before noted in relation to the fundamental source current of the latch. This leakage current is produced by the pair in the Strong

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ARM's input stage. The input stage current is capped at 0.5 V due to the common mode stage across. A greater input voltage from the power source is required due to the increased use of transistors. When it comes to source leakage current, two-stage comparators do better than one [5-11]. The two-stage plan of Miyahara is seen in Figure 1. It is impossible for the source current to regulate the regeneration speed of the input mode transistors M6 and M7 in this configuration, since they are biased by VDD/2. The biased voltage is about double that of the Strong ARM latch. The reduced number of transistors in the two-stage configuration results in a more manageable minimum supply voltage.

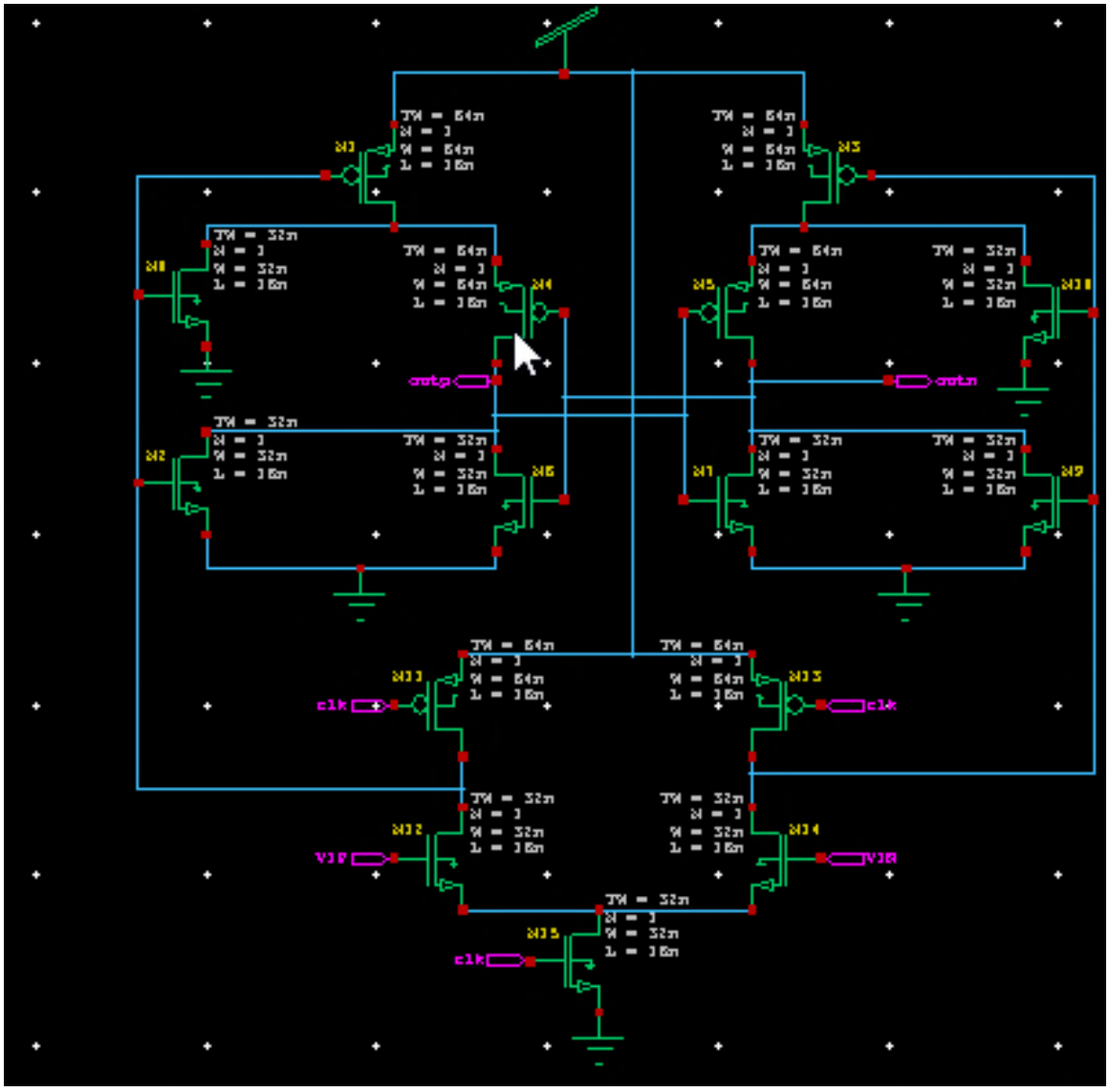


**Figure 1.** Schematic of two stage.

Two-stage structures are faster than single-stage ones and they may perform even better with topological tweaks. Changing the preamplifier stage from a PMOS transistor design to an NMOS transistor layout significantly improves its performance. Significant performance gains may be seen when NMOS transistors are used instead of PMOS ones. The preamplifier module will be expanded by adding a third stage, or comparator module, using a pair of NMOS transistors. There are two potential uses for extra NMOS transistors. The first is a preamplifier stage, while the second is a latch circuit. The voltage gain, regeneration rate, and noise floor are all improved by using a larger number of transistors that can operate in the saturation area. With its revised input configuration, the proposed three-stage module increases regeneration speed while decreasing offset and noise [12]. The updated

 

stage is used for verification of the proposed design using 16nm BSIM4 CMOS Technology. The suggested solution increased productivity by 26% compared to conventional design methods while simultaneously reducing energy consumption by 35%.

## LITERATURE SURVEY

A three-level comparator was used in this study. There is a natural development between the three phases. Unlike the Miyahara comparator, this one has an additional preamplifier stage. During the latch stage, this auxiliary preamplifier inverts the signal by exchanging the PMOS input pair with the faster NMOS pair M11-12. Voltage gain from a second preamplifier speeds up the regeneration process and reduces input-referred offset and noise. When utilizing a second preamplifier, efficiency is sacrificed for speed since the amplified signal must travel farther, via two stages, before reaching the latch stage. Miyahara's comparator and a three-stage comparator's generated transient waveforms are shown in Fig. 3. Equivalent to VDD voltage. M8-9's strong current has the potential to rapidly improve RP and RN. This demonstrates that the extra delay generated by the second stage (about 20 ps in post-layout simulation) is far lower than the huge delay imposed by the latch stage (approximately 200 ps). Due to the second stage's dynamic inverter design, there is little delay between stages. Comparing the three-stage comparator shown in Figure 2 with the Miyahara comparator shown in Figure 3, we see that the latter has a greater amplification rate since its loads are lower (M6-7 and M12-15, respectively) than those of the former In this short exploration, we present a unique comparator design that significantly boosts throughput without negatively impacting noise performance. This comparison works well with SAR ADCs that have both a high sampling rate and a high resolution. This design makes extensive use of the Miyahara two-stage comparator, enhancing it with a single charge pump.

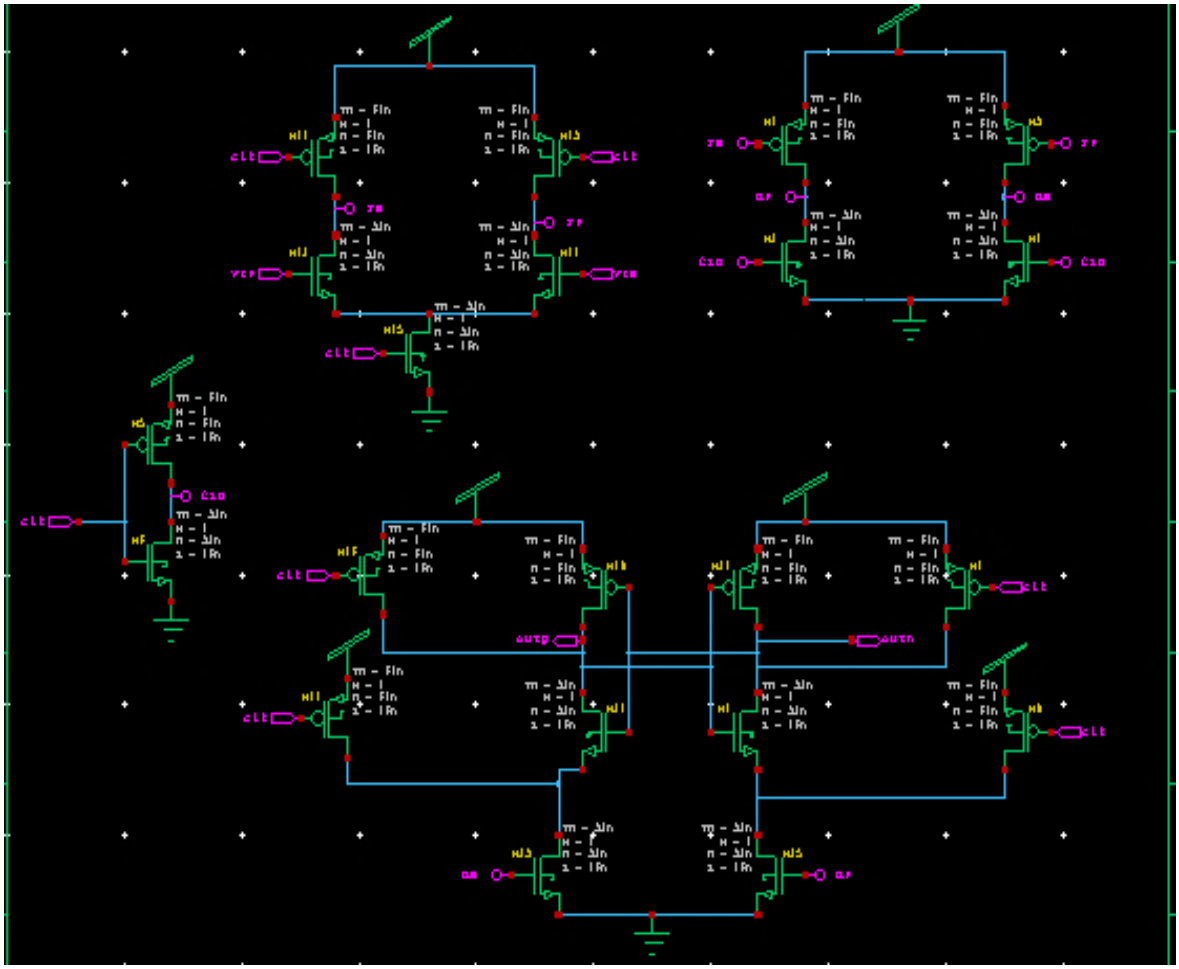

**Figure 2.** Schematic of three-stage comparator (a) Pre-amplifier stage, (b) Latch stage.

 

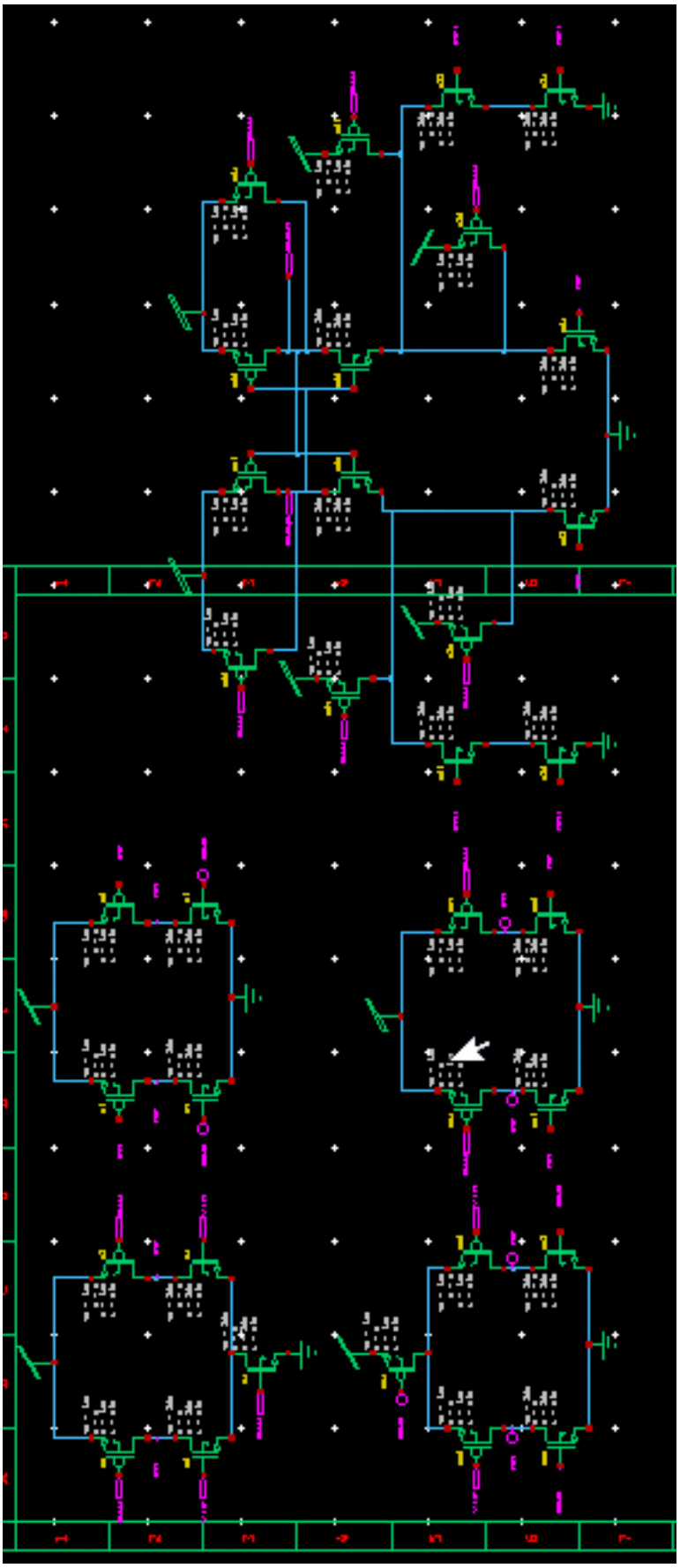

**Figure 3.** Schematic of modified three-stage comparator. (a) pre-Amplifiers with NMOS input pair (b) pre-Amplifiers with PMOS input pair, (c) Latch stage.

 

Very easy adjustment considerably accelerates the comparison process by reducing the time spent on the second-stage amplification and regeneration. The second stage's noise performance may be enhanced by increasing the transconductance of its input pairs and decreasing the integration time. To establish parity, a 40nm CMOS technology is used for both the proposed comparator and the gold standard Miyahara's comparator. Based on the obtained data, it is clear that the suggested comparator is 60% quicker than the traditional Miyahara's comparator, with no noticeable increase in input-referred noise.

This research uses a cascade of integrators with feed-forward (CIFF) architecture to create a wide-band, low-power, time-interleaved (TI) noise-shaped (NS) SAR ADC. To accomplish interleaving and loop filtering passively, switched capacitor (SC) circuits are utilized. This feed forward summing is achieved by using a multi-path comparator. Device ratios control the whole NTF, making it very resilient to changes in PV, P, and T. Because of this, the poles of the loop filter may be situated in a nearly circular area around the unit circle. By eliminating the requirement for amplifiers that generate static current, this study decreases power consumption in comparison to a previously disclosed TI NS SAR ADC based on the error-feedback (EF) architecture. Without the need to control the volume of the amplifier, the PVT-sensitive NTF is unburdened. A prototype ADC constructed with 40nm technology achieves an SNDR of 69.1dB while operating at 50MHz bandwidth, 36.3fJ/conv.-step Walden FoM, and 8.5mW power consumption from a 1.1V supply.

Using 65 nm CMOS technology, we created a latch-type comparator with a dynamic bias pre-amplifier. When using a tail capacitor in combination with the fundamental dynamic bias, it may be possible to reduce power consumption by just partially discharging the pre-amplifier's output nodes. The comparator's power efficiency and input referred noise voltage are measured and compared to those of state-of-the-art devices. Using first-order equations, we demonstrate how to optimize the pre-amplifier's signal-to-noise ratio and gain. The findings indicate that the average energy consumption of the dynamic bias comparator may be decreased by a factor of 2.5 when compared to the previous art, which is also implemented on the same device, for the same input- equivalent noise at an input common-mode level of half the supply voltage Delaying the latch until the assessment is complete might help the preamplifier keep its gain without wasting too much power. By increasing the gain of the preamplifier using tiny cross- coupled transistors, the PMOS transistors at the latch input may turn on sooner, resulting in a shorter delay.

## EXISTING METHOD

Existing two-stage comparator modules (shown in Figure 1) employ a three-stage architecture consisting of a regeneration stage, a reset stage, and an amplification stage. The two-stage design enters the reset phase when the input clock signal goes to zero. When the time is set to one, the circuits enter an amplified state. After being amplified, the input signal is transmitted on to the latch circuit. OUTP and OUTN were linked to VDD or GND during the recovery phase. The current state, however, has a number of drawbacks, such as increased waiting times, higher energy consumption, and reduced transfer rates. This is because the input stage makes use of two complementary PMOS transistors.

## PROPOSED METHOD

### Three Stage Comparator

The preamplifier stage (often referred to as the second stage) is a new module introduced in the suggested design that improves the current architecture. Everything is released in a systematic manner. Using an inverter design for transistors M11 and 12 instead of PMOS transistor pairs may increase the speed of the comparator circuit. Although the comparator is efficient in producing higher voltage gain with lower noise, its speed is diminished since the signal must go through two stages before reaching the final stage. The delay occurred during the wiring of GND to FP and FN. Significant gate-to-source voltage dips are generated at these nodes, which are linked to transistors M8 and M9.

 

## PROPOSED COMPARATOR ARCHITECTURE

We propose a novel design based on a revised three-stage comparator model that achieves both faster operation and lower kickback noise. Figure 3 depicts the primary variations between the modified comparator model and the conventional comparator circuit. (b) The M29-32 transistors are used in the two-stage comparator shown in Figure 3. (a) And the latch stage shown in Figure 3. (c). PMOS transistors are used in the preliminary design stages.

What follows is an explanation of the revised three-stage model. Nodes FP1 and FN1 (where F for fall and P for Promenade) are connected to the positive supply voltage (VDD) in the reset phase, as seen in Figure 3 (b), whereas nodes RP1 and RN1 (where R for Rise) are connected to the ground terminals. Figure 3(c) shows that M30 and M32 are in cut off mode due to the biasing transistor design. Static electricity is prevented from damaging transistors M29-M32 in these setups.

During the amplifying phase, CLK is set to logic 1 and CLKB is assigned to logic 0. Figure 3(c) depicts the area where RP1 and RN1 intersect VDD. After that, we reset the FP1 and FN1 Nodes' logic to zero. This occurred because of RP1 and RN1 rising to prominence before FP1 and FN1. Figure 3(c) shows that a differential current may flow between the OUTP and OUTN nodes thanks to the latching connections. When both FP1 and FN1 are set to logic 0, the static current drops and the speed rises, as shown in Figure 3(c), thanks to the differential voltage created between OUTP and OUTN, which is employed to reduce background noise and speed up the regeneration process.

### Simulation Results with 16nm BSIM4 Technologies

The differences between 65nm and 16nm BSIM4 CMOS Technology in a three-stage CMOS comparator is laid out in Table 1. The following table demonstrates that the suggested design verified with 0.8VDD has lower static power consumption (0.38W) and lower latency (25.01ns).

Various comparators design supply voltage number of transistors delay, and power consumption are compared and contrasted in Figure 4.

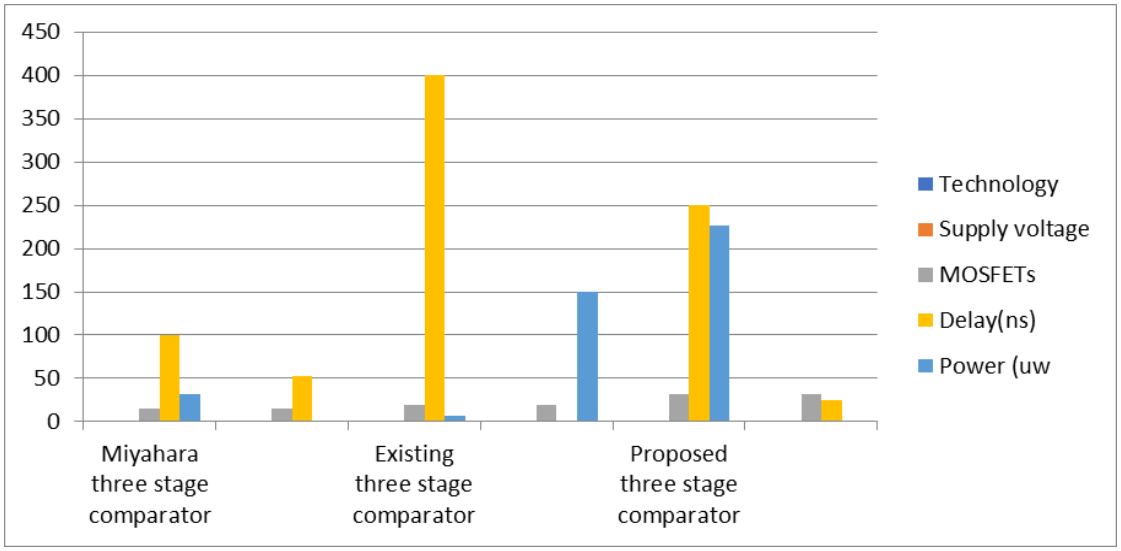


**Figure 4.** Graphics representation of CMOS three stage comparators with different methods.

## CONCLUSION

A three-stage comparator circuit is suggested for this purpose. Modified design to accommodate more circuitry. The suggested method reduces power consumption, produces less kickback noise, and processes data more rapidly than the standard approach. Mentor Graphics' 16nm BSIM4 technology

 

was used to verify the efficacy of the suggested three-stage comparator technique shown in table.1. We also compiled a table that shows how various two-stage comparators fared in our simulations.

**Table 1.** Comparison of CMOS three stage comparators.

| | **Comparison of three stage comparator and its modified version with fastest speed and low kickback** | | | | | |
|---|---|---|---|---|---|---|
| | ***Miyahara Two- stage comparator*** | | ***Existing three stage comparator*** | | ***Proposed three stage comparator*** | |
| Technology | 65nm | 16nm | 65nm | 16nm | 65nm | 16nm |
| Supply voltage | 1.8 | 0.7 | 1.8 | 0.7 | 1.8 | 0.7 |
| MOSFETs | 15 | 15 | 19 | 19 | 32 | 32 |
| Delay (ns) | 99.96 | 53.43 | 399.75 | 0.77 | 249.64 | 25.01 |
| Power (uw) | 31.247 | 0.0801 | 6.55 | 150.166 | 227.03 | 0.38 |

## Future Scope

Fast operation, minimal kickback noise, and low offset and noise at the input are some of the features of the three-stage comparator and its modified version that we present in this short. These comparators pair well with SAR ADCs that sample at fast rates and provide great resolution. Finally, real-world application has confirmed these criteria's worth.

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