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Study the Effect of Applied Gate Voltage on Threshold Potential and Carrier Transport Behavior of Three-Terminal Novel Prototype Device having Configuration P-type $Si/SiO_2/CuFeS_2/Al$

Asmita Patra[1], Suman Mahata[1], Animesh Layek[1,*]

Abstract

This study presents a trial approach for the fabrication and characterization of a novel p-Si/SiO_2/$CuFeS_2$/Al field-dependent three-terminal electronic device designed to investigate charge transport behavior across multiple semiconductor junctions under externally applied bias voltages. The proposed prototype incorporates $CuFeS_2$ (chalcopyrite) as the active semiconductor layer, marking its first reported application in a field-induced electronic device architecture. The device was fabricated using a layered heterostructure consisting of p-type silicon, a silicon dioxide insulating layer, a $CuFeS_2$ active channel, and an aluminum electrode. Electrical characterization was performed by applying source-drain and gate bias voltages to evaluate carrier transport mechanisms, threshold voltage modulation, and field-dependent electronic response. The experimental results demonstrate that the applied gate electric field significantly influences charge carrier transport from the source to the drain, indicating effective field-controlled conduction through the heterojunction interfaces. A notable and unusual shift in the threshold voltage was observed with increasing gate voltage, suggesting the presence of interface charge trapping, field-induced band modulation, or altered carrier injection mechanisms within the $CuFeS_2$ layer. The observed transport characteristics reveal the potential of $CuFeS_2$ as a promising semiconductor material for field-effect electronic applications. The underlying physical mechanisms responsible for the electrical behavior are analyzed and discussed based on experimental observations and device architecture. This preliminary investigation establishes the feasibility of integrating $CuFeS_2$ into field-controlled semiconductor devices and provides valuable insights into its charge transport characteristics. The findings may contribute to the future development of novel semiconductor devices, electronic switches, sensors, and low-cost field-effect electronic components based on chalcopyrite materials.

Keywords: CuFeS2 semiconductor; Threshold potential; carrier transport mechanism; Three terminal electronic device

INTRODUCTION

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In the recent past, the inorganic metal-oxide semiconductors and their derivatives have become popular over conventional semiconductors in designing electronic devices such as diodes and field-effect-transistors. This has been made possible due to their easy fabrication, modulation capabilities, low cost, and large area device characterization compared to crystalline intrinsic and extrinsic semiconductors. Compounds of the chalcopyrite type are of considerable interest as they are closely related to the well-known semiconductors with a wide range of energy gap. Among all the pronounced chalcopyrite, $CuFeS_2$

plays a crucial role in determining their eventual use for any particular application. The iron chalcopyrite is extensively studied system among the chalcopyrite family containing transition metal ions and its structure consists of Cu^{1+} and Fe^{3+} ions. It was reported earlier that $CuFeS_2$ is a semiconductor having unusual optical [1], electrical [2] and magnetic [3] properties. The band gap energy of $CuFeS_2$ is reported very low (0.5-0.6 eV) with anomalous conductivity [4]. The high mobility of Cu and the existence of mixed valence states in copper sulfides [5-7] offer chemical and structural freedom for the easy diffusion of other metal ion/ions in them. $CuFeS_2$ has been quite beneficial to tune the band gap energy over a wide range during their chemical growth. Depending upon the precursor and chemical route, morphology can also be altered to tune the optical band gap. It is reported earlier that $CuFeS_2$ nanoparticle is an energy quencher and is a productive semiconductor like material. However, still the execution of this type of material in fabrication of electronic devices is unexplored.

In this report we illustrated the easiest approach to executing $CuFeS_2$ of wide band gap energy in application to a new kind of electronic device, which consists of semiconductor-insulator-semiconductor with configuration p-type $Si/SiO_2/CuFeS_2$. Since, there was no such background, only but semiconductor-insulator-semiconductor (SIS) junction physics, so the device (mentioned in Figure 1) have been treated as three-electrode semiconductor system, consisting of source, drain and gate terminals. The main objective of this research is to intervene into the carrier transport mechanism within the structured device and investigate the responsible change in transportation pathway within the junctions for the applied potentials as constraint at gate terminal. To get insight into the charge transport mechanism and to realize the underlying phenomena the data of this device had been computed. This computation is alike to p-channel metal-oxide-semiconductor field effect transistor (p-channel MOSFET).

Experimental

The prototype structure investigated here is a metal sulfide semiconductor-insulator-semiconductor junction, consisting of two thin layers of $CuFeS_2$ (considered as source and drain) at separation 2mm on SiO_2 coated p-type Si wafer (Figure 2). Two aluminium electrodes were deposited on the thin films of $CuFeS_2$ by vapor deposition method. A third electrode (gate) is deposited on SiO_2 in between the channel of $CuFeS_2$ films by the same technique with shadow mask. Another back contact is made by Ag paste. The thin films of $CuFeS_2$ were fabricated by room-temperature cast deposition. Before fabrication of the device, $CuFeS_2$ was synthesized by hydrothermal method and was characterized, which were described elsewhere [8]. The transport experiment was performed by changing the gate voltage (V_G) in order to investigate its influence on the current (I_{SD}) – voltage (V_{SD}) characteristics between the source and drain electrodes and to evaluate the response of the nano-device upon variation of V_G. Current-voltage measurement was carried out by using Keithley 2635B sourcemeter and a D.C. regulated power supply of 15V-2A. The corresponding current (I_{SD}) was measured by varying voltage (V_{SD}) in the voltage range between 0V and 10V.

RESULTS AND DISCUSSIONS

Typical I-V curves at positive gate voltage (V_G): 0V, 2V, 2V, 4V, 6V, 8V and 10V are shown in Figure 3(a) and 1(b). The entire current voltage characteristics on semi-log scale are illustrated in Figure 1(c). Figure 1(b) illustrates that the current rises steeply above a threshold voltage (V_T) following an exponential dependence. V_T is being extrapolated by fitting the different I-V characteristics for each gate voltage, by means of a straight line of constant resistance. Figure 4 displays the threshold voltage (V_T) as a function of the gate voltage (V_G), showing linear dependence on V_G.

The current at fixed V_{SD} decreases with V_G (Figure 1) as in a p-channel MOSFET. Considering the small signal equivalent circuit for a MOS transistor, we have evaluated the parameters like trance-conductance (g_m), output resistance (r_0) and the maximum voltage gain (A_V, max.) of this prototype (Table 1). The dependency of these parameters on gate voltage is sketched as follows (Figure 5).

Figure 6(a) represents the variation of output resistance with different gate voltage, which illustrates

that the output resistance increases as the forward bias voltage at the gate terminal increases. The V_G dependent transconductance and the maximum voltage gains are shown in Figure 6(b) and 3(c) respectively.

It is surprising about the source-drain current and source-drain voltage characteristics as long the gate voltage increases further. For the limitation of our power supply, it was bound to record the I_{SD} –V_{SD} characteristics in the maximum gate voltage 14V. Hence, the forward gate voltage in the interval of 1V from 10V to 14V had been applied. The characteristics I_{SD} vs. V_{SD} are illustrated in Figure 5(a). The estimated threshold voltages (V_T) for each characteristic (Figure 5(b)) astonished us about the transport

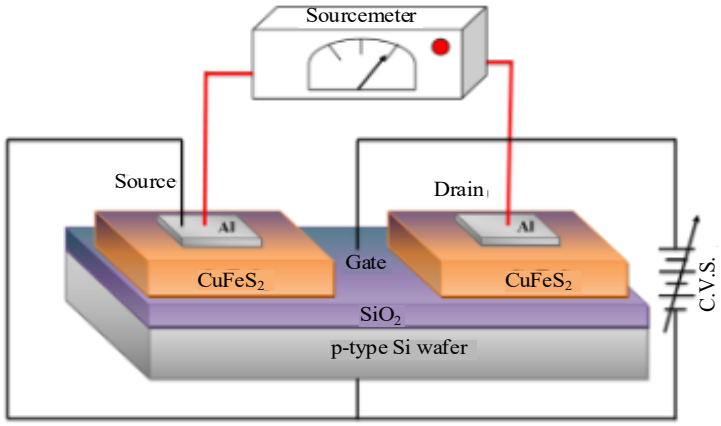

Figure 1. Configuration of the device along with biasing.

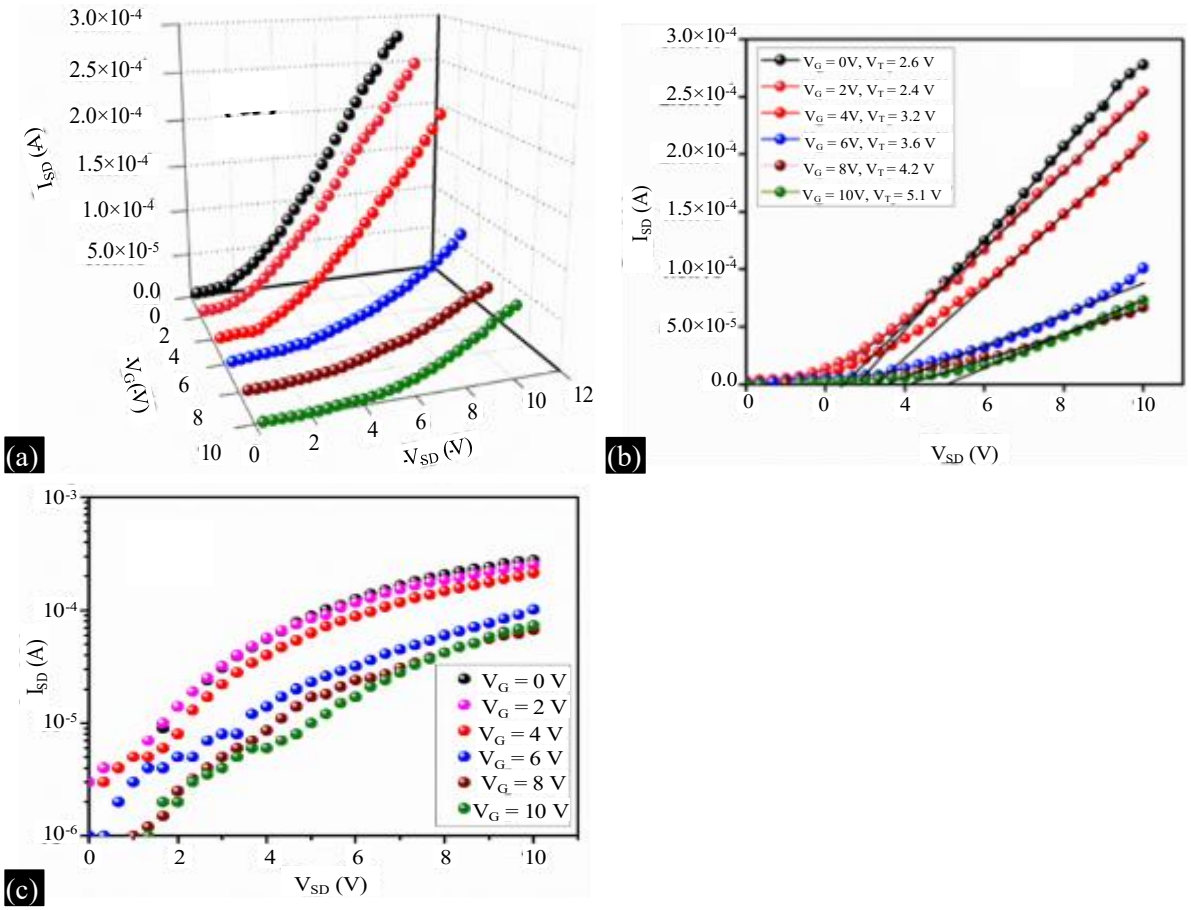

Figure 2. (a). I_{SD} vs. V_{SD} at constant V_G curves; (b): I_{SD} vs. V_{SD} characteristics for estimation of V_T; (c):

ln (I_{SD}) vs. ln (V_{SD}) plots.

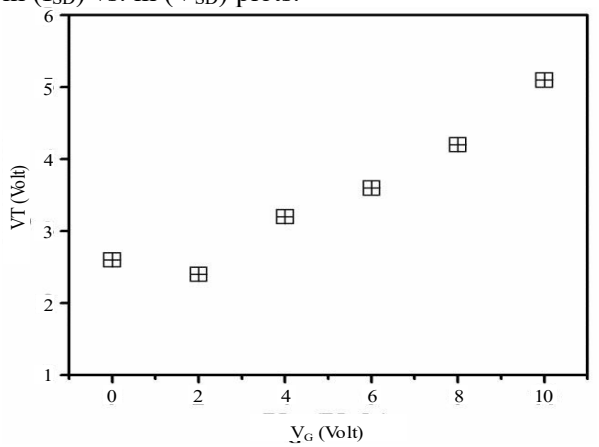

Figure 3. V_T vs V_G plot.

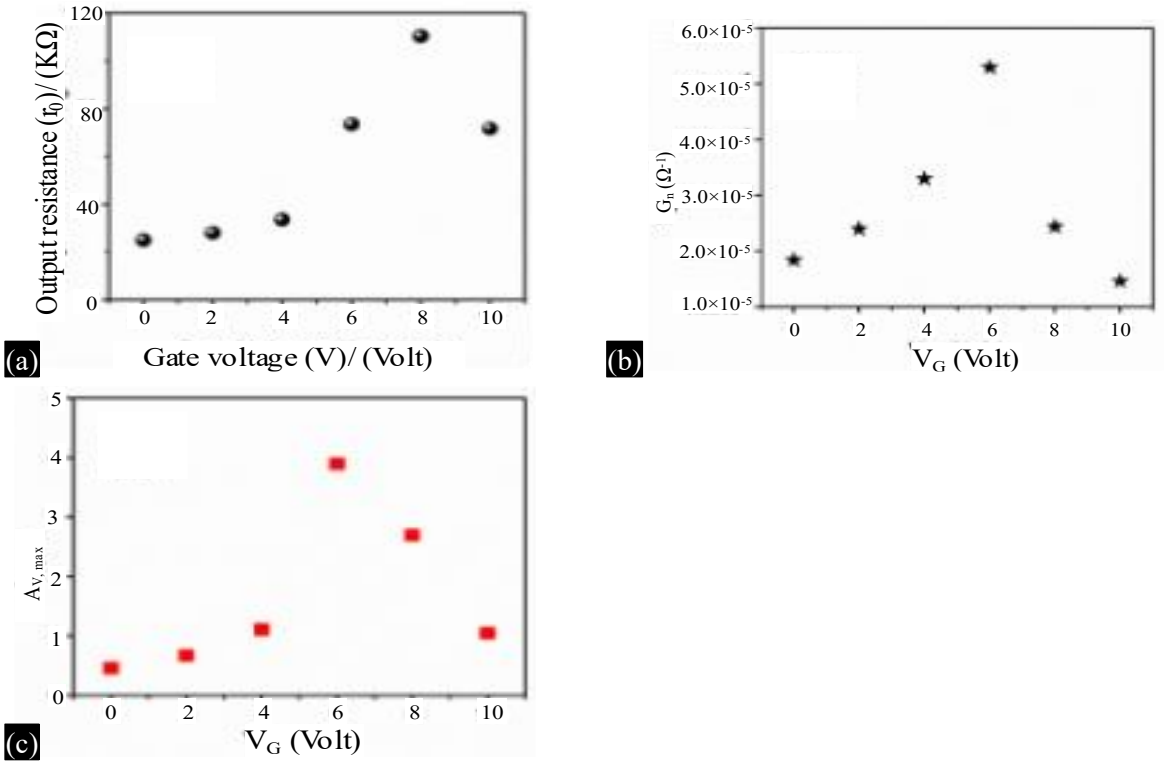

Figure 4. (a) Output resistance vs gate voltage; (b): Transconductance vs gate voltage; (c): Voltage gain vs gate voltage.

mechanism of the device structure. From the constant resistance part of the characteristics the threshold voltages were estimated by extrapolating the straight line. From this measurement it is obtained that the threshold voltage decreased as the voltage of gate terminal increased. For better analysis we have estimated tranceconductance (g_m), output resistance (r_0) and the maximum voltage gain (A_V, max.) at each gate voltage, in similar fashion. Figure 6 represents the dependency of the parameters on gate voltage.

It should be pointed out that the proposed device exhibits some surprising phenomena compared to the p-channel MOSFET. In our case the device resulting in an almost linear dependence of I_{SD} on V_G for a given $V_{SD,}$ the expected saturation of I_{SD} does not occur (Figure 7). This can be illustrated by considering the band alignment and resonant transport. In this regard, we have estimated the HOMO

and LUMO energy level of our synthesized materials as -6.97 eV and -2.93 eV by adopting electro-chemical Cyclic-Voltametry, which is reported elsewhere [8] and we have considered the conduction and valence band energy level of p-type silicon (Si) at -4.05 eV and -5.17 eV [9] respectively. In thermal equilibrium conditions the major carriers, those are moving from source to drain through the p-type Si are facing two barriers, due to insulator SiO_2, occurring at the interfaces of $CuFeS_2$ and p-type Si. Figure 8 depicts the mechanism of carrier transport through schematic band diagram. When the applied gate voltage (V_G) is zero, a resonant tunneling occurs at $V_{SD} = V_T$, due to level alignment. At $V_{SD} > V_T$, the current rectification occurs due to space charge limited current. As the applied gate potential increases,

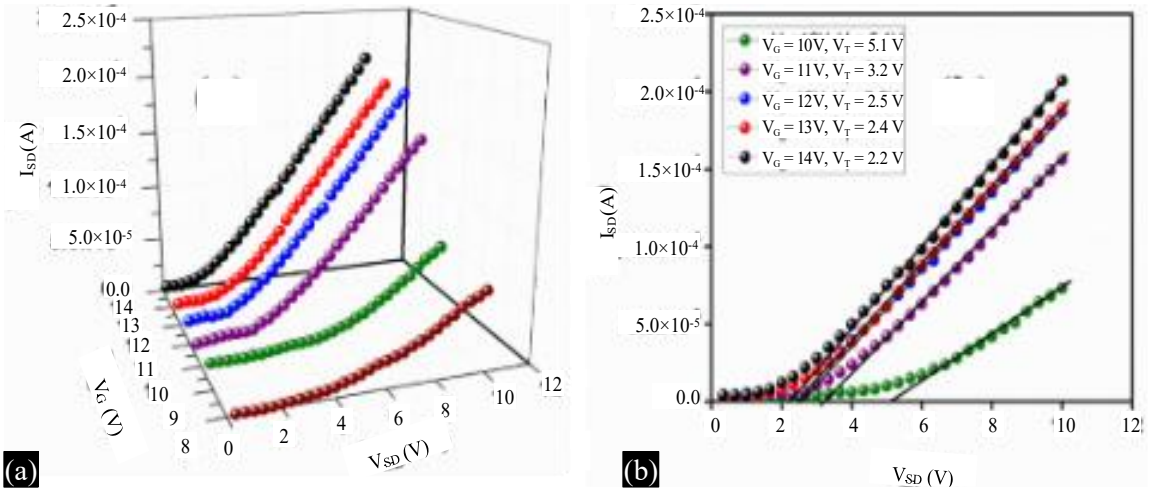

Figure 5. (a) I_{SD} vs. V_{SD} at constant V_G curves; (b): I_{SD} vs. V_{SD} characteristics for estimation of V_T.

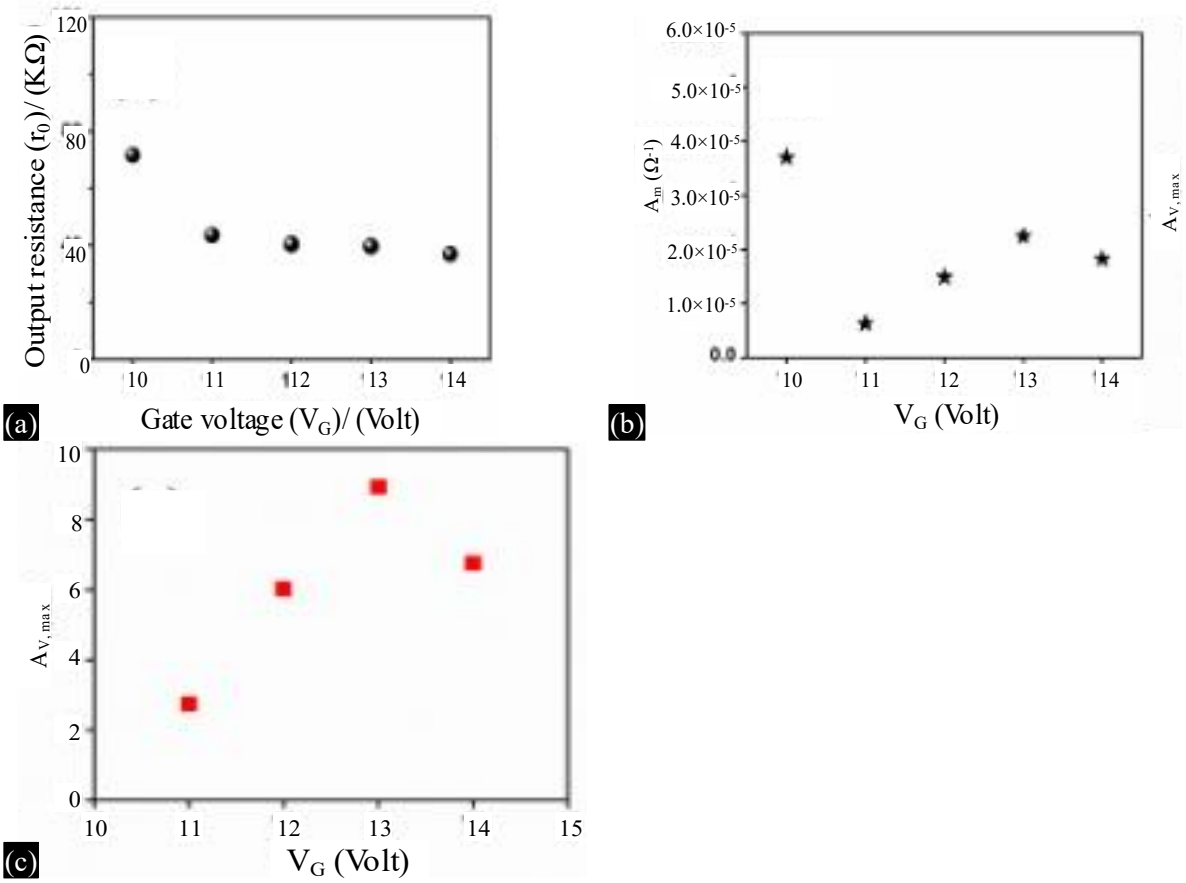

Figure 6. (a) Output resistance vs gate voltage; (b): Transconductance vs gate Voltage; (c): Voltage

gain vs gate voltage.

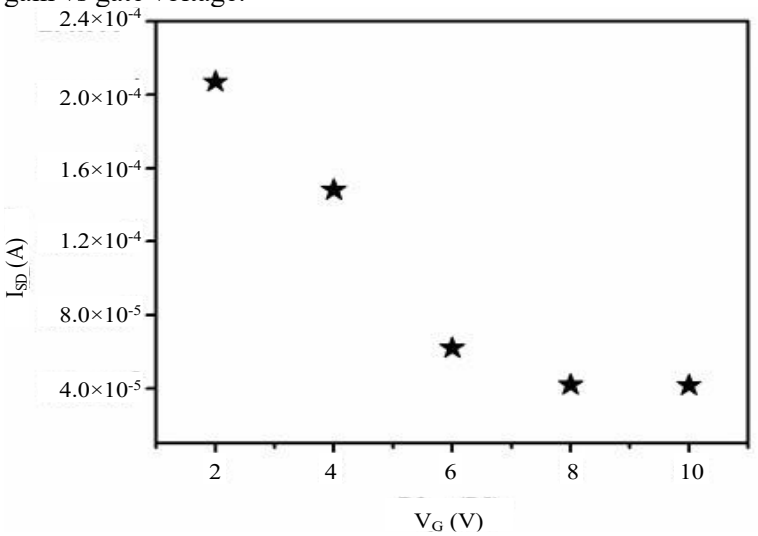

Figure 7. I_{SD} vs V_G plot.

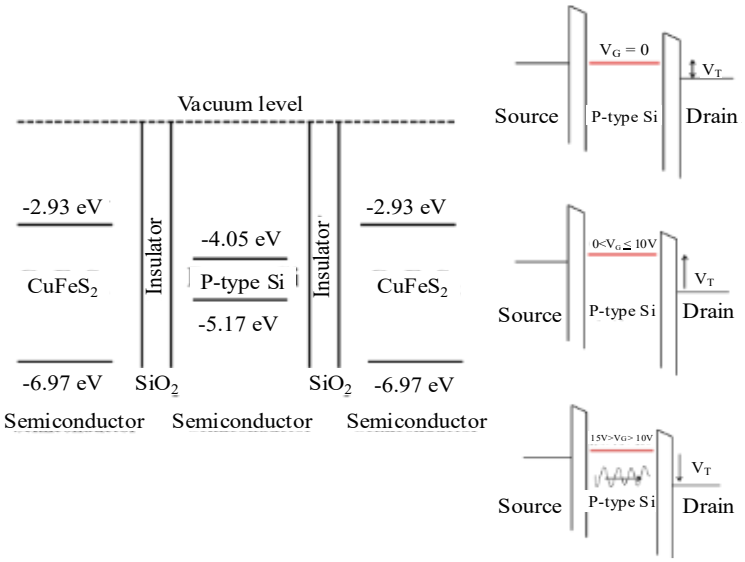

Figure 8. Schematic band diagram of carrier transport mechanism.

Table 1: Characteristic parameters of p-Si/SiO_2/$CuFeS_2$/Al prototype

V_{GS} (Volt)	V_T (Volt)	r_o (Ω)	g_m (℧)	A_v
2	2.4	28.0 x10^4	2.41 x10^{-5}	0.67
4	3.2	33.6 x10^4	3.32 x10^{-5}	1.11
6	3.6	73.5 x10^4	5.31x10^{-5}	3.89
8	4.2	110.5 x10^4	2.44 x10^{-5}	2.69
10	5.1	71.7 x10^4	3.71 x10^{-5}	1.05
11	3.1	43.6 x10^4	0.63 x10^{-5}	2.74
12	2.5	40.4 x10^4	1.49 x10^{-5}	6.02
13	2.4	39.7 x10^4	2.25 x10^{-5}	8.93
14	2.2	36.9 x10^4	1.83 x10^{-5}	6.75

there is every possibility of modification of molecular bands depending upon the magnitude of applied field. This results in the shift of V_T towards high energy level and as well as the formation of different alignment. In this case an additional energy is needed to percolate the carriers across the structure. Depending upon the field intensity the rate of recombination of carrier is highly impacted which results

in I_{SD}. In Figure 1 it is clear that the source-drain current decreased as the gate voltage was increased. When the applied field was quite high (i.e. $V_G > 10V$) the shift of V_T towards lower energy level has been observed for the device. At high V_G the source-drain current also increased. This may happen due to the production of heat during modification of molecular bands which increase the kinetic energy of the carriers to transport at ease with less amount of recombination inside the structure.

CONCLUSIONS

This report explores the newly approach of application of hydrothermally derived $CuFeS_2$ nano-semiconductor material towards fabrication of p-Si/SiO_2/$CuFeS_2$/Al based novel prototype field dependent three terminal electronic devices. Here the device was characterized only by applying bias voltages across the terminals, since the material characterization was reported elsewhere. It is observed that when the gate voltage (V_G) is just beyond the threshold voltage ($V_{GS} < V_T$) and the source to drain voltage (V_{SD}) is low, the device acts as a voltage-controlled resistor. Here, the gain increases as the gate voltage becomes more negative. The variation of gain A_v, specifically, the transconductance (g_m) of prototype upon the V_G had been noticed. That happened because the gate voltage dictates how strongly the channel conducts. The transconductance of the device directly depends on the gate-to-source voltage, dictates how much the drain current changes in response to input voltage. All these analyses conclude that the proposed prototype can be an effective potential device in semiconductor electronics and the synthesized $CuFeS_2$ will be accepted as a potential candidate for material-chemistry.

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Credit authorship contribution statement

Asmita Patra: Conceptualization, Formal analysis, Data curation, Writing - original draft, Writing - review & editing. Suman Mahata: Data curation, Formal analysis, Writing - review & editing. Animesh Layek: Funding acquisition, Conceptualization, Formal analysis, Writing - original draft, Writing - review & editing.

Conflicts of Interest

Authors whose names are listed immediately below the title of this article, certify that they have no affiliations with or involvement in any organization or entity with any financial interest (such as honoraria, educational grants, participation in speakers' bureaus, membership, employment, consultancies, stock ownership, or other equity in interest, and expert testimony or patent-licensing arrangements), or non-financial interest (such as personal or professional relationships, affiliations, knowledge or beliefs) in the subject matter or materials discussed in this manuscript.

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