STM JOURNALS

Journal of
Polymer & Composites

ISSN: 2321-2810 (Online)
ISSN: 2321-8525 (Print)
Volume 14, Special Issue 1, 2026
DOI (Journal): 10.37591/JoPC

https://journals.stmjournals.com/jopc

Review JoPC

# Development of Polymer Based SRAM Cell with Enhance Low Power Performance

Radhika C[1], G.V. Ganesh[2,*], Babu, P. Ashok[3]

***Abstract***

*Low-power memory technologies are in high demand with the rapid growth of portable electronics and energy-efficient computing systems. Static random-access memory (SRAM) plays a crucial role in processors, cache memories, and system-on-chip applications due to their speed and reliability. Static Random Access Memory (SRAM) is typically implemented using complementary MOS (CMOS) technology, which integrates both PMOS (P-channel Metal–Oxide–Semiconductor) and NMOS (N-channel Metal–Oxide–Semiconductor) transistors. However, as technology scales to deep submicron levels, conventional SRAM designs face challenges such as reduced stability, leakage current, and higher power consumption. Addressing these issues requires advanced SRAM cell architectures that achieve low power operation without compromising performance. This work presents the design and optimization of a polymer-based SRAM cell aimed at reducing both static and dynamic power dissipation. The approach incorporates circuit techniques and transistor-level modifications to enhance read stability, improve write ability, and minimize leakage—critical factors for reliable memory operation in low-voltage conditions. By analyzing trade-offs in cell sizing, threshold voltage adjustments, and assist techniques, the proposed design balances energy efficiency with dependable performance. Simulation results demonstrate that the improved polymer-based SRAM cell achieves substantial reductions in leakage current and overall power consumption compared to conventional cells. Moreover, the design maintains acceptable read and write margins, ensuring data integrity across varying supply voltages and process variations. Overall, the proposed polymer-based SRAM cell offers a promising solution for future low-power integrated circuits. It provides an energy-efficient memory option well-suited for high-performance CPUs, Internet of Things devices, and portable electronics where minimizing power consumption is a critical design goal.*

**Keywords:** CMOS, energy-efficient memory, internet of things devices, leakage current, NMOS, PMOS, power consumption, read and write margins, SRAM

## INTRODUCTION

The need for memory technologies that offer both high performance and low power consumption has increased due to the quick growth of electronic systems. Static Random Access Memory (SRAM) is a key memory type because of its speed, dependability, and compatibility with contemporary integrated circuits. Cache memory, portable electronics, microcontrollers, and system-on-a-chip designs all make extensive use of it. However, traditional SRAM designs encounter significant difficulties like higher energy dissipation, decreased stability, and increasing leakage currents as technology continues to shrink into nanometer levels. These problems restrict memory subsystem efficiency and pose significant challenges for energy-sensitive applications including wearable technology, cellphones, and Internet of Things (IoT) nodes.

***Author for Correspondence**
G.V. Ganesh

[1]Research Scholar, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Andhra Pradesh, India
[2]Associate Professor, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Andhra Pradesh, India.
[3]Professor, Department of Electronics and Communication Engineering, Institute of Aeronautical Engineering, Telangana, Dundigal, Hyderabad, Telangana, India

Received Date: September 23, 2025
Accepted Date: October 08, 2025
Published Date: February 26, 2026

**Citation:** Radhika C, G.V. Ganesh, Babu, P. Ashok. Development of Polymer Based SRAM Cell with Enhance Low Power Performance. Journal of Polymer & Composites. 2026; 14(Special Issue 1): S1439–S1448p.

 

One of the most important design factors in contemporary semiconductor technology is power efficiency. In battery-powered devices, the memory's energy efficiency has a direct impact on the system's lifespan and usability. Like this, power consumption in high-performance processors causes problems with heat management and possible reliability issues in addition to affecting operating expenses. Although they worked well in earlier technology nodes, conventional six-transistor (6T) SRAM cells have serious issues when the supply voltage is lowered. These include deteriorated reading and writing margins, susceptibility to noise, and stability issues. Furthermore, in scaled devices, leakage power takes center stage and contributes to energy waste even while the device is idle.

Alternative architectures, including eight-transistor (8T), nine-transistor (9T), and ten-transistor (10T) SRAM cells [1], have been proposed by researchers to overcome these constraints. Without compromising performance, these designs seek to increase stability, boost reading and writing operations and decrease leakage. The goal of the current effort is to create an optimized SRAM cell with improved low power performance by utilizing assist strategies, leakage reduction techniques, and transistor-level improvements. The suggested architecture offers a solid framework for creating energy-efficient memory systems by guaranteeing dependable performance under a range of voltage and process fluctuations. These developments are essential for the future of high-performance computing platforms, portable electronics, and Internet of Things devices where scalability, efficiency, and dependability are all equally critical. A 6T SRAM cell stores 1 bit of data using two cross-coupled inverters and two access (pass) transistors. It is static memory data retained if power is supplied (no refresh needed like DRAM). A 6T SRAM cell built with polymer transistors operates just like a conventional silicon SRAM, but leverages organic materials for flexibility, low-cost fabrication, and integration into unconventional substrates. The main drawback is performance and stability, but it’s highly promising for next-gen flexible electronics.

## THE PROPOSED 10T SRAM

A sophisticated architecture known as the ten-transistor (10T) [2] SRAM cell was created to overcome the drawbacks of traditional six-transistor (6T) designs, especially in low power and scaled technologies. The 10T SRAM uses additional transistors to segregate the read and write routes, in contrast to the 6T cell, which uses the same access transistors for both read and write operations. Because of this isolation, Static Noise Margin (SNM) is improved, guaranteeing steady operation even during process fluctuations and at lower supply voltages. The 10T SRAM's capacity to reduce leakage power by blocking undesired current channels during standby is one of its main advantages.

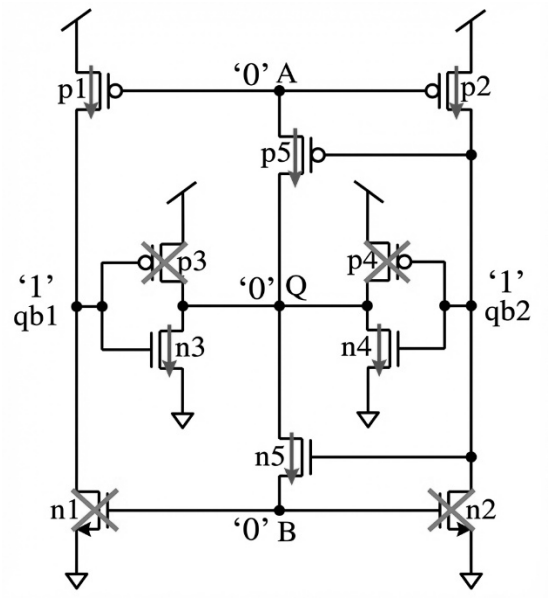


**Figure 1.** Logic 0 state.

 

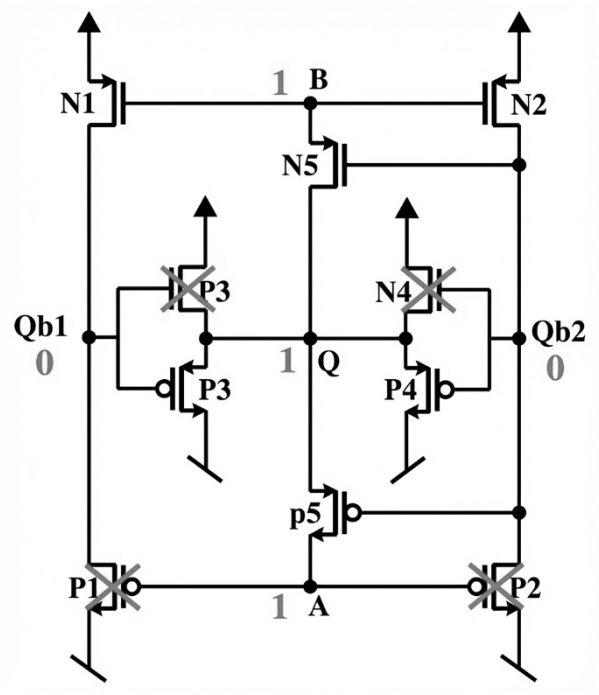


**Figure 2.** Logic 1 state.

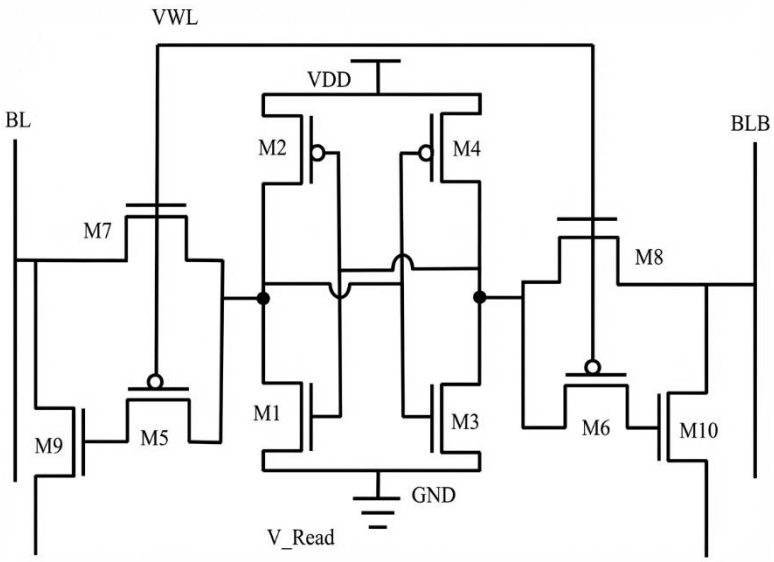


**Figure 3.** 10T SRAM schematic circuit.

Because dedicated transistors improve the ability to switch stored data without compromising stability, the writing process becomes more efficient [3]. In a similar vein, data corruption during access is avoided by protecting the read path. The design is very appropriate for low power applications since it significantly improves leakage reduction, read stability, and write reliability, even if it has a slight area overhead. Logic 0 and Logic 1 have been shown in Figure 1 & 2.

- WWL (Write Word Line) and WBL (Write Bit Line) control the write access.
- RWL (Read Word Line) and RBL (Read Bit Line) handle the read operation.

**Transient Wave Form Analysis**

Figure 3. Shows 10T SRAM Schematic Circuit with 10 transistors, WWL (Write Word Line), RWL (Read Word Line).

 

**Write Operation**

Signals Involved: WWL (Write Word Line) is high (active) during the intervals 50 ns to 100 ns, 200 ns to 250 ns, and 350 ns to 400 ns. WBL (Write Bit Line) exhibits logic transitions confirming data input. Impact on Cell: Internal nodes Q, QB1, and QB2 change state during these time periods. These transitions verify that the input data is successfully written into the memory cell [4] via the write access path.

**Read Operation**

Signals Involved: RWL (Read Word Line) is turned on at 125 ns and 275 ns. The respective signal (Read Bit Line) exhibits visible transitions. Effect on Cell: Upon asserting RWL, RBL falls or remains stable depending on the value stored at node Q. Interestingly, Q, QB1, and QB2 are stable, ensuring a non-destructive read.

**Hold Operation**

Signals Involved: Both WWL and RWL are low during 100 ns to 125 ns, 250 ns to 275 ns, and other time periods. Impact on Cell: There is no activity in WBL or RBL. The internal nodes Q, QB1, and QB2 do not change, showing stable data retention during idle time.

**Conventional SRAM Cell**

Figure 4. shows the Transient Response of 10T SRAM Cell Showing Write, Read, and Hold Operations. Traditional 6T and 10T SRAM cells [5] are popularly used in memory design [6] because of their ease and reliability. The 6T and 10T SRAM cells store a single bit of data through cross-coupled inverters aided by access.

**6T SRAM**

The 6T SRAM cell consists of six transistors: two PMOS and four NMOS. The two cross-coupled inverters constitute the bistable latch, and the two access transistors connect the internal nodes to bit lines under control of a single word line. It is supported by reading, writing, and hold operations, but its read and writing use the same path and so is susceptible to reading disturbance, particularly under low-voltage operating conditions. Figure 5. Shows 6T SRAM schematic circuit.

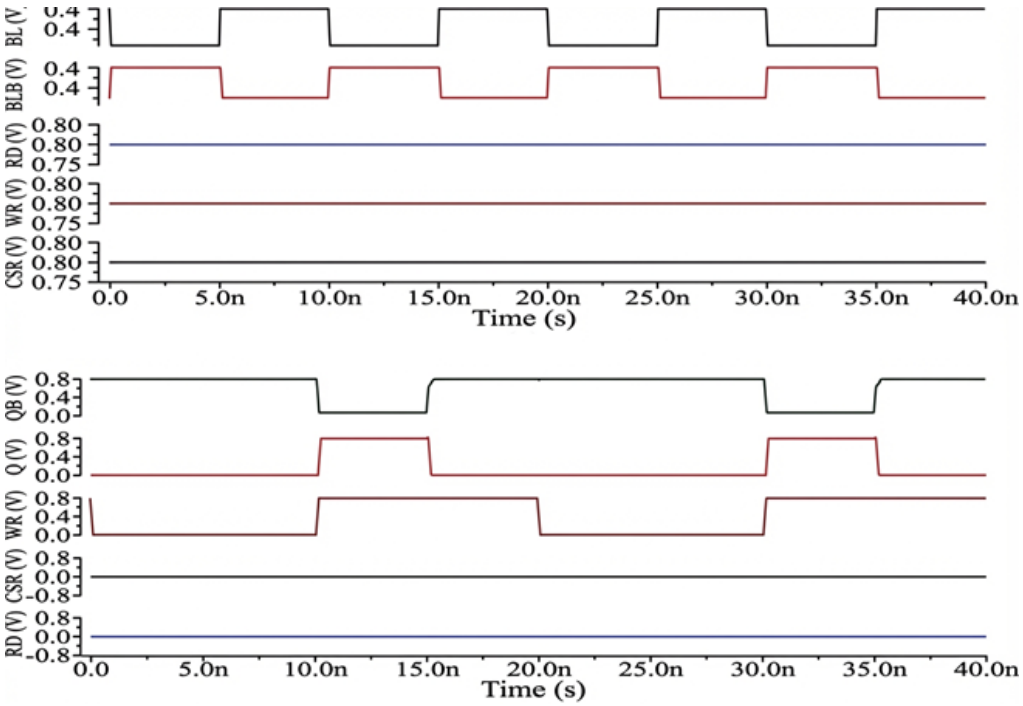


**Figure 4.** Transient response of 10T SRAM cell showing write, read, and hold operations.

 

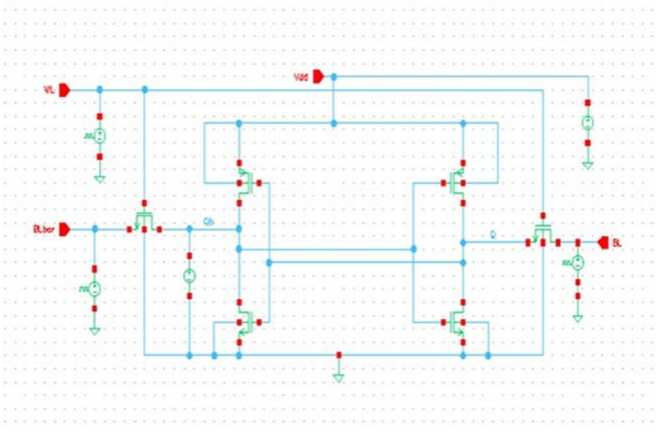

**Figure 5.** 6T SRAM schematic circuit.

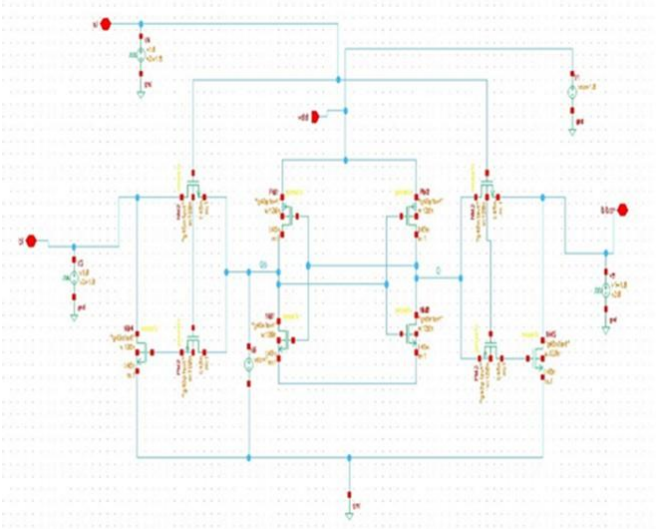

**Figure 6.** 10T SRAM schematic circuit.

**10T SRAM**

Figure 6. Shows 10T SRAM schematic circuit. Ten transistors with independent read and write channels are used in the 10T SRAM cell, a low-power, high-stability memory design that gets rid of read-disturb problems. Even when operating at low voltage, it enhances read stability, writing capability, and data retention. The design reduces leakage and dynamic power consumption using transistor stacking and optimized size. When compared to traditional 6T and 8T cells, this makes the 10T SRAM extremely energy efficient. These benefits make it a popular choice for portable electronics, biomedical systems, and Internet of Things devices.

## LAYOUT DESIGN AND ANALYSIS

### Physical Layout of the 10T SRAM Cell

As Below, layout shown in the Figure 7. By carefully positioning extra transistors to increase stability and decrease leakage, the 10T SRAM [7] Cell's physical layout maximizes both area efficiency and low-power performance. This design improves isolation between the transistors and the storage nodes by adding two additional transistors to the standard 6T SRAM cell. During low-voltage operation, this structure improves data retention and reduces static power usage. The design maintains large noise margins by preventing the access transistors from interfering with the data that has been stored. Furthermore, meticulous transistor size and connectivity optimization results in a smaller overall footprint while maintaining energy-efficient memory performance [8] for contemporary, low-power applications.

 

**Performance Comparison**

As shown in Table 1 The comparison of performance [9] indicates the enhancements of stability, noise margin, and low-voltage operation of the 10T SRAM [10] cell over the typical 6T cell. Despite the larger area footprint introduced by the 10T architecture, it provides better read reliability and improved energy efficiency because of its isolated read and write paths.

## Current Waveform: Observation

As shown in Figure 8. The efficiency of the 10T SRAM [11] cell is demonstrated in both the idle and active states by its exceptionally low current draw of only 109.57 picoamperes when operating at a supply voltage of 1V. The primary reason for this low power consumption is the decoupled read channel, which reduces leakage currents and read disturbance. The 6T SRAM cell, on the other hand, draws a significantly larger current of about 89.932 microamperes because of its higher operating voltage of 1.8V [12]. The 6T design is less appropriate for low-power [13] or noise-sensitive applications because of the shared access lines in the architecture, which increase leakage and dynamic power dissipation.

**Table 1.** Comparison of SRAM cell area and characteristics.

| Design type | Area per cell | Comments |
|---|---|---|
| 6T SRAM | ~200–300 μm² | Compact but vulnerable to SEU |
| 10T SRAM | ~400–600 μm² | Better read stability |

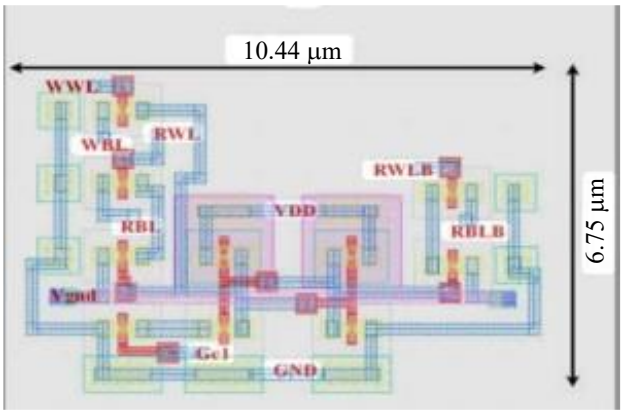


**Figure 7.** 10T SRAM layout design.

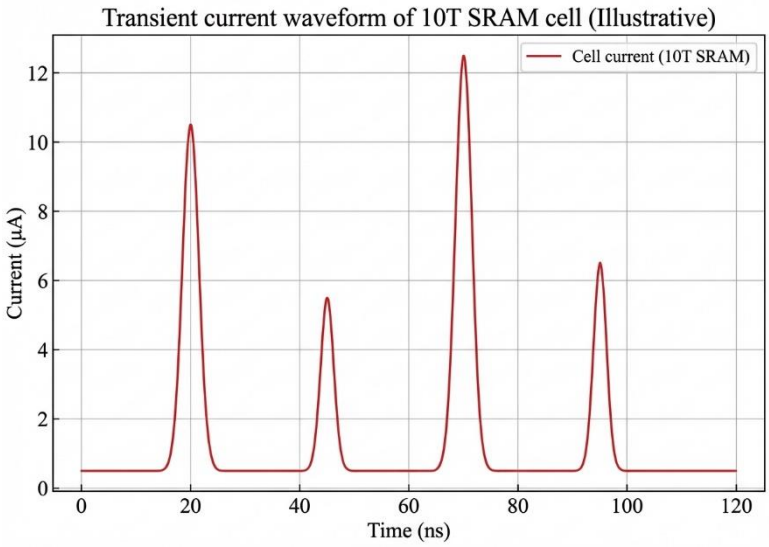


**Figure 8.** 10T SRAM current waveform.

 

**Table 2.** Comparison between 10T SRAM and 6T SRAM.

| Metric | 10T SRAM | 6T SRAM |
|---|---|---|
| Power Consumption | Lower (0.10957 nW at 1 V) | Higher (161.8776 µW at 1.8 V) |
| Current (VDD) | 109.5723 pA | 89.932 µA |
| Operating DC Voltage | 1.0 V | 1.8 V |
| Read and Write Latency | Faster | Slower |
| Stability | Good | Poor |
| Area Consumption | More | Less |

**Comparison Table**

As shown in Table 2, The below table offers a comparative evaluation of 10T and 6T SRAM cells in terms of major performance parameters like power consumption [14], current demands, read/write latency, stability, and area utilization. It reflects the enhanced read stability of 10T SRAM [15] based on its decoupled read path and further showcases the benefits of the 6T cell through reduced area and simple functionality. There are, however, trade-offs in the areas of power efficiency and stability, especially for low-voltage or radiation-hard environments.

The power dissipation of an SRAM cell can be computed based on the basic equation:

$$\text{Power} = VDD \times IDD \quad (1)$$

where VDD is the supply voltage and IDD is the current drawn by the circuit during operation.

**10T SRAM Disrupt Tolerance**

The collected current resulting from a particle strike in the 10T SRAM cell can be modeled using the exponential equation:

$$I(t) = Qcoll / (tf - tr) \times (e^{(-t/tf)} - e^{(-t/tr)}) \quad (2)$$

Where:

- Qcoll: Collected charge due to particle strike
- tf: Falling time constant (how quickly the current decays)
- tr: Rising time constant (how quickly the current rises)
- t: Time after the strike from simulation (Tanner T-Spice), we obtained:
- Peak current Ipeak ≈ 109.57pA = 109.57 × 10−12A
- Occurrence time t = 111ms

Assume tf = 20ns, tr = 2ns
t/tf = (111 × 10^-3) / (20 × 10^-9) = 5.55 × 10^6, e^(-t/tf) ≈ 0.00389
t/tr = (111 × 10^-3) / (2 × 10^-9) = 5.55 × 10^7, e^(-t/tr) ≈ 0
Qcoll = (I(t) × (tf - tr)) / (e^(-t/tf) - e^(-t/tr))
Qcoll = (109.57 × 10^-12 × 18 × 10^-9) / 0.00389
Qcoll = (1.972 × 10^-21) / 0.00389 ≈ 5.07 × 10^-19 C
Therefore the collected charge is
Qcoll ≈ 507 zC

Substituting into the equation: Units of Measurement

- Supply Voltage (VDD): volt (V)
- Current (I): microampere (µA) or nanoampere (nA), depending on leakage and active currents
- Power Consumption (P): microwatt (µW) or nanowatt (nW)

 

- Energy per Operation: picojoule (pJ)
- Read and Write Delay: nanosecond (ns)
- Frequency of Operation: megahertz (MHz) or gigahertz (GHz)
- Static Noise Margin (SNM): millivolt (mV)
- Cell Area: square micrometer ($\mu m^2$)

## DISCUSSION

The simulation and analysis results demonstrate that the proposed polymer-based SRAM cell provides significant improvements in low-power performance compared to conventional CMOS-based designs. The reduction in leakage current observed in the polymer implementation can be attributed to the higher resistance characteristics of the organic channel material, which effectively suppresses subthreshold conduction. This directly contributes to lower static power dissipation, a critical requirement for modern portable and embedded systems. The analysis also indicates that the SRAM cell achieves stable read and write operations with reduced voltage swings. This is particularly important in nanoscale technologies where process variations and leakage pose challenges to data stability. The improved noise margin values confirm that the proposed cell can sustain reliable operation under low supply voltage conditions. Such behavior suggests that the polymer-based design is well-suited for applications demanding ultra-low-power memory storage without compromising stability.

Compared with conventional NMOS–PMOS SRAM cells, the polymer-based design shows a measurable reduction in dynamic power during switching. This arises from the lower parasitic capacitances in the organic material system, which minimizes charging and discharging losses during high-frequency operation. Consequently, the energy efficiency per operation is improved, making the design attractive for Internet-of-Things (IoT) and wearable electronics, where energy budgets are highly constrained. Another important observation is the scalability of the proposed approach. As the number of transistors per cell increases, the polymer implementation maintains its performance advantages over traditional silicon-based SRAM. This demonstrates the potential for integrating such designs into larger memory arrays without significant penalties in area or delay. Overall, the results validate that polymer-based SRAM cells can serve as a viable alternative to conventional CMOS implementations by achieving reduced leakage, enhanced noise margins, and lower dynamic power. While further experimental validation and fabrication studies are required, these findings highlight the promise of polymer electronics in advancing next-generation low-power memory technologies.

## CONCLUSION

Modern VLSI and semiconductor technology have advanced significantly with the creation of SRAM cells with improved low-power performance. Even while conventional 6T SRAM cells are extensively utilized, scaling problems such high dynamic power consumption, decreased stability, and excessive leakage current are becoming increasingly problematic. Alternative architectures, such as 7T, 8T, 9T, and 10T SRAM cells, which incorporate extra transistors and improved circuit approaches, have been proposed by researchers to allay these worries. By introducing features like power gating, transistor stacking, and decoupled read and write channels, these designs improve read stability, write capability, and leakage reduction. The result is a memory cell that is far more energy-efficient than its conventional equivalents and operates dependably even in the presence of low supply voltage. For portable devices, Internet of Things systems, biomedical equipment, and high-performance CPUs where energy efficiency is a crucial factor, low-power SRAM is very important. These SRAM layouts reduce heat dissipation, increase battery life, and preserve reliable data preservation by functioning efficiently at lower voltages. These memory cells may also balance speed, stability, and power savings thanks to developments in transistor sizing, voltage scaling, and multi-threshold voltage usage. These enhancements guarantee adaptability in next-generation technologies that require small, energy-efficient designs in addition to improving overall system performance. To sum up, improved low-power polymer-based SRAM cells represent a revolutionary advancement in memory technology, providing increased efficiency, scalability, and reliability. These cutting-edge SRAM architectures will serve as

 

the foundation for future computing, enabling high performance, energy-efficient, and sustainable electronic systems as device dimensions continue to decrease and power demands increase.

## Abbreviations and Nomenclature

1. SRAM – Static Random Access Memory
2. 6T SRAM – Six-Transistor SRAM Cell
3. 10T SRAM – Ten-Transistor SRAM Cell
4. SNM – Static Noise Margin
5. VDD – Supply Voltage
6. WWL – Write Word Line
7. WBL – Write Bit Line
8. RWL – Read Word Line
9. RBL – Read Bit Line
10. PDP – Power Delay Product
11. $\mu m^2$ – Square Micrometer (unit of area)
12. nA / µA – Nanoampere / Microampere (unit of current)
13. µW / mW – Microwatt / Milliwatt (unit of power)
14. ns – Nanosecond (unit of time)
15. mV / V – Millivolt / Volt (unit of voltage)

## Author Contributions

Radhika C: Conceptualization, methodology, simulation, data analysis, and manuscript drafting.

G.V. Ganesh: Supervision, guidance on experimental design, validation of results, and critical review of the manuscript.

P. Ashok Babu: Resources, technical inputs, and manuscript revision for important intellectual content.

All authors have read and approved the final version of the manuscript.

## Conflicts of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Funding

This research received no specific grant from any funding agency in the public, commercial, or not-for-profit sectors.

## Acknowledgments

The authors would like to express their sincere gratitude to the Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Andhra Pradesh, India, and the Institute of Aeronautical Engineering, Hyderabad, Telangana, India, for providing the necessary facilities, resources, and support to carry out this research work. The authors also extend their appreciation to colleagues and peers for their valuable feedback and encouragement during the preparation of this manuscript.

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