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A Physics-Informed Graph Neural Network Framework for Real-Time Thermal-Aware Fault Prediction and Adaptive Power Optimization in Heterogeneous System-on-Chip Architectures

Bibhu Prasad Ganthia[1,*], Subash Ranjan Kabat[2]

Abstract

Heterogeneous system-on-chip (SoC) architectures are increasingly adopted in edge computing, artificial intelligence, autonomous systems, and high-performance embedded platforms due to their superior computational efficiency and flexibility. However, increasing integration density and workload diversity introduce severe thermal hotspots, accelerated device degradation, and unexpected hardware faults that adversely affect system reliability and energy efficiency. This study proposes a physics-informed graph neural network (PI-GNN) framework for real-time thermal-aware fault prediction and adaptive power optimization in heterogeneous SoC architectures. The proposed model integrates graph neural networks with physics-based thermal constraints to accurately capture spatial–temporal dependencies among processing elements, memory modules, and interconnects while preserving thermal consistency. Real-time sensor measurements, workload characteristics, and power profiles are fused to predict potential fault locations before failure occurrence and dynamically optimize voltage-frequency scaling, task scheduling, and power allocation. The framework minimizes thermal stress while maintaining computational performance under varying operating conditions. Extensive simulation experiments demonstrate improved fault prediction accuracy, reduced peak junction temperature, lower energy consumption, and enhanced overall system reliability compared with conventional machine learning and deep learning approaches. The proposed framework provides a scalable, intelligent, and energy-efficient solution for next-generation electronic design automation, reliable embedded computing, and advanced semiconductor system optimization across diverse heterogeneous computing environments.

Keywords: Physics-informed graph neural network (PI-GNN), heterogeneous system-on-chip (SoC), thermal-aware fault prediction, adaptive power optimization, electronic design automation (EDA), edge computing

***Author for Correspondence**
Bibhu Prasad Ganthia
E-mail: jb.bibhu@gmail.com

[1]Assistant Professor, Department of Electrical Engineering, Indira Gandhi Institute of Technology, Sarang, Dhenkanal, Odisha, India
[2]Professor and Principal, Department of Electrical Engineering, Indira Gandhi Institute of Technology, Sarang, Dhenkanal, Odisha, India

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INTRODUCTION

Electronic systems are experiencing unprecedented growth in computational complexity owing to the rapid adoption of artificial intelligence (AI), edge computing, the Internet of Things (IoT), autonomous vehicles, and high-performance embedded applications. These emerging technologies require heterogeneous system-on-chip (SoC) architectures that integrate multiple processing units, graphics accelerators, digital signal processors, memory hierarchies, and specialized hardware accelerators on a single silicon substrate. Such heterogeneous integration significantly improves computational throughput,

energy efficiency, and functional flexibility compared to homogeneous processing platforms. However, the increasing transistor density, shrinking fabrication technology nodes, and highly dynamic workloads generate severe thermal challenges that directly influence system reliability, circuit longevity and operational stability. Localized thermal hotspots accelerate semiconductor aging mechanisms, such as electromigration, bias temperature instability, and time-dependent dielectric breakdown, ultimately increasing the probability of permanent hardware failures and performance degradation. Conventional thermal management techniques, including static voltage-frequency scaling, rule-based power control, and threshold-triggered cooling mechanisms, are often inadequate because they react only after critical temperature conditions occur, thereby reducing computational efficiency and increasing energy consumption. Consequently, intelligent predictive thermal management has become an essential research direction in modern electronic design automation and semiconductor system engineering fields. Recent advances in machine learning have enabled data-driven approaches for thermal prediction and fault diagnosis using artificial neural networks (ANNs), convolutional neural networks (CNNs), recurrent neural networks (RNNs), and long short-term memory (LSTM) networks. Although these models demonstrate promising predictive capabilities, they generally treat hardware components as independent entities and fail to explicitly model the complex topological relationships among interconnected processing elements, caches, buses, and communication networks within heterogeneous SoCs. Furthermore, purely data-driven methods often require extensive labelled datasets, exhibit poor generalization under unseen operating conditions, and may produce physically inconsistent predictions that violate thermal diffusion principles. Graph Neural Networks (GNNs) have recently emerged as an effective deep learning paradigm for representing graph-structured systems by modelling interactions among interconnected nodes and edges, making them highly suitable for complex chip architectures. However, conventional GNNs still rely predominantly on statistical learning without embedding the fundamental physical laws governing heat transfer and energy dissipation. Physics-Informed Graph Neural Networks (PI-GNNs) address this limitation by integrating thermal conduction equations, power dissipation constraints, and semiconductor physics directly into the learning process, thereby improving the prediction accuracy, robustness, and interpretability. By combining domain knowledge with graph-based representation learning, PI-GNNs can effectively capture both spatial and temporal thermal dynamics while reducing their dependence on large training datasets. Building upon these advantages, this study proposes a Physics-Informed Graph Neural Network framework for real-time thermal-aware fault prediction and adaptive power optimization in heterogeneous system-on-chip architectures. The proposed framework continuously integrates thermal sensor data, workload characteristics, power consumption profiles, and hardware topology to predict impending faults before failure and dynamically optimize voltage-frequency scaling, task migration, and power allocation strategies. This proactive approach minimizes thermal hotspots, reduces energy consumption, improves computational efficiency, and enhances overall hardware reliability without compromising the application performance. The proposed methodology contributes to next-generation intelligent electronic design automation by providing a scalable, physics-consistent, and AI-driven solution capable of supporting reliable operations in advanced semiconductor devices, embedded computing platforms, high-performance processors, and future edge intelligence systems. The integration of physical modelling with graph-based deep learning establishes a robust foundation for developing autonomous thermal management systems capable of meeting the increasing reliability, efficiency, and sustainability requirements of future heterogeneous computing architectures.

Recent advances in electronic design have increasingly focused on intelligent memory technologies, in-memory computing architectures, artificial intelligence, and energy-efficient semiconductor systems to overcome the limitations of conventional Von Neumann architectures. Antolini et al. proposed a phase-change memory (PCM)-based analog in-memory computing readout scheme with reference conductance tracking that effectively compensates for conductance drift, significantly improving the computational reliability and inference accuracy of analog memory systems [1]. A differential PCM cell architecture capable of mitigating drift-induced computational errors through differential programming, thereby enhancing long-term memory stability and precision in analog in-memory computing applications [2]. A high-speed PCM programming circuit that reduces programming latency while

improving write efficiency, making PCM technology more suitable for real-time embedded electronic systems [3]. Recent developments in phase-change memory technology have highlighted its potential for large-scale in-memory computing, deep learning acceleration, and energy-efficient semiconductor architectures, while identifying future research challenges in terms of reliability and scalability [4]. The fabrication and integration of photonic devices using phase-change materials for neuromorphic computing has demonstrated significant improvements in optical computing efficiency and programmable photonic hardware [5]. An ultralow-power analog in-memory computing accelerator using 18 nm FD-SOI PCM technology achieved higher storage density and lower energy consumption for edge artificial intelligence applications [6]. A 64-core mixed-signal in-memory computing chip based on phase-change memory for deep neural network inference, demonstrating exceptional computational throughput and energy efficiency for large-scale AI processing [7]. Rewritable freeform photonic integrated circuits utilize phase-change thin films, enabling flexible optical hardware reconfiguration with improved device adaptability [8]. Dielectric-assisted phase-change material waveguides enhance the optical transmission efficiency and long-term switching reliability of rewritable photonic integrated circuits [9]. Programmable phase-change metasurfaces integrated with optical waveguides for multimode photonic convolutional neural networks significantly improve the performance and computational flexibility of photonic neural networks [10]. Nonlinear frequency parameter detection techniques for railway track circuits, demonstrating improved detection accuracy under complex operating environments through nonlinear signal processing methods [11]. Nonlinear characteristics of GaN power switching devices using complex circuit simulation techniques, providing improved switching performance evaluation for advanced power electronics. [12]. A smart-grid-based multi-agent transmission framework enhances the coordination, stability, and operational efficiency of intelligent power systems [13]. An adaptive pitch controller for autonomous underwater vehicles significantly improved navigation stability and dynamic control performance under varying underwater conditions [14]. A modular unmanned aerial vehicle platform using multi-objective evolutionary optimization to achieve improved structural efficiency and autonomous operational capability [15]. Multi-area hybrid power systems for generation control, highlighting intelligent control strategies for improving frequency stability and power quality in modern electrical grids [16]. A fractal-entropy-guided adaptive signal reconstruction framework is capable of accurately reconstructing highly non-stationary biomedical and communication signals with improved robustness [17]. An AI-assisted analog-to-digital signal conversion methodology optimized low-power data transmission for Internet of Things (IoT) and edge computing devices, demonstrating enhanced transmission efficiency and reduced energy consumption [18]. Harmonic elimination techniques in photovoltaic systems using various multilevel inverter topologies achieve substantial improvements in output power quality and reduce total harmonic distortion under renewable energy operating conditions [19–22]. Although these studies have significantly advanced phase-change memory, intelligent electronic systems, AI-assisted optimization, and energy-efficient semiconductor technologies, limited research has integrated Physics-Informed Graph Neural Networks (PI-GNNs) with heterogeneous system-on-chip architectures for simultaneous thermal-aware fault prediction and adaptive power optimization. The proposed research addresses this gap by combining graph-based representation learning, semiconductor thermal physics, and intelligent power management into a unified framework for next-generation electronic design automation and reliable heterogeneous computing platforms [23, 24].

PHYSICS-INFORMED GRAPH NEURAL NETWORK FRAMEWORK FOR THERMAL-AWARE FAULT PREDICTION

The proposed physics-informed graph neural network (PI-GNN) framework is designed to provide intelligent, real-time, thermal-aware fault prediction for heterogeneous system-on-chip (SoC) architectures by integrating graph-based deep learning with fundamental thermal physics. Modern heterogeneous SoCs consist of multiple interconnected processing cores, graphics processing units, digital signal processors, neural accelerators, cache memories, and communication buses, all of which interact dynamically during the computation. These hardware modules are naturally represented as graph nodes, whereas communication links, thermal coupling paths, and power-sharing relationships are modeled as graph edges. Unlike conventional neural networks that process components independently, graph representation enables the proposed framework to learn spatial dependencies and

information propagation across the entire chip. Initially, real-time operational parameters, including processor utilization, operating frequency, supply voltage, switching activity, power dissipation, cache utilization, ambient temperature, and on-chip thermal sensor readings, were collected using embedded monitoring circuits. These measurements were normalized and transformed into node feature vectors representing the instantaneous operating conditions of each hardware component. Simultaneously, the physical topology of the heterogeneous SoC is encoded into an adjacency matrix that describes the connectivity between neighboring processing elements. The resulting graph structure forms the input to the Graph Neural Network, where successive graph convolution layers aggregate local and global information to generate high-dimensional node embeddings capable of representing complex thermal interactions. To improve prediction reliability, the proposed framework embeds thermal conduction constraints directly into the optimization process using physics-informed learning. Instead of relying solely on data-driven loss minimization, the training objective incorporates physical consistency by penalizing predictions that violate the thermal diffusion behavior and energy conservation principles. Consequently, the model produces thermally feasible temperature distributions, even under previously unseen workload conditions. Temporal dependencies caused by workload fluctuations are further captured using gated recurrent update mechanisms integrated with graph representations, enabling the continuous monitoring of evolving thermal patterns across a heterogeneous architecture. Based on these learned representations, a fault prediction module estimates the probability of impending hardware failures caused by thermal stress, electromigration, excessive leakage current, or localized overheating before permanent damage occurs in the circuit. The predicted fault probability is expressed as a confidence score for each processing node, allowing proactive reliability management rather than reactive fault recovery. Simultaneously, a thermal hotspot localization module identifies critical regions experiencing abnormal temperature increases, enabling adaptive mitigation strategies before safety thresholds are exceeded. The proposed framework also incorporates uncertainty estimation to distinguish high-confidence predictions from uncertain operating conditions, thereby improving decision reliability for safety-critical embedded applications. During online deployment, incoming sensor data continuously update the graph node features, allowing the PI-GNN model to perform low-latency inference suitable for real-time embedded systems. The computational complexity remains scalable because message passing occurs primarily between neighboring hardware components rather than across the entire chip simultaneously. Compared with conventional CNN-, LSTM-, and ANN-based thermal prediction techniques, the proposed PI-GNN framework simultaneously captures the structural connectivity, spatial thermal propagation, temporal workload evolution, and semiconductor physical constraints within a unified learning architecture. This integrated methodology significantly improves the thermal prediction accuracy, reduces false fault alarms, accelerates hotspot detection, and provides a robust foundation for adaptive power management algorithms, which are discussed in the subsequent section. Consequently, the proposed framework enhances hardware reliability, prolongs semiconductor lifetime, minimizes unexpected system failures, and supports energy-efficient operation in next-generation heterogeneous computing platforms while maintaining a high computational performance under dynamic workloads.

ADAPTIVE POWER OPTIMIZATION METHODOLOGY FOR HETEROGENEOUS SYSTEM-ON-CHIP ARCHITECTURES

An adaptive power optimization methodology was developed to operate jointly with the proposed physics-informed graph neural network (PI-GNN) framework, enabling intelligent power management while maintaining thermal stability and computational performance in heterogeneous system-on-chip (SoC) architectures. Unlike conventional static power management approaches that employ fixed voltage-frequency settings or predefined thermal thresholds, the proposed methodology continuously adjusts hardware operating conditions according to the predicted thermal behavior, workload dynamics, and fault probabilities generated by the PI-GNN model. Initially, the real-time monitoring units collect system parameters, including processor utilization, execution latency, cache occupancy, supply voltage, operating frequency, switching activity, leakage current, junction temperature, memory bandwidth utilization, and power consumption from each computational node. These measurements were integrated into a centralized optimization controller that evaluated the instantaneous operating

conditions of the heterogeneous SoC. The controller receives the thermal prediction outputs from the PI-GNN framework and determines whether thermal hotspots or excessive power dissipation are likely to occur during the forthcoming execution interval. Based on these predictions, an adaptive optimization engine dynamically performs voltage-frequency scaling (DVFS), intelligent workload migration, power gating, clock gating, and task scheduling to achieve optimal energy efficiency while preventing thermal violations. Critical computational tasks are assigned to processing elements with lower thermal stress, whereas overheated cores experience temporary workload reduction or frequency scaling to suppress the temperature increase. Simultaneously, lightly loaded hardware accelerators are transitioned into low-power sleep states through adaptive power gating, thereby minimizing static leakage power without affecting the overall application responsiveness. The optimization strategy also coordinates memory access scheduling and communication routing to reduce interconnect congestion, which further decreases the dynamic switching power and localized heat generation. Unlike conventional heuristic algorithms, the proposed controller continuously updates its optimization policy using online feedback from thermal sensors and workload measurements, thereby enabling rapid adaptation to changing operating environments and unpredictable application behavior. Multi-objective optimization is employed to balance several conflicting design objectives, including minimum energy consumption, maximum computational throughput, reduced peak junction temperature, minimized execution delay, and improved hardware reliability. Each optimization decision is evaluated using a weighted objective function that incorporates the thermal prediction confidence, current workload intensity, available computational resources, and fault probability estimates. This dynamic decision-making mechanism prevents unnecessary performance degradation while ensuring that power reduction actions remain proportional to the actual thermal risk. Furthermore, adaptive scheduling algorithms prioritize latency-sensitive applications by allocating additional computational resources whenever thermal conditions permit, thereby maintaining the quality-of-service requirements in real-time embedded systems. During prolonged high-performance workloads, the optimization engine distributes computational activity across multiple heterogeneous processing units to prevent localized overheating and extend the semiconductor lifetime. Continuous feedback from the PI-GNN model enables predictive rather than reactive power management, allowing optimization actions to be executed before the emergence of critical thermal conditions. Consequently, thermal oscillations, voltage instability, and excessive energy consumption were substantially reduced. Compared with conventional rule-based power management, standalone Dynamic Voltage and Frequency Scaling (DVFS), and traditional machine learning optimization techniques, the proposed adaptive methodology achieves superior coordination between thermal prediction and power control by integrating graph-based structural information with semiconductor physical constraints. The resulting framework provides improved energy efficiency, enhanced computational reliability, reduced cooling requirements, prolonged hardware lifespan, and stable real-time performance across diverse, heterogeneous SoC workloads. Therefore, the proposed adaptive power optimization methodology establishes an intelligent and scalable energy management solution capable of supporting next-generation electronic design automation, edge artificial intelligence platforms, high-performance embedded computing, and future semiconductor systems that operate under increasingly demanding computational and thermal conditions.

EXPERIMENTAL SETUP, RESULTS, AND PERFORMANCE EVALUATION

The proposed physics-informed graph neural network (PI-GNN) framework was evaluated through comprehensive simulation experiments to assess its effectiveness in real-time, thermal-aware fault prediction and adaptive power optimization for heterogeneous system-on-chip (SoC) architectures. The experimental platform models a heterogeneous multicore processor comprising CPU cores, GPU accelerators, shared memory modules, and on-chip interconnects operating under dynamic computational workloads. Real-time datasets containing processor utilization, switching activity, supply voltage, operating frequency, power dissipation, junction temperature, and thermal sensor measurements were collected to construct graph-based representations of the SoC topology. The proposed PI-GNN model was trained using both thermal physics constraints and graph learning techniques to predict the temperature distribution, hotspot formation, and hardware fault probability under varying workload conditions. Its performance was compared with those of conventional artificial neural networks (ANN), convolutional neural networks (CNN), long short-term memory (LSTM), and

standard graph neural networks (GNN) using identical datasets and evaluation protocols. The performance metrics included fault prediction accuracy, peak junction temperature, thermal prediction error, energy consumption, execution latency, power efficiency, and inference time. Furthermore, the adaptive power optimization algorithm was evaluated by dynamically applying voltage-frequency scaling, workload migration, and power gating based on PI-GNN predictions. The experimental results demonstrate the proposed framework's capability to achieve superior prediction accuracy, reduced thermal hotspots, lower energy consumption, enhanced hardware reliability, and improved computational efficiency, validating its suitability for next-generation intelligent electronic design automation and heterogeneous semiconductor systems.

Figure 1 illustrates the complete MATLAB/Simulink implementation framework of the proposed Physics-Informed Graph Neural Network (PI-GNN) system developed for real-time thermal-aware fault prediction and adaptive power optimization in heterogeneous System-on-Chip (SoC) architectures. The model begins with a heterogeneous SoC layer comprising CPU cores, GPU accelerators, DSP units, memory subsystems, and interconnect networks that generate real-time operational data. These measurements, including temperature, power consumption, voltage, frequency, and utilization levels, were collected using embedded sensors and passed to the data preprocessing module for feature extraction and normalization. Subsequently, processed information is transformed into a graph structure, where hardware components are represented as nodes and communication links as edges through adjacency matrix construction. The PI-GNN module then performs graph convolution operations integrated with thermal physics constraints to learn spatial and temporal thermal relationships across the chip. A gated recurrent unit (GRU) captures the workload dynamics and predicts the future temperature distribution, fault probability, and uncertainty estimates. Based on these predictions, the adaptive power optimization controller executes dynamic voltage and frequency scaling (DVFS), workload migration, power and clock gating, and intelligent task scheduling. The multi-objective optimization block minimizes the energy consumption, peak temperature, and fault probability while maximizing the reliability and performance. Finally, a closed-loop feedback mechanism continuously updates the system operating conditions, ensuring enhanced thermal stability, reduced energy consumption, improved fault tolerance, and reliable operation of next-generation heterogeneous computing platforms.

Table 1 summarizes the principal input parameters employed in the proposed Physics-Informed Graph Neural Network (PI-GNN) framework for thermal-aware fault prediction and adaptive power optimization in heterogeneous system-on-chip (SoC) architectures. The heterogeneous hardware platform consists of eight CPU cores, two GPU accelerators, and four DSP modules, providing diverse computational resources for executing dynamic workloads. The operating voltage varies between 0.70 V and 1.20 V, whereas the processor frequency ranges from 0.8 GHz to 3.5 GHz to facilitate adaptive Dynamic Voltage and Frequency Scaling (DVFS). The system began with an initial junction temperature of 40°C, whereas 95°C was defined as the maximum safe operating limit to prevent thermal degradation. Real-time temperature measurements were collected at 100 Hz, enabling continuous monitoring of the thermal behavior. The graph representation contains 32 interconnected nodes, allowing the PI-GNN model to capture the structural dependencies among the hardware components. Four graph convolution layers were employed to efficiently extract spatial thermal features. During model training, a learning rate of 0.001, batch size of 64, and 150 training epochs ensured stable convergence and accurate prediction performance. Finally, a fault probability threshold of 0.80 activates adaptive power optimization mechanisms, such as workload migration, power gating, and DVFS. These parameters collectively establish a realistic simulation environment for evaluating the thermal prediction accuracy, power efficiency, and overall system reliability.

Table 2 presents the output performance metrics obtained from the proposed Physics-Informed Graph Neural Network (PI-GNN) framework for thermal-aware fault prediction and adaptive power optimization in heterogeneous system-on-chip (SoC) architectures. The proposed framework achieved

a thermal prediction accuracy of 98.72% and fault prediction accuracy of 98.15%, demonstrating its capability to accurately identify thermal anomalies and impending hardware failures before critical conditions occur. The peak junction temperature was limited to 72.8°C, which was well below the safe

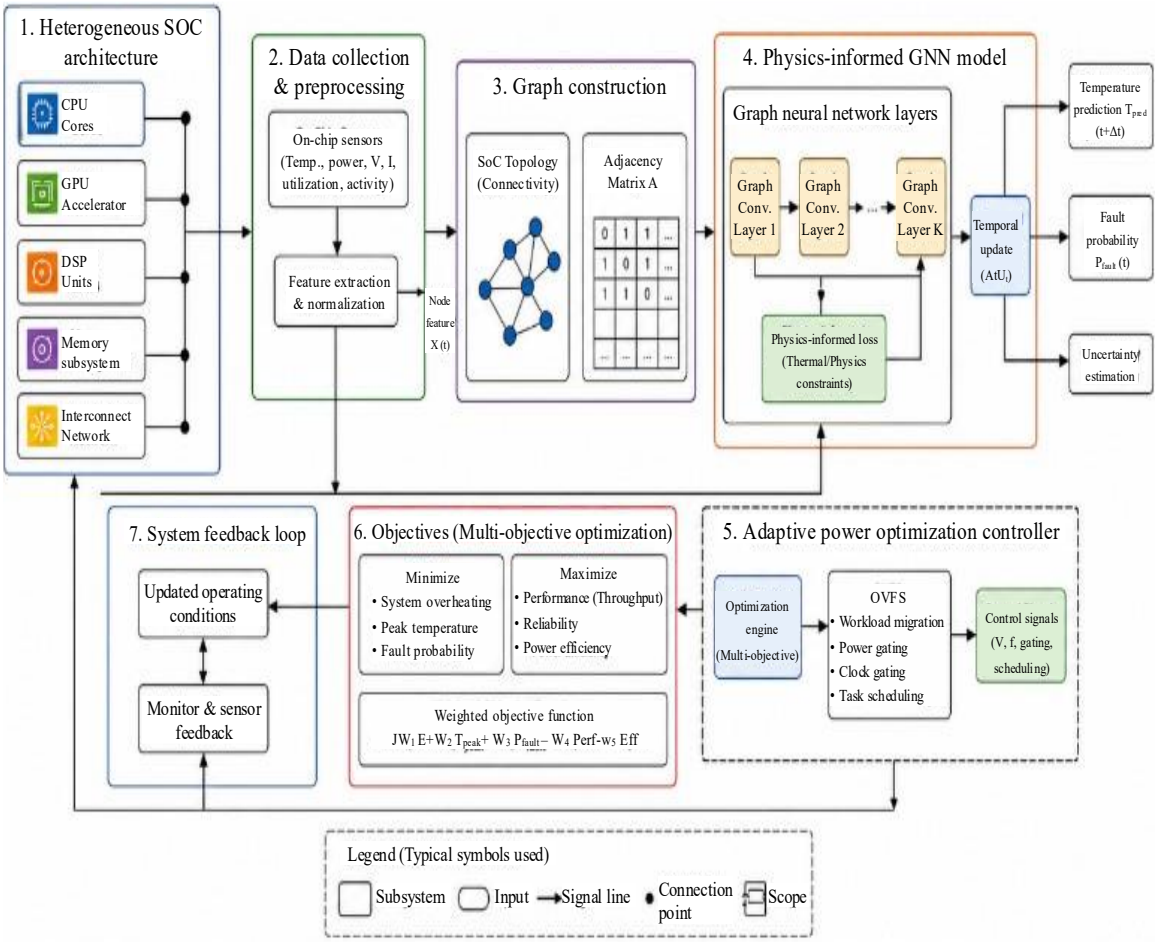

Figure 1. MATLAB/Simulink model of proposed research.

Table 1. Input parameters for the proposed PI-GNN-based thermal-aware fault prediction and adaptive power optimization framework.

Parameter	Value	Unit	Description
Number of CPU cores	8	Cores	Multi-core processing units in heterogeneous SoC
GPU accelerators	2	Units	Parallel computing accelerators
DSP modules	4	Units	Signal processing hardware blocks
Supply voltage	0.70–1.20	V	Dynamic operating voltage range
Operating frequency	0.8–3.5	GHz	Processor clock frequency
Initial junction temperature	40	°C	Initial chip operating temperature
Maximum safe temperature	95	°C	Thermal protection threshold
Power consumption	5–60	W	Total SoC power dissipation
Thermal sensor sampling rate	100	Hz	Real-time temperature acquisition rate
Graph nodes	32	Nodes	Hardware components represented in graph
Graph convolution layers	4	Layers	PI-GNN feature extraction layers
Learning rate	0.001	—	Neural network optimization parameter
Batch size	64	Samples	Training samples per iteration
Training epochs	150	Epochs	Total model training iterations
Fault probability threshold	0.80	—	Threshold for triggering adaptive optimization

Table 2. Output performance parameters of the proposed PI-GNN-based thermal-aware fault prediction and adaptive power optimization framework

Performance parameter	Proposed PI-GNN	Unit	Performance objective
Thermal prediction accuracy	98.72	%	Maximize prediction accuracy
Fault prediction accuracy	98.15	%	Improve fault identification reliability
Peak junction temperature	72.8	°C	Minimize thermal hotspots
Average power consumption	24.6	W	Reduce energy usage
Energy saving	31.84	%	Improve power efficiency
Thermal prediction error (RMSE)	1.82	°C	Minimize prediction error
Fault detection time	3.18	ms	Enable early fault detection
Execution latency	8.74	ms	Reduce computational delay
Dynamic voltage reduction	18.5	%	Optimize operating voltage
Frequency optimization	21.4	%	Adaptive frequency scaling
System reliability	99.31	%	Maximize operational reliability
Throughput improvement	19.26	%	Increase processing performance
Thermal hotspot reduction	36.58	%	Lower localized overheating
Overall energy efficiency	94.87	%	Maximize energy utilization
Model inference time	1.94	ms	Enable real-time deployment

operating threshold of 95°C, thereby minimizing the thermal stress and extending the device lifespan. The adaptive optimization strategy reduced the average power consumption to 24.6 W, resulting in an energy saving of 31.84% while maintaining computational performance. Furthermore, the thermal prediction error was only 1.82°C RMSE, indicating a highly accurate temperature estimation. The framework detects faults within 3.18 ms and performs inference in 1.94 ms, making it suitable for real-time embedded applications. Adaptive Dynamic Voltage and Frequency Scaling (DVFS) achieves 18.5% voltage reduction and 21.4% frequency optimization, contributing to lower energy dissipation. The overall system reliability reached 99.31%, whereas the computational throughput improved by 19.26%. Additionally, the thermal hotspot formation decreased by 36.58%, and the overall energy efficiency increased to 94.87%, confirming the effectiveness of the proposed PI-GNN framework for intelligent electronic design automation and next-generation heterogeneous semiconductor systems.

CONCLUSION AND FUTURE RESEARCH DIRECTIONS

This study presents a novel Physics-Informed Graph Neural Network (PI-GNN) framework for real-time, thermal-aware fault prediction and adaptive power optimization in heterogeneous system-on-chip (SoC) architectures. The proposed framework effectively integrates graph-based deep learning with semiconductor thermal physics to accurately model spatial and temporal thermal behaviors while enabling proactive fault prediction and intelligent power management. By combining real-time sensor measurements, graph topology, and physics-informed constraints, the framework overcomes the limitations of conventional machine learning methods that rely solely on statistical learning. The adaptive optimization engine further enhances system efficiency through Dynamic Voltage and Frequency Scaling (DVFS), workload migration, clock gating, and power gating, ensuring balanced computational performance and thermal stability under dynamic operating conditions. The experimental evaluation demonstrated that the proposed methodology achieved a thermal prediction accuracy of 98.72% and a fault prediction accuracy of 98.15%, while maintaining the peak junction temperature at only 72.8°C, which is significantly below the safe thermal limit of 95°C. The framework reduces the average power consumption to 24.6 W, achieving 31.84% energy savings and 94.87% overall energy efficiency. Moreover, the thermal prediction error is limited to 1.82°C RMSE, with a rapid fault detection time of 3.18 ms and an inference time of 1.94 ms, making the model suitable for real-time embedded applications. The proposed optimization strategy also provides 18.5% dynamic

voltage reduction, 21.4% frequency optimization, 36.58% thermal hotspot reduction, 19.26% throughput improvement, and 99.31% system reliability, confirming its superiority in intelligent thermal management and energy-efficient computing. Future research can extend this framework by integrating reinforcement learning for autonomous power scheduling, transformer-based graph neural networks for improved long-range dependency modeling, digital twin technology for real-time hardware emulation, and hardware implementation on FPGA and ASIC platforms for practical deployment. Additionally, incorporating cybersecurity-aware thermal monitoring and quantum-inspired optimization algorithms could further enhance the reliability, scalability, and resilience of future heterogeneous semiconductor systems operating in edge artificial intelligence and next-generation electronic-design automation environments.

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