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An Efficient Counter Using Modified Upper and Lower SVL Techniques and TSPCL

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Abstract

Low-power VLSI has emerged as the fundamental building block of the modern electronic era. This leads to a substantial paradigm shift where both power dissipation, performance, and areas of utmost importance. In the earlier time of fabrication, power dissipation was mainly neglected due to the low device density and low operating frequency needed for computation. But in the modern technological era, the need for high device density, higher operating frequency, the proliferation of portable consumer electronics, concerns on environments, device reliability, and cooling cost lead to power dissipation issues being of prime concern. This study aims to tackle power dissipation by modifying the structures of D-type Flip-Flops (D-FF) and XOR gates. The objective is to minimize the number of gate counts, which in turn reduces overall power consumption. We compare our proposed method against existing methodologies, using the latter as a reference. Our approach shows a notable reduction in transistor count, leading to lower power consumption and decreased delay. The findings underscore the effectiveness of our method in improving the efficiency of low-power VLSI designs, contributing significantly to the advancement of modern electronic systems. The proposal exhibits an enhanced reduction in transistor count and hence in overall power and delay.

Keywords: VLSI, SVL, true single-phase clock (TSPCL), leakage power, CMOS transistor

INTRODUCTION

VLSI has always been a thrusting area for the miniaturization or scaling of device dimensions. However, achieving this invites an additional bottleneck between power consumption and delay. Techniques to reduce dynamic power have been addressed [1–4]. Various ideas for making memory cells more efficient with respect to power consumption have been discussed [5–9]. In this study, by altering the existing structure of the D-FF and X-OR gates to reduce the number of gate counts, power consumption can be reduced. We considered the existing proposed methodology as a reference and compared it with the proposed method. The proposed method exhibits an enhanced reduction in transistor count and, hence, in the overall power and delay.

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Existing Methodology

The generalized setup of the proposed system is illustrated in Figure 1. The system comprises a TSPCL (true single-phase clock) [10, 11]. for the entire procedure. In addition, the author incorporated two additional mechanisms: upper self-controllable voltage level (upper SVL) and lower self-controllable voltage level (lower SVL). The SVL [12] circuits initiate timed triggering of the circuit elements to achieve efficient power savings.

Upper SVL

In Figure 2, there are three transistors: two NMOS transistors and one PMOS transistor. The top SVL had two NMOS coupled in series with a

PMOS. The PMOS obtains the supply's two NMOS gates, as well as the input clock bar. When clk is 1, the PMOS is activated, which allows it to conduct. Thus, the supply voltage (Logic1) passes. At zero, the two NMOS begs were connected to the ground. When the circuit is off, the NMOS is connected in series to reduce leakage power. The simulated output for the upper SVL is shown in Figure 3.

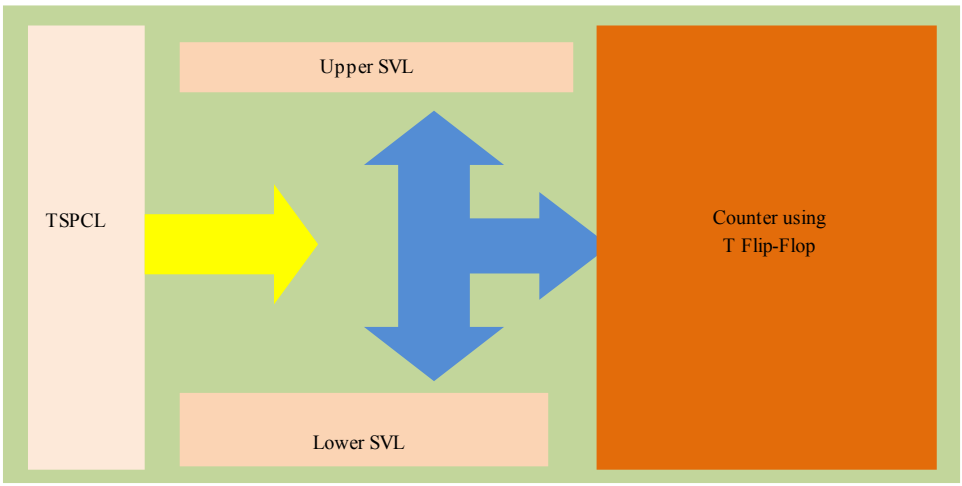

Figure 1. Generalized setup of the existing design.

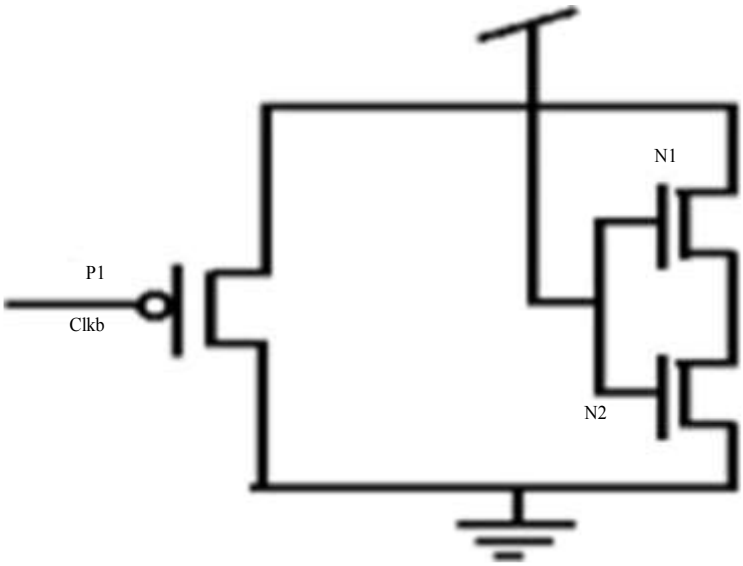

Figure 2. Upper SVL.

Lower SVL

In the diagram shown in Figure 4, there are three transistors: two PMOS transistors and one NMOS transistor. The bottom SVL has two PMOS and an NMOS in sequence [13]. The input clock is tied to the gate terminal of the PMOS and the gate of the NMOS is grounded. When clk = 1 and NMOS = 0. The PMOS begins conducting and is related to the ground. To enable a supply voltage of 1, clk was set to 0. As a result of the bias reversal, the standby mode leakage current is reduced. Figure 3 shows the lower SVL. Example of a commonly used CMOS DFF circuit [12]. The leakage power is of prime importance in CMOS technology [5]. During the off state of the circuit, the supply voltage should be brought to the minimum possible value to reduce the power dissipation and extend the battery life. An SVL approach is adopted to modify the CMOS D FF circuit to minimize the consumption of power contributed by leakage currents [7]. The use of dynamic power is also reduced because the improved design uses a smaller number of transistors. The simulated output for the lower SVL is shown in Figure 5.

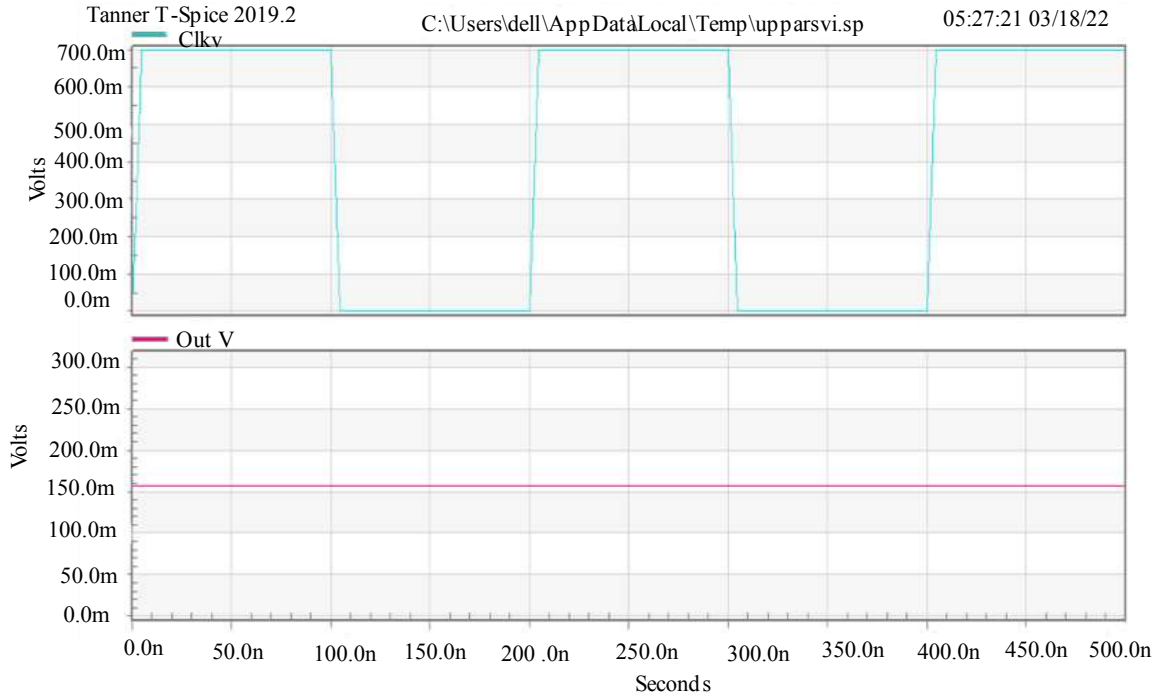

Figure 3. Simulation results of upper SVL.

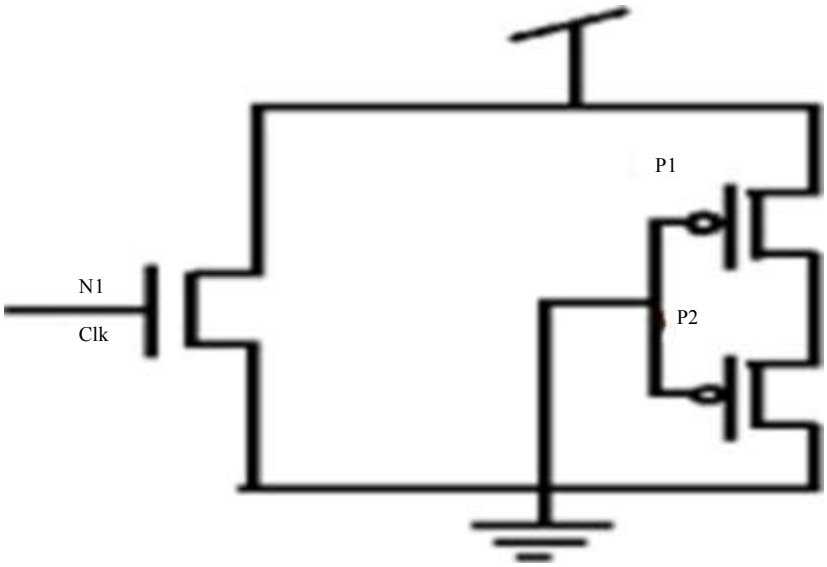

Figure 4. Lower SVL.

Proposed Methodology

Proposed Design of XOR Gate Using Pass Transistor

In the proposed idea, we first modified the existing X-OR gate and simulated its output for faithful logic generation with proper timing constraints.

Figure 6 shows the X-OR gate using PTL logic. In a conventional gate, the logic input is applied to the gate terminal of the CMOS transistor, whereas in our pass transistor logic, the input is applied at the source/drain terminal. The setup above comprises two transistors, N1 and N2. The ABAR signal propagates through the N1 transistor with gate input B. Signal A propagates through another pass transistor N2 with BBAR as a gate signal. Thus, the outputs of these two pass transistors, which are tied to the output, form the desired o/p logic.

The concept used in the above design was based on the pass transistor methodology. By using the pass transistor methodology, the transistor count requirement will be reduced to two from 12 transistors. The simulated waveforms for the proper functionality of the proposed X-OR gate show that it suffers from an attenuated VoH. Thus, there is scope to nullify this op-swing variation to an optimal level. Figure 7 represents the simulated output for the proposed X-OR gate.

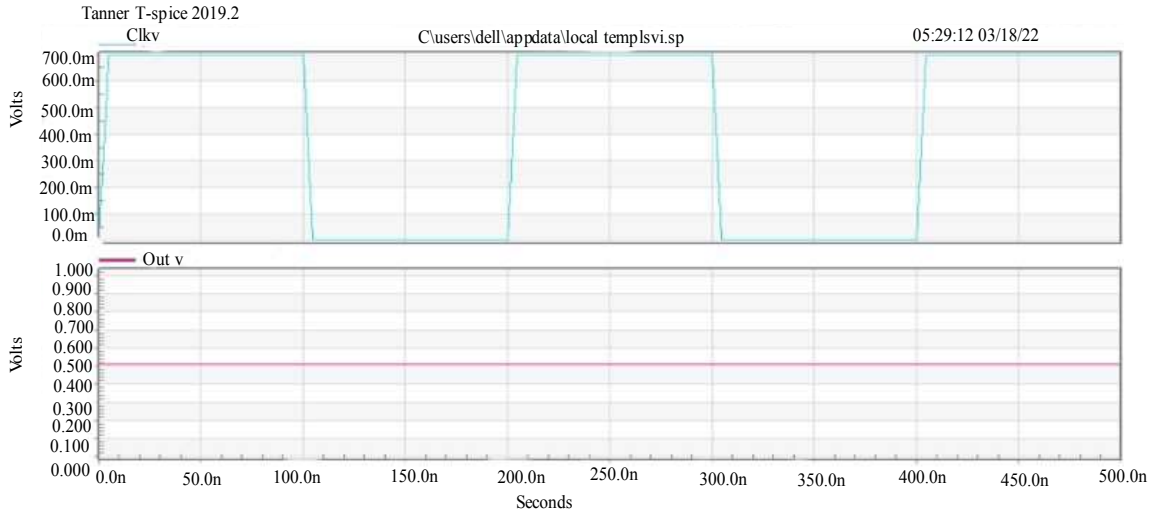

Figure 5. Simulation result of lower SVL.

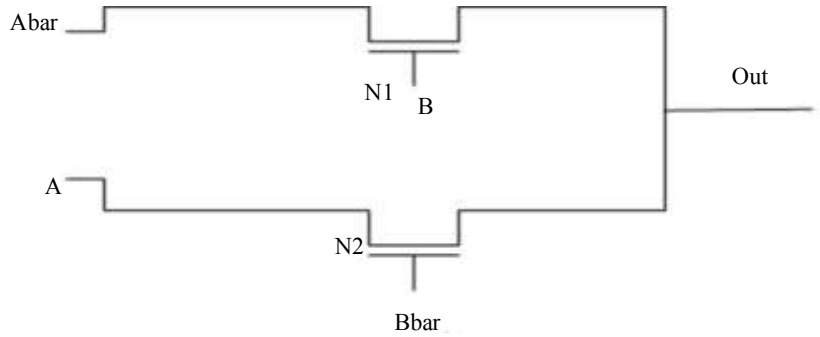

Figure 6. Proposed schematic design of the proposed X-OR gate.

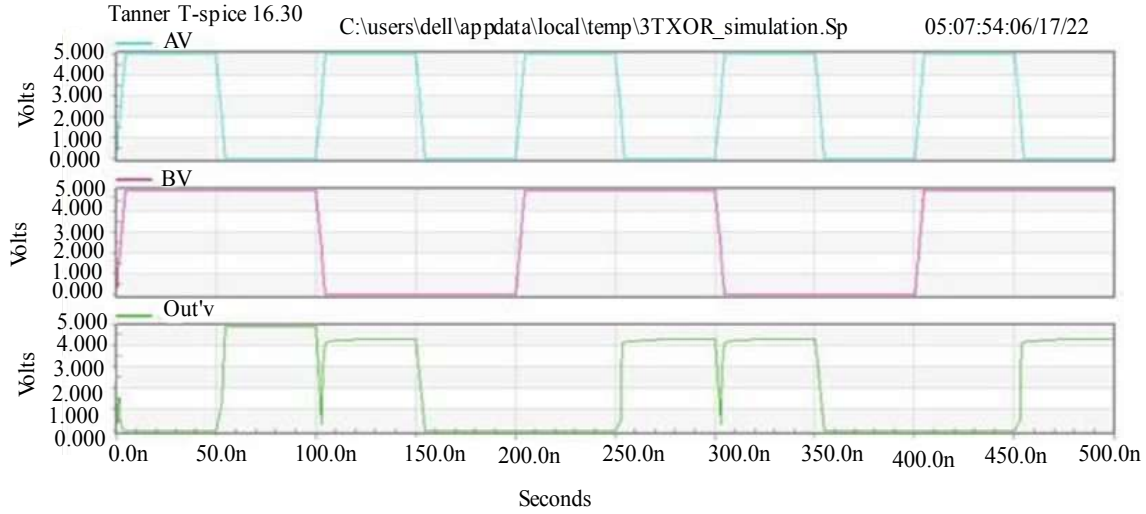

Figure 7. Simulation results of existing XOR gate using pass transistor.

Proposed D Flip-Flop Using Static CMOS

A schematic of the proposed DFF is shown in Figure 8. The circuit comprises five transistors in total, where two PMOS and three NOS transistors are used, which are positive edge triggered. The idea we used in the above design is based on a Static CMOS transistor methodology in the dynamic mode. By using a Static CMOS transistor in the dynamic methodology, the requirement of transistors is reduced to a great extent, which requires 05 transistors only compared to its normal counterpart, which requires 20 transistors. Thus, the proposed technique achieves almost 40% area efficiency compared with the existing design. When Clock and input =1, transistorsP1, and N3 turn OFF, but the rest of the transistors N1, N2, and P2 turn ON, which makes o/p=1. Thus, when the clock time is 1, o/p reflects the value of i/p. The o/p waveform in Figure 9 of the modified DF–F shows the exact behavior of the said FF and thus validates the proper functionality of the proposed design.

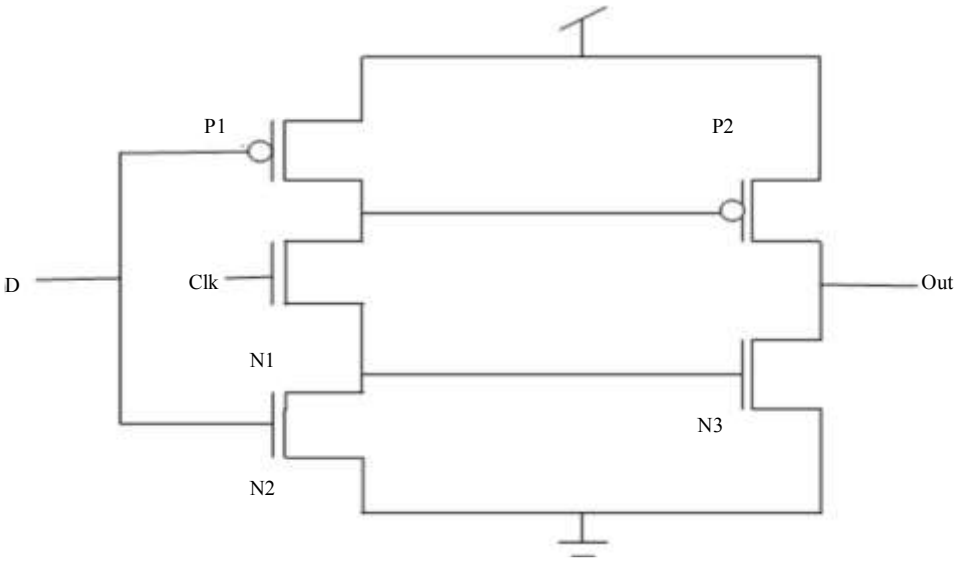

Figure 8. Proposed schematic design of D flip-flop using 5 transistors.

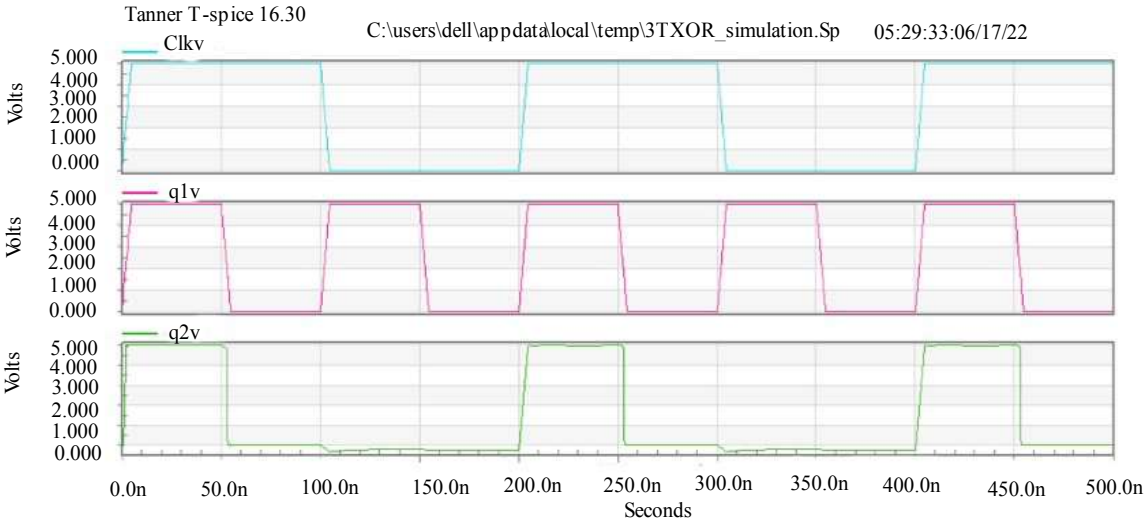

Figure 9. Simulation result of D Flip-flop using 5 transistors.

The Proposed 4-Bit Synchronous Counter

Several ideas have been formulated to implement a power-efficient counter [14, 15, 16]. The proposed counter was designed with three XOR gates, six D flip-flops, and three inverters. An additional buffer in each of the three sections helps build the master and slave operations. This 3-bit

synchronous counter increments sequentially on every clock pulse, causing the outputs to count upward from 0 (000) to 7 (111). This type of counter is known as a 3-bit Synchronous Up Counter. Initially, all the flip-flops were set to 0. Thus, the initial state of the three flip-flop outputs was QCQBQA = 000. On the falling edge of the first CLK signal, the output of flip-flop A toggles from 0 to 1. However, flip-flops B and C remain unchanged, as their inputs are zero until the next CLK signal arrives. Therefore, after the first CLK signal, the output of the flip-flops is QCQBQA = 001.

Before the second clock signal, both flip-flops A and B inputs become 1 because of the high output of gate A1. Consequently, on the falling edge of the second CLK signal, both flip-flops toggled again, changing the output from 001 to 010. This turns off the logic gates A1 and A2.

Upon application of the third clock signal, flip-flop A toggles again on its falling edge, turning logic gates A1 and A2 on, resulting in an output of 011. With the fourth clock signal, all three flip-flop inputs are high. On the falling edge of the fourth flip-flop, all flip-flops output toggles, changing QA and QB to 0 and QC to 1, resulting in an output of 100. This turns off the logic gates A1 and A2.

At the fifth clock signal, on the falling edge, flip-flop A toggles again, setting QCQBQA to 101 and activating logic gates A1 and A2. This sequence continues, with each subsequent clock signal causing further toggling of the flip-flop.

Upon reaching the eighth clock signal on the falling edge, all flip-flop outputs QCQBQA are reset to 000. The simulation results are shown in Figure 10.

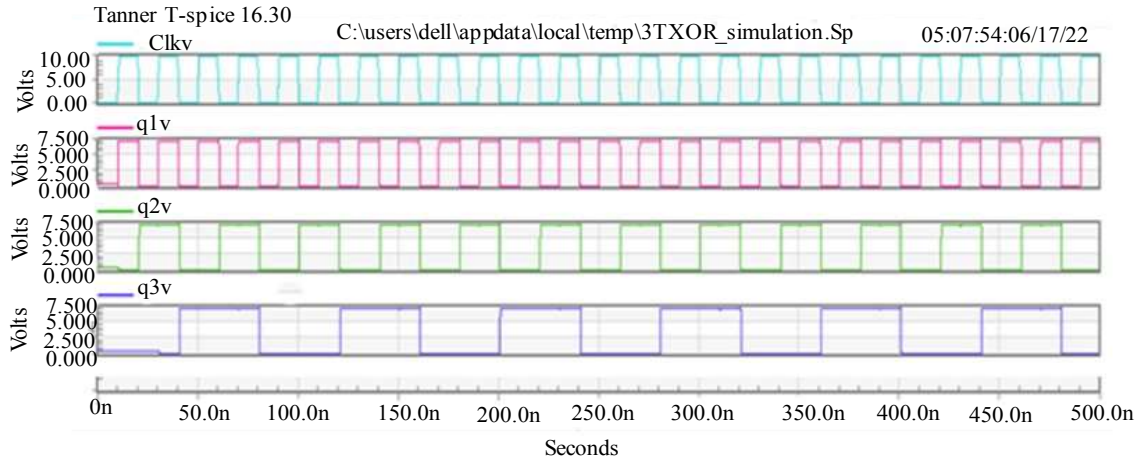

Figure 10. Simulation results of the proposed 4-bit synchronous counter.

Comparison of Results Between Existing &Proposed Design

The table above shows the differences between the existing and proposed design methods. By validating the TANNER 250 nm technology tool, we can say that the proposed method consumes less power than the existing methodology.

Table 1. Comparison of results.

S.N.	Parameters	Existing technology (250 nm)	Proposed technology (250 nm)
1	Area	184 Transistors	76-Transistors
2	Power	4.68 Watts	0.01102 watts
3	Delay	10.2946n	90Ps
4	Power delay product (PDP)	47.35	0.99

CONCLUSION

The findings from this study clearly show that simple modifications to conventional XOR gates and D-type Flip-Flops (D-FFs) can lead to significant improvements in various critical parameters. Specifically, these modifications result in substantial reductions in the transistor count, power consumption, area, delay, and power delay product (PDP). By decreasing the transistor count, the efficiency of VLSI designs is enhanced, contributing to lower power usage and improved performance metrics, which makes the designs more compact and faster.

Moreover, the impact of these modifications is broad and significant. Enhanced efficiency in power and area utilization can lead to cost savings, improved reliability, and extended battery life for portable electronic devices. In addition, a reduced delay can result in faster processing speeds, which is essential for high-performance computing applications.

Further research in this area promises even greater reductions in the transistor count. More efficient VLSI designs can be achieved by continuing to explore and refine these modifications. Future studies could investigate alternative design techniques, optimization algorithms, and emerging materials that could further advance the low-power VLSI technology. Such advancements would not only push the boundaries of current technology but also pave the way for the development of more powerful, energy-efficient, and compact electronic devices in the future.

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