International Journal of
Electrical and Communication
Engineering Technology

Volume 3, Issue 2, 2025
July–December
DOI (Journal): 10.37591/IJECET

https://journals.stmjournals.com/ijecet

Research IJECET

A High Frequency and Power Efficient Memristor Emulator and Its Application

Sudhir Singh[1],*, Manoj Josh[2], Rahul Kumar Gupta[3], Stuti Sachan[4], Suman Chaudhary[5]

Abstract

This study presents a small, energy-efficient memristor emulator made for use at high frequencies. The proposed circuit has a simple design that only includes three n-type MOSFETs and a grounded capacitor. This means that there is no need for active components or DC biasing. This streamlined architecture not only makes things easier, but it also uses very little power, with dynamic and static power measured at 15.82 µW and 65.6 µW, respectively. The design copies the most important memristive behaviour, especially the pinched hysteresis loop in the current-voltage relationship, even at frequencies up to 100 MHz. The emulator was made with 90 nm CMOS technology and works well across a wide range of frequencies. The emulator not only has a small size and low power use, but it also works well in a wide range of operating conditions. Its ability to keep the pinched hysteresis loop that memristive systems have, even at high frequencies, shows how reliable and faithful it is. This design is especially good for use in high-speed neuromorphic computing systems, signal processing circuits, and non-volatile memory applications. Using only three nMOS transistors and a grounded capacitor makes it easier to make and more scalable. Overall, the suggested emulator is a useful and effective way to solve problems with high-frequency analog computing platforms.

Keywords: Memristor emulator, energy-efficient circuit, high-frequency operation, MOSFET-only design, pinched hysteresis behavior, grounded capacitor, neuromorphic computing, in-memory processing, SRAM integration

***Author for Correspondence**
Sudhir Singh
E-mail: sudhirsingh.ss0000@gmail.com

[1]Student, Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Noida, Uttar Pradesh, India
[2]Assistant Professor, Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Noida, Uttar Pradesh, India
[3]Assistant Professor, Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Noida, Uttar Pradesh, India
[4]Student, Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Noida, Uttar Pradesh, India
[5]Student, Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Noida, Uttar Pradesh, India

Received Date: July 05, 2025
Accepted Date: September 08, 2025
Published Date: October 14 , 2025

Citation: Sudhir Singh, Manoj Josh, Rahul Kumar Gupta, Stuti Sachan, Suman Chaudhary. A High Frequency and Power Efficient Memristor Emulator and Its Application. International Journal of Electrical and Communication Engineering Technology.2025; 3(2): 45-52p. DOI: https://doi.org/10.37591/IJECET.v03i02.211948

INTRODUCTION

The memristor can be described as the "missing circuit element," which establishes a link between charge and magnetic flux, complementing the fundamental relationships defined by resistors, capacitors, and inductors in electrical circuits. It is a two-terminal component whose resistance varies based on the previous flow of current and has attracted attention because of its promise in cutting-edge applications. Over time, a range of memristor emulator circuits have been developed to mimic their behavior, frequently relying on active elements, such as operational transconductance amplifiers, current conveyors, and voltage difference transconductance amplifiers. However, many of these designs consume more power, and some of them have complex architectures and a large number of transistors.

To overcome these challenges, researchers have focused on MOS-only implementations to achieve lower power consumption, reduced circuit area, and simplified structures. In this context, the current study introduces a high-frequency, energy-efficient memristor emulator that employs three NMOS transistors and a grounded capacitor. By forgoing active blocks and DC biasing, the design not only improves energy efficiency, but also maintains the essential pinched hysteresis loop characteristic of memristors. Simulation results, based on 90 nm CMOS technology, confirm the effectiveness of the proposed design, making it well-suited for neuromorphic computing, in-memory processing, and high-speed memory applications.

LITERATURE REVIEW

The idea of a memristor—a unique electronic device that has the properties of memory and resistance—was first introduced by Leon Chua in the early 1970s [1]. These devices are built using a metal-insulator-metal (MIM) structure and have the ability to toggle between high- and low-resistance states in a distinctive, hysteresis-driven manner. This switching behaviour has enabled memristors to be used as the next-generation non-volatile memory, particularly in resistive RAM (RRAM) applications.

Although the theoretical idea sparked curiosity early on, real experimental breakthroughs did not occur until the late 1990s, when researchers began exploring a variety of materials such as binary metal oxides [2]. A major milestone was when Strukov and his team at Hewlett-Packard Labs succeeded in creating the first physical memristor, turning Chua's theory into reality [3].

Over the years, a wide range of emulator circuits has been proposed using analog components, current-mode designs, and active building blocks. For example, one design used four AD844 op-amps, a multiplier, and several passive components [4], while another combined three OTAs and four second-generation current conveyors (CCIIs) in decremental operating mode [5]. The grounded memristor emulator in [6] included a CCII, analog multiplier, resistor, and capacitor. Other solutions have leveraged elements such as CCTA [7], DVCCTA [8], and VDTA [9, 10], achieving operating frequencies as high as 50 MHz. Some designs aimed for simplicity, such as the single-CFTA-based emulator in [11] or the OTA-based 8 MHz emulator in [12]. Still, others such as the floating CCTA-CCII design [13], a hybrid CCII-OTA structure [14], and a high-speed 120 MHz DZ-VDTA-based circuit [15] have pushed for performance at the cost of increased complexity. The DVCCTA-based emulator in [16] also delivered high performance but required significant static power (8.74 mW). These examples highlight a common trade-off: higher complexity, power usage, and component count often increase with performance improvements.

To overcome these drawbacks, many researchers have focused only on using MOSFETs in their emulator circuits. For example, Yesil et al. [17] demonstrated a grounded emulator built from seven MOSFETs operated at 50 MHz. Another minimalist approach used only three transistors and achieved 100 kHz [18], whereas a four-transistor design in [19] managed up to 100 MHz. Passive floating and grounded versions were explored in [20], and Ghosh et al. [21] introduced a highly efficient 3-NMOS design with an extremely low power consumption of 2.6 µW. Further variations can be found in [22] and [23].

This study introduces a new grounded memristor emulator that stands out for its simplicity and efficiency. The circuit was built using only three N-channel MOSFETs and one capacitor, completely avoiding any active components or analog multipliers. It also requires no DC biasing, which means that it consumes no static power. Even the dynamic power usage is very low. The voltage across the capacitor controls the behaviour of two of the transistors (M2 and M3), allowing the circuit to replicate key memristive features, such as the pinched hysteresis loop, and providing tunability as needed.

METHODOLOGY

The proposed memristor emulator was developed through a structured design process involving key stages, as outlined below.

Circuit Design

The emulator circuit (Figure 1) is composed of three n-type MOSFETs, labelled M1, M2, and M3, and a single grounded capacitor (C). The layout avoids the use of any active components or DC biasing circuits, instead focusing on a minimalist yet functional structure. Within this design, M1 operates in the saturation region, whereas M2 and M3 are configured to function in the linear region. This specific setup facilitates the nonlinear resistance behavior typical of memristors. The grounded capacitor plays a crucial role by regulating the gate voltages M2 and M3, enabling variable resistance through voltage-controlled conduction.

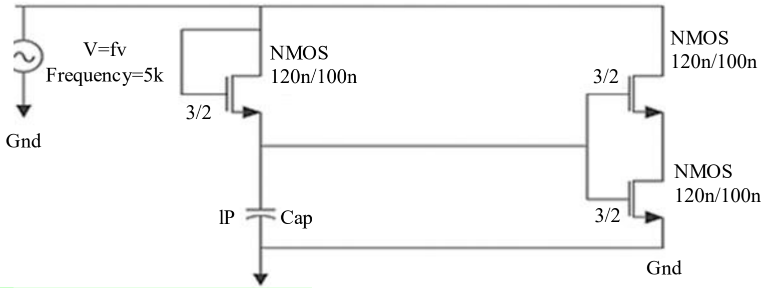

Figure 1. Circuit Diagram.

2. Mathematical Analysis

Detailed mathematical modelling was performed to establish the relationship between the capacitor voltage and nonlinear resistance across M2 and M3. The governing equations emphasize the influence of the gate voltage, controlled by the capacitor, on the overall memductance. The equations highlight the dynamic threshold characteristics of MOSFETs and their interactions under alternating input signals.

Next, considering the mathematical analysis, the drain current equation through the capacitor C can be written as

$$=> \quad C\frac{dVc(t)}{dt}=K_{n_1}(V_{in(t)}-V_c(t)-|(V_{TN})|) \tag{1}$$

$V_{in(t)}$ is the applied sinusoidal input voltage, $V_c(t)$ represent the capacitor voltage, V_{TN} is the threshold voltage of M1,$k_{n_1} = \frac{1}{2}\mu_n C_0 x\left(\frac{W}{L}\right)_{M_1}$ is the transconductance parameter of M1 in which μ_n is the mobility of electron and C_0x is gate oxide capacitance respectively. Expanding and rearranging equation 1.

$\varphi(t) \approx \int V_{in(t)}dt$ is the flux (also called state variable and its depend on the capacitor voltage $V_c(t)$
Now, considering the transistor M2 and M3 ,the conductance seen at M3 can be written as

$$=> \quad \frac{I_{in}(t)}{v_{in}(t)}=K_n(V_{GS3}-V_{TN3}) \tag{2}$$

It can be noted that identical current flows through M2 and M3 as they are in series, hence the current equation can be represented as

$$=> \quad I_{in}(t)=K_n(V_{GS3}-V_{TN3})V_{in(t)} \tag{3}$$

The gate of M3 is connected to capacitor and source is grounded so , the voltage across the capacitor and voltage across Gate to source is equal hence equation (10) can be modified as

$$=> \quad \frac{I_{in}(t)}{v_{in}(t)} \approx K_n(\frac{1}{C_1}+2\frac{K_{n_1}}{CC_1}\varphi(t)) \tag{4}$$

The Memductance equation in its final form can be eventually written as

$$=> \quad W(\varphi(t)) \approx K_n(\frac{1}{C_1}+2\frac{K_{n_1}}{CC_1}\varphi(t)) \tag{5}$$

Where, $K_n = \frac{1}{2}\mu_n C_0 x\left(\frac{W}{L}\right)$ is the transconductance parameter of M3 transistor

The first term inside the bracket contains the initial state of the memristor, which is time invariant, whereas the second term inside the bracket denotes the linear time-variant part.

It is clear that the memductance is function of its state variable φ which is the time integral of voltage.

Now, to analyze the effect of frequency on the hysteresis nature, a sinusoidal input voltage of the form $A_m \sin(2\pi ft)$ is applied where A_m is amplitude and f is signal frequency

$$\varphi(t) = \int V_{in(t)} dt$$

$$\varphi(t) = \int A_m \sin(2\pi ft)\, dt$$

$$\varphi(t) = \frac{A_m \cos(2\pi ft)}{2\pi f}$$

Substituting this in equation (12)

$$=> \quad W(\varphi(t)) = K_n[\frac{1}{C_1} + 2\frac{K_{n_1}}{CC_1}\varphi(t)]$$

$$=> \quad W(\varphi(t)) = K_n \frac{K_{n_1}}{\pi fCC_1}\cos(2\pi ft) + \frac{K_{n_1}}{C_1}$$

As f → ∞, $W(\varphi(t))$ become Linear.

IMPLEMENTATION

The memristor was made using 90 nm CMOS technology to obtain a compact, high-performance design. The circuit consists of three n-type MOSFETs (M1, M2, and M3) and a grounded capacitor (C) without using active components or DC biasing. This design architecture not only simplifies the design but also enhances the overall energy efficiency.

In the implementation, the MOSFETs were connected to produce the desired nonlinear behaviour. M1 operates in the saturation region, producing a voltage across the capacitor that subsequently controls the gate voltages of M2 and M3. Both M2 and M3 function in the linear region, acting as variable resistances that establish the nonlinear current-voltage relationship of the circuit. This specific configuration was selected to ensure the preservation of the pinched hysteresis loop characteristic of the memristors over a wide frequency spectrum.

Simulation results were obtained to evaluate the performance of the circuit. Using industry-standard simulation tools, the design demonstrated stable operation up to 100 MHz, achieving a dynamic power consumption of just 15.82 μW and an extremely low static power consumption of 65.6 μW. The analysis of the transient and frequency responses further confirmed the functionality of the circuit, verifying its suitability for low-power, high-speed applications.

To assess the real-world practicality, experimental validation was performed using commercially available MOSFETs. The experimental results closely matched the simulation results, confirming the robustness and reliability of the design. Overall, this implementation demonstrates how a compact, energy-efficient memristor emulator can be achieved without active blocks, making it an excellent candidate for use in neuromorphic systems, in-memory computing, and SRAM-based technologies.

Simulation and Experimental Validation

The circuit successfully maintained a distinct pinched hysteresis loop over a wide frequency range. The simulation results demonstrate that this behaviour is preserved even at frequencies reaching 100 MHz, confirming the high-speed capabilities of the proposed design (Figures 2-4). This marks a substantial advancement compared to earlier designs, which typically operate within only a few kilohertz to low megahertz ranges.

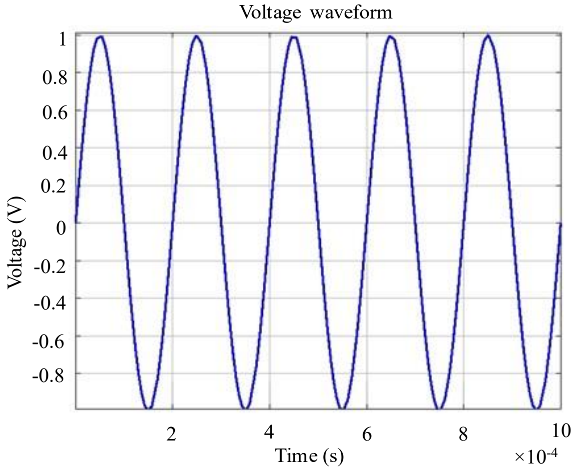

Figure 2. Voltage waveform

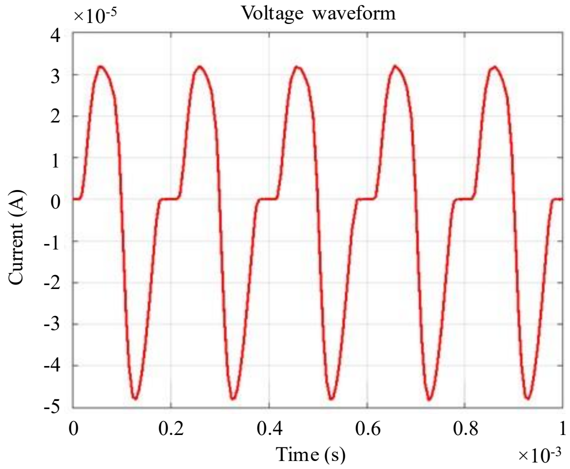

Figure 3. Current waveform

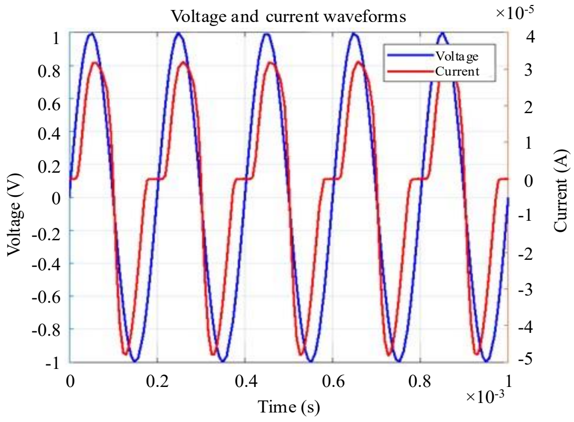

Figure 4. Voltage and current waveform.

Frequency Response

This circuit can normally operate at frequencies up to 100 MHz, making it an optimized option for high-speed applications, such as in-memory computing and neuromorphic engineering. The use of a grounded capacitor improves stability and ensures consistent performance across a wide frequency spectrum (Figures 5-8).

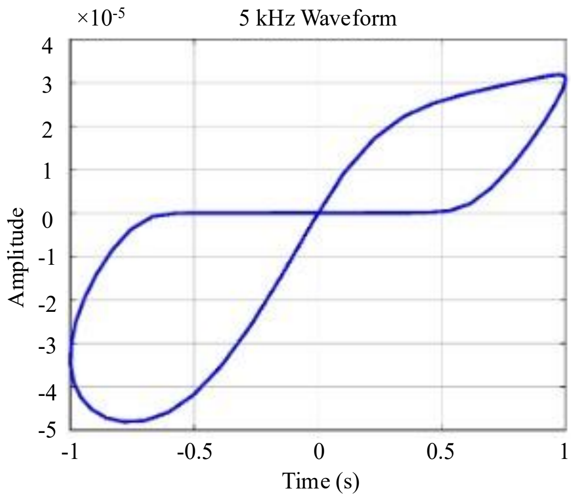

Figure 5. kHz waveform

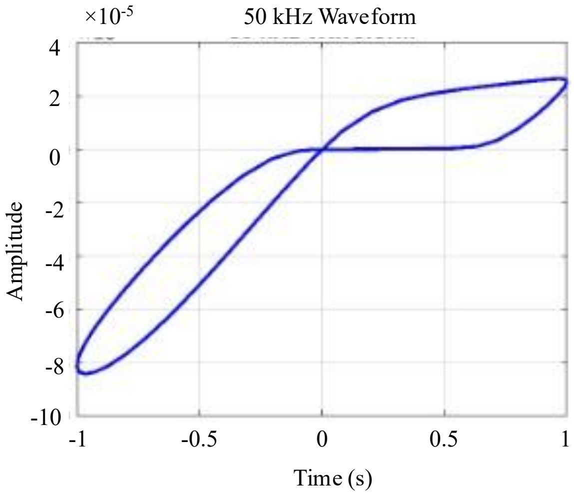

Figure 6. 50 kHz waveform

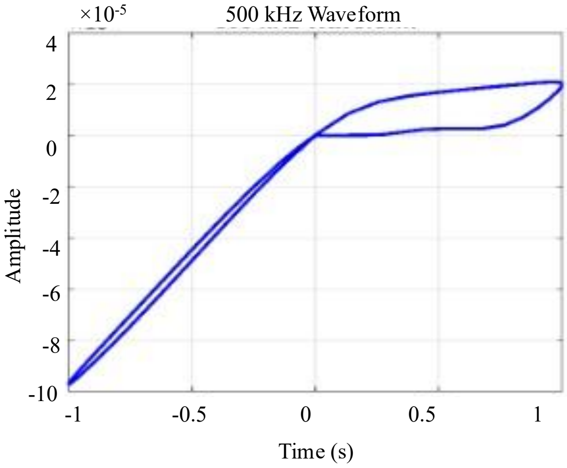

Figure 7. 500 kHz waveform

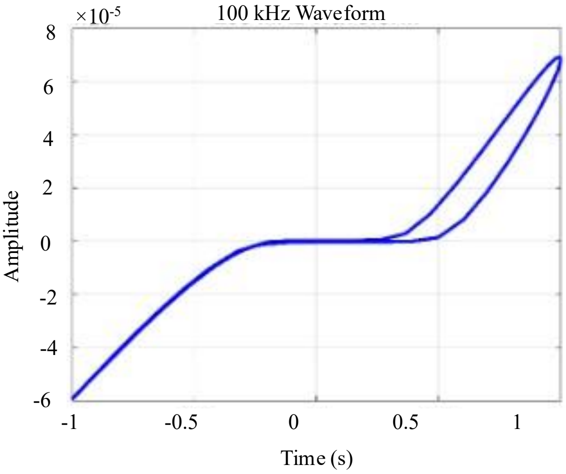

Figure 8. 100 kHz waveform

Comparison Analysis

To highlight the advantages of the proposed memristor emulator, a comparison with existing designs in terms of components, power consumption, and operating frequency is presented in Table 1.

Table 1. Comparison of the proposed memristor emulator circuit with the existing design

Ref. No.	Active Component	Passive Component	Power	Operating Frequency
[6]	1-CCII 1-Multiplier	R-1,C-1	NA	860kHz
[7]	1-CCTA	R-3,C-1	NA	1MHz
[8]	1-DVCCTA	R-3,C-1	NA	1MHz
[9]	1-VDTA	C-1	8uW/NA	50MHz
[10]	1-VDTA	R-1,C-1	NA	50MHz
[11]	1-CFTA	C-1	9.567mW	9MHz
[19]	2-PMOS 1-NMOS	NIL	8.74mW	100MHz
This work	3-NMOS	C-1	15.82uW/65.6 µW	10MHz

CONCLUSION

The proposed memristor emulator demonstrates a compact, power-efficient, and high-frequency design sui for modern electronic applications. By utilizing only three NMOS transistors and a grounded capacitor, the circuit eliminates the need for active components and DC biasing, achieving both simplicity and low energy consumption. Simulation and experimental validation confirm that the emulator preserves the key memristive characteristic—the pinched hysteresis loop—over a wide frequency range, extending up to 100 MHz. With dynamic and static power consumption values of 15.82 µW and 65.6 µW, respectively, the design is highly optimized for neuromorphic computing, in-memory processing, and non-volatile memory systems. While certain limitations exist, such as sensitivity to process variations and scalability concerns, the overall efficiency, robustness, and fidelity of the emulator make it a promising candidate for integration in high-speed and energy-aware systems. This work contributes a practical and reliable solution for advancing next-generation analog and neuromorphic circuits.

LIMITATION

a. *Limited Representation of Non-Ideal Effects:* While the design has a valid memristive operation, it might not be able to realistically represent some non-ideal attributes of physical memristors, such as temperature dependence or stochastic switching behaviors.

b. *Frequency Limits for High-Frequency Performance:* The circuit can maintain the pinched hysteresis loop up to 100 MHz. It seems practical that we have usable performance data covering a <1Hz to 100 MHz frequency range, however, to improve the optimized high-frequency application may require reducing distortion and signal degradation.

c. *Scalability Issues for Integrated Systems*: While the design is small and thus adds to overall lower power consumption, it could be the cause for parasitic net effects to be introduced in larger integrated systems, effectively preventing the use of multiple circuits in more complicated neuromorphic networks.
d. *Process Variation Sensitivity*: Given the nature of operation of the circuit, there might also be some slight sensitivity to how the component fabrication is being completed that could introduce small variance-defeat in behaviour, especially within the nanoscale regime.

REFERENCES

1. Chua L. Memristor—The missing circuit element. IEEE Trans Circuit Theory. 1971;18(5):507-19. doi:10.1109/TCT.1971.1083337
2. Waser R, Aono M. Nanoionics-based resistive switching memories. Nat Mater. 2007;6(11):833-40. doi:10.1038/nmat2023. PMID:17972938
3. Strukov DB, Snider GS, Stewart DR, Williams RS. The missing memristor found. Nature. 2008;453(7191):80-3. doi:10.1038/nature06932. Erratum in: Nature. 2009;459(7250):1154. PMID:18451858
4. Sánchez-López C, Mendoza-López J, Carrasco-Aguilar MA, Muñiz-Montero C. A floating analog memristor emulator circuit. IEEE Trans Circuits Syst II Exp Briefs. 2014;61(5):309-13. doi:10.1109/TCSII.2014.2312806
5. Ranjan R, Sharma P, Singh SP, Raj N, Kumari B, Khateb F. Memristor emulator circuit using multiple-output OTA and its experimental results. J Circuits Syst Comput. 2019;28(3):1950166. doi:10.1142/S0218126619501664
6. Carrasco-Aguilar M, Sanchez-Lopez C, Morales-López F. Current-controlled grounded memristor emulator circuit based on analog multiplier. J Appl Res Technol. 2022;20(3):347-54. doi:10.22201/icat.24486736e.2022.20.3.932
7. Raj N, Ranjan R, Khateb F. Flux-controlled memristor emulator and its experimental results. IEEE Trans Very Large Scale Integr (VLSI) Syst. 2020;28(4):1050-61. doi:10.1109/TVLSI.2020.2966292
8. Ranjan RK, Raj N, Bhuwal N, Khateb F. Single DVCCTA-based high frequency incremental/decremental memristor emulator and its application. AEU Int J Electron Commun. 2017;82:106-12. doi:10.1016/j.aeue.2017.07.039
9. Yeşil A, Babacan Y, Kaçar F. Design and experimental evolution of memristor with only one VDTA and one capacitor. IEEE Trans Comput Aided Des Integr Circuits Syst. 2019;38(6):1123-32. doi:10.1109/TCAD.2018.2834399
10. Vista J, Ranjan A. Flux controlled floating memristor employing VDTA: incremental or decremental operation. IEEE Trans Comput Aided Des Integr Circuits Syst. 2021;40(2):364-72. doi:10.1109/TCAD.2020.2999919
11. Prasad SS, Kumar P, Ranjan RK. Resistorless memristor emulator using CFTA and its experimental verification. IEEE Access. 2021;9:64065-75. doi:10.1109/ACCESS.2021.3075341
12. Kanyal G, Kumar P, Paul SK, Kumar A. OTA-based high frequency tunable resistorless grounded and floating memristor emulator. AEU Int J Electron Commun. 2018;92:61-7. doi:10.1016/j.aeue.2018.05.027
13. Ranjan RK, Sagar S, Roushan S, Kumari B, Rani N, Khateb F. High-frequency floating memristor emulator and its experimental results. IET Circuits Devices Syst. 2019;13(3):292-302. doi:10.1049/iet-cds.2018.5191
14. Bhardwaj K, Srivastava M. Wide-band compact floating memristor emulator configuration with electronic/resistive adjustability. Microelectron J. 2021;117:105284. doi:10.1016/j.mejo.2021.105284
15. Yeşil A, Prasad YSS, Kumar P, Raj N, Sharma PK, Priyadarshini B, Ranjan RK, et al. A compact floating and grounded memristor model using single active element. AEU Int J Electron Commun. 2022;157:154426. doi:10.1016/j.aeue.2022.154426

16. Yeşil A. A new grounded memristor emulator based on MOSFET-C. AEU Int J Electron Commun. 2018;91:143-9. doi:10.1016/j.aeue.2018.05.004
17. Barraj I, Neifar A, Mestiri H, Masmoudi M. Zero-power, high-frequency floating memristor emulator circuit and its applications. Micromachines. 2025;16(3):269. doi:10.3390/mi16030269
18. Babacan Y, Yesil A, Gul F. The fabrication and MOSFET-only circuit implementation of semiconductor memristor. IEEE Trans Electron Devices. 2018;65(4):1625-32. doi:10.1109/TED.2018.2808530
19. Srivastava P, Gupta RK, Sharma RK, et al. MOS-only memristor emulator. Circuits Syst Signal Process. 2020;39:5848-61. doi:10.1007/s00034-020-01421-x
20. Ghosh M, Singh A, Borah SS, Vista J, Ranjan A, Kumar S. MOSFET-based memristor for high-frequency signal processing. IEEE Trans Electron Devices. 2022;69(5):2248-55. doi:10.1109/TED.2022.3160940
21. Sharma PK, Ranjan RK, Khateb F, Kumngern M. Charge-controlled mem-element emulator and its application in a chaotic system. IEEE Access. 2020;8:171397-407. doi:10.1109/ACCESS.2020.3024769
22. Carrasco A, Sánchez-López C, Muñiz-Montero C. A 16 Hz–160 kHz memristor emulator circuit. AEU Int J Electron Commun. 2015;69(9):1208-19. doi:10.1016/j.aeue.2015.05.003
23. Ghosh M, Mondal P, Borah SS, Kumar S. Resistorless memristor emulators: floating and grounded using OTA and VDBA for high-frequency applications. IEEE Trans Comput Aided Des Integr Circuits Syst. 2023;42(3):978-86. doi:10.1109/TCAD.2022.3189837