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Design and Implementation of A 16-Bit Mac Unit Using Vedic Mathematics

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Abstract

Multiply-and-Accumulate (MAC) units are essential parts of digital systems, particularly in embedded systems, digital signal processing (DSP), and image processing. The performance of these systems is significantly impacted by the efficiency of the multiplication process. The design and construction of a fast 16-bit MAC unit utilizing Vedic mathematics are presented in this study. The proposed design utilizes the Urdhva Tiryagbhyam sutra to perform multiplication in a parallel manner, reducing delay and improving computational speed. Verilog HDL is used to describe and implement the entire architecture, guaranteeing a scalable and modular design appropriate for synthesis in contemporary VLSI systems. Simulation is used to verify the design's functionality by testing different input combinations to confirm accuracy and performance under various operating situations. Throughput is increased by the multiplier's integration with a 16-bit accumulator, which enables effective processing of sequential operations without the need for additional storage components. An 8-bit Vedic multiplier is integrated with a 16-bit accumulator to perform continuous multiply–accumulate operations. The design is implemented using Verilog HDL, and it is verified by simulation. The suggested architecture delivers enhanced speed, decreased propagation latency, and optimal power usage when compared to traditional MAC architecture. The design's effectiveness and simplicity make it appropriate for applications in contemporary real-time VLSI systems.

Keywords: MAC unit, Vedic mathematics, Urdhva Tiryagbhyam, Verilog HDL, DSP, carry-save adder.

INTRODUCTION

In the era of rapidly evolving digital technology, high-speed and efficient arithmetic processing has become a fundamental requirement in modern electronic systems. Arithmetic operations are crucial for applications including digital signal processing (DSP), image processing, wireless communication, artificial intelligence, and embedded systems. Among these operations, multiplication is considered one of the most critical and time-consuming processes, as it directly influences the overall system performance, speed, and power consumption [11].

In many real-time applications, arithmetic operations are not executed once but are performed repeatedly in a continuous manner. Particularly in DSP systems, operations, such as filtering, convolution, and Fast Fourier Transform (FFT) involve many multiplication and addition operations. To efficiently handle such repetitive

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computations, a specialized hardware unit known as the Multiply-and-Accumulate (MAC) unit is widely used. The MAC unit performs multiplication of two input operands and adds the result to a previously stored value, making it a core building block in processors and signal processing units [1].

The basic MAC operation can be expressed as:

$$MAC = (A \times B) + C$$

where, A and B are input operands and C is the accumulated result. The efficiency of the MAC unit largely depends on the performance of the multiplier and adder circuits used within it. Therefore, optimizing the multiplication process is essential for improving the speed and reducing the delay of the MAC unit [3].

Conventional multiplication techniques, such as array multipliers and shift-and-add methods, perform operations sequentially [12]. Although these methods are simple to implement, they suffer from several drawbacks, including high propagation delay, increased hardware complexity, and higher power consumption. As the bit size increases, these limitations become more significant, making conventional designs less suitable for high-performance applications [7].

To overcome these challenges, alternative multiplication techniques are required that can provide faster computation with reduced hardware overhead. One such promising approach is the use of Vedic mathematics, an ancient system of Indian mathematics that offers efficient algorithms for arithmetic operations. Among the various Vedic sutras, the Urdhva Tiryagbhyam (Vertical and Crosswise) method is widely used for designing high-speed multipliers. This method enables the generation of partial products in parallel, thereby significantly reducing computation time and improving overall efficiency [8].

The inherent parallelism of the Urdhva Tiryagbhyam technique makes it highly suitable for digital hardware implementation. By breaking down large multiplications into smaller operations and processing them simultaneously, it reduces the critical path delay and enhances system performance. Additionally, Vedic multipliers are scalable and can be extended to higher bit-width designs with minimal complexity [5].

In this work, a 16-bit MAC unit using Vedic mathematics is proposed to achieve improved speed, reduced delay, and efficient hardware utilization. The design incorporates an 8-bit Vedic multiplier, a 16-bit adder, and an accumulator unit to perform continuous multiply-and-accumulate operations. The entire system is implemented using Verilog HDL and verified through simulation to ensure correctness and reliability [4]

The suggested design performs better in terms of speed and power efficiency than traditional MAC designs, making it appropriate for contemporary high-performance applications [9]. Arithmetic operations are essential to determining system performance in contemporary digital systems. Multiplication is the most difficult and time-consuming of these procedures. Multiplication and accumulation processes are often carried out in applications like DSP, image processing, and artificial intelligence [2].

Conventional multiplication techniques suffer from high delay, increased hardware complexity, and higher power consumption. To overcome these limitations, Vedic mathematics provides efficient algorithms that can be implemented in digital hardware for faster computation [10].

This work focuses on designing a 16-bit MAC unit using Vedic mathematics to achieve high speed and reduced delay [6].

LITERATURE SURVEY

Any place there is a requirement for elite processing applications there is an obvious interest for an effective rapid multiplier. Augmentation takes the main time when contrasted with other number-crunching activities. Multipliers are the most fundamental squares in each elite registering design like Digital sign handling (DSP). The Mac-intosh unit, which consists of an accumulator and multiplier, plays a major role in selecting the exhibition 1 Manoj Kumar et al. 2 of any DSP block. A DSP's capacity for continuous preparation and speedy computation is satisfied by the MAC unit's improved presentation.

Throughout the long term, various thoughts have been proposed to improve the presentation and alleviate the over-the-top incomplete item term age during the traditional augmentation approach. In this paper, we have zeroed in on proposing the MAC design utilizing a coordinated Hybrid paired Multiplier and incorporated CLA viper organization. The coordinated multiplier is a mix of the Karatsuba calculation and Urdhva Triyagbhyamsutra from Vedic math. CLA viper network comprises of CLA and restrictive whole snake which assists with decreasing expansion time by performing equal expansion

In this paper, an effective parallel multiplier and accumulator (MAC) unit based on Vedic mathematics is presented. Vedic mathematics utilizes the Urdhva Tiryagbhyam sutra for the multiplier design. The proposed MAC design improves the speed of operation while reducing the gate area and power dissipation. We also achieve an improved delay with the help of a Vedic encoder, followed by the removal of the detector stage by parallelizing the intermediate results handling the data. Such pipelining of the intermediate results, before the final adder, merges the accumulator stage with the partial product stage of the multiplier. Further, the overall computation speed of the MAC unit is raised by the effective use of higher-order compressors in the consolidated partial product compression and accumulator (PPCA) architecture. The area, timing, and power reports show that the critical path delay of the proposed configuration is substantially reduced and that it outperforms existing designs. We report overall improvements of 20%–30% and 7%–18% for the 4-bit and 8-bit Vedic MAC units, respectively, with respect to their total circuit power, critical path delay, and cell area. The design was synthesized using a standard 90 nm CMOS library and implemented on an Altera Cyclone II series FPGA.

Enlargement is a critical cutoff in the measure of changing tasks. Development-based activities, for example, duplicate and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), isolating are by and large utilized in signal managing applications. As duplication over whelms the execution period of DSP structures, there is a need to create fast multipliers. Old Vedic mathematical longings the reaction fairly. In this paper, the chance of Urdhwa-Tiryagbhyam is utilized i.e., vertically and momentarily amplification to execute a 16 × 16 Bit Vedic multiplier, and improvement is made by utilizing the pass on saving adders. Secluding and past plans, the proposed configuration accomplishes a 33.26% reducing in com binational way delay. The Vedic multiplier proposed is executed in VHDL while joined and imitated utilizing Xilinx ISE Design Suite 14.5.

In RISCs (Reduced Instruction Set Computers), DSPs (Digital Signal Processors), accelerators, and other devices, high-speed parallel multipliers are essential. Some common methods for executing combined multipliers that are suitable for VLSI implementation include array multipliers, Booth multipliers, and Wallace tree multipliers. In accordance with the Urdhva Tiryagbhyam (Vertically and Crosswise) sutra of Vedic mathematics, a novel digital multiplier (hereafter referred to as the Vedic Multiplier, or VM) scheme is presented.

An improved system for a low-power and high-speed multiplier of two binary numbers (16 bits each) is developed. An algorithm is proposed and implemented on 16 nm CMOS technology. The designed 16 × 16-bit multiplier dissipates a power of 0.17 mW. The propagation delay period of the proposed design is 27.15 ns. These results show various improvements in power dissipation and delay reported in the literature for Vedic and Booth multipliers.

In VLSI design, low-power reduction is achieved by primarily reducing the power. Currently, low-power designs are prevalent in VLSI for many reasons. The main focus is to reduce the heat in the device. From the basic mathematical equations for power, a reduction in power can be achieved by either reducing the clock frequency, reducing the voltage, or reducing the load capacitance. The option of reducing power can be achieved by reducing voltage, as clock speeds should be maintained for faster systems. Power reduction can be done at various levels, such as architecture, logic, and semiconductor. A reduction of power and area can be achieved by trading off one factor to achieve the other. In this work, a Booth multiplier is designed based on a probabilistic approach. In the truncation part of partial products, a probabilistic estimation bias circuit is introduced. The Ripple-Carry Adder (RCA) was replaced with a Carry-Lookahead Adder (CLA) in the implementation. Simulations were done using Synopsys Design Compiler for 90 nm technology. A 9.7% area decrease and a 3.9% power decrease were reported for L = 8 and L = 10 when compared with existing work.

EXISTING SYSTEM

Multiplication is a crucial function of an arithmetic block as it accounts for most of execution time in most of mathematical operations. As a result, creating a fast multiplier has long been a major subject of study. Vedic mathematics is an approach to arithmetic rules that enables faster and more effective applications. This approach divides multiplication into three steps: partial product production, partial product reduction, and carry-propagate addition.

Because the partial products and sums are produced in a single step, which minimizes the carry propagation from LSB to MSB, multiplier design based on Vedic mathematics offers several benefits. Because all of the design's smaller blocks operate simultaneously, this characteristic aids in scaling the design for bigger inputs without correspondingly increasing the propagation time.

PROPOSED SYSTEM

The Urdhva Tiryagbhyam and Nikhilam sutras of Vedic mathematics provide the foundation for the Vedic multiplier schemes suggested in the literature. Since the Nikhilam sutra is only useful for inputs near a power of ten, a design to achieve high-speed multiplication is shown in this study based on the Urdhva Tiryagbhyam sutra of Vedic mathematics, which is a generalized technique for all numbers from table 1. A set of adder designs has been proposed in the literature to improve the performance of the Vedic multiplier Figure 1. In this paper, a novel implementation of an adder based on a carry-save adder (CSA) is proposed, which reduces the carry propagation delay in the design by using carry-free arithmetic. The proposed adder configuration handles a hybrid of binary and quaternary number systems wherein the sum is directly produced in binary using the concept of a changing bit, implementing the conversion module. Vedic mathematics is an ancient technique that can be directly used in various parts of mathematics, such as algebra, calculus, etc. (Figures 2, 3, and 4). It reduces the complexity by eliminating unnecessary steps when calculating any result. There are 16 sutras in Vedic mathematics.

CONCLUSION

This paper presented the design of a 16-bit MAC unit using Vedic mathematics. Parallel processing is made possible by the Urdhva Tiryagbhyam sutra, which improves performance and decreases latency. The suggested architecture is effective, scalable, and appropriate for real-time applications, as shown by the Verilog implementation. Compared to conventional methods, the Vedic MAC unit offers better performance in terms of speed, power, and hardware utilization.

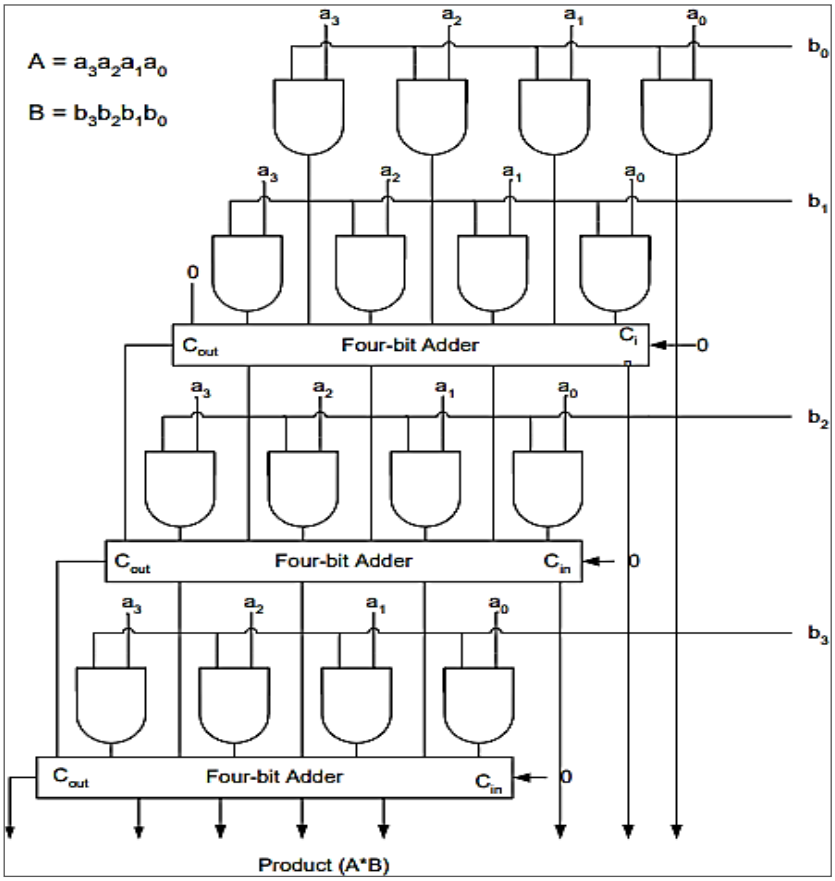

Figure 1. Block diagram.

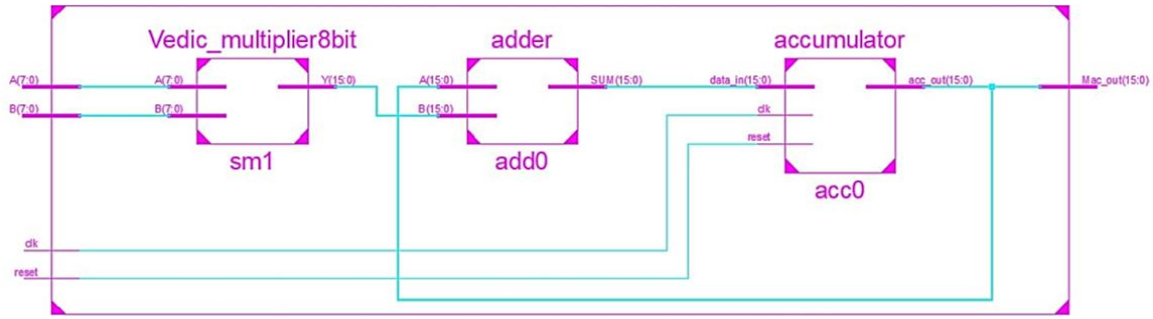

Figure 2. 16-bit MAC.

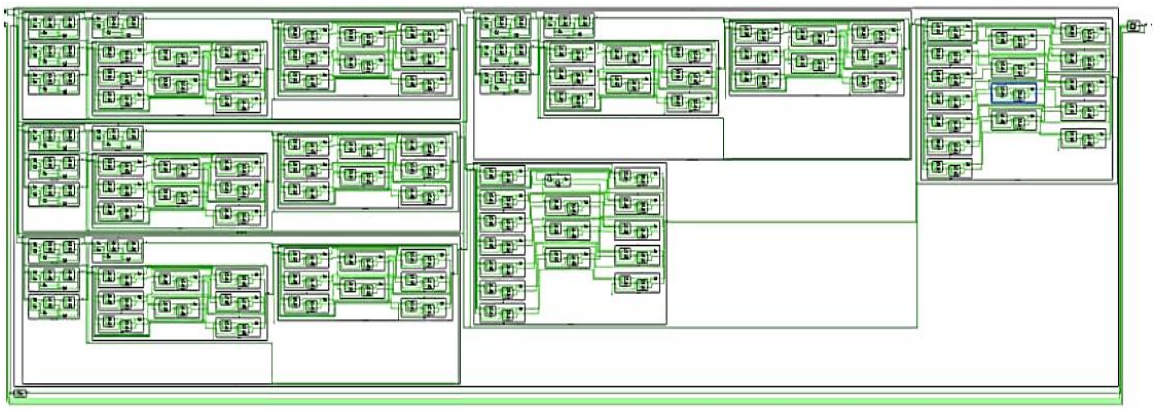

Figure 3. 16-bit MAC internal schematic.

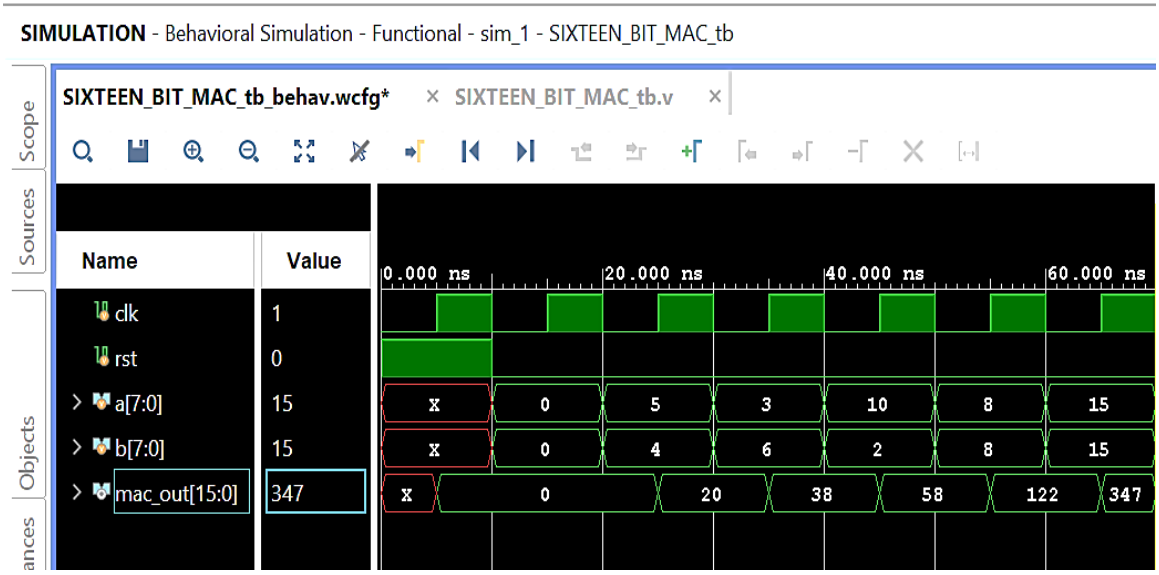

Figure 4. 16-bit MAC waveform.

Table 1. Waveforms and their results.

Features	Conventional multiplier/MAC	Vedic multiplier-based MAC
Power (W)	26.305	18.549
Delay	4.511	3.231

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