International Journal of
Digital Communication and Analog Signals

ISSN: 2455-0329
Volume 7, Issue 2, 2021
DOI (Journal): 10.37628/IJDCAS

http://ecc.journalspub.info/index.php?journal=JDCAS&page=index

Review IJDCAS

High Frequency Design Approach and Feasibility Study of HBT Based W-band (90.0 GHz-100.0 GHz) Amplifier using 130 nm SiGe Based BiCMOS Technology

Shib Shankar Singh[1, *], M. Madhav Kumar[2], Divya Kumar Garg[3]

Abstract

This paper present high frequency design approach and feasibility study of HBT (Hetero Junction Bipolar Transistor) based two-stage cascode amplifiers at W-band (90.0 GHz-100.0 GHz). The proposed amplifier has design using 130 nm SiGe based BiCMOS technology. This paper used low cost technology for designing of w-band amplifier and this is novelty of this paper. The schematic design and feasibility study has been carried out using Cadence software. The selection of active device, input and output matching and impacts of passive components have been analyzed for designing of amplifier at W-band frequency range. The schematic designed two-stage amplifier achieved +18.794±2.0 dB of small signal gain, better than – 15 dB of input return loss and better than-8.0dB of output return loss in simulation. This amplifier achieved +5.93 dBm of linear output power (+1 dB compression output power (P1 dB)) and +8.14 dBm of saturated output power in simulation at 95 GHz. This amplifier achieved less than +7% of %THD (Total Harmonic distortion). This schematic design amplifier includes the effect of all pads and bond wires of both stages of amplifier. The total current consumption of two-stage amplifier has only 30.0 mA with supply voltage of 3.3 volt.

Keywords: W-band, Cascode, BiCMOS, SiGe, HBT, Amplifier

INTRODUCTION

Microwave industry continuously progress day by day. In these days, microwave scientists and researchers have been interested in millimeter wave frequency range (30-300GHz). The main popularity of W-band (75GHz-110GHz) has low atmospheric attenuation. Due to this reason, W-band has popular in various applications such as satellite communications, various military and civilian tracking applications, radar targeting and millimeter-wave radar search used for civilian and military purposes, non-destructive testing (NDT) and security-screening techniques for inspection of various materials and detection/ visualization of internal defects/anomalies [1]. The other attractive feature of this band has very small size of system should be realized.

Various advance technologies such as compound semiconductors and SiGe based BiCMOS have used for designing of microwave amplifier at W-band, but SiGe based BiCMOS has widely used for W-band application due to low cost, small size, light weight and able to integrate many functions, because of their high integration degree and easy to realize large scale integration.

*Author for Correspondence
Shib Shankar Singh

[1]Manager, Gallium Arsenide Enabling Technology Centre (GAETEC), Hyderabad, Telangana, India
[2]Scientist-F, Advance Numerical Research and Analysis Group (ANURAG), Hyderabad, Telangana, India
[3]Scientist-E, Advance Numerical Research and Analysis Group (ANURAG), Hyderabad, Telangana, India

Received Date: March 10, 2022
Accepted Date: March 22, 2022
Published Date: March 25, 2022

Citation: Shib Shankar Singh, M. Madhav Kumar, Divya Kumar Garg. High Frequency Design Approach and Feasibility Study of HBT Based W-band (90.0GHz-100.0GHz) Amplifier using 130nm SiGe based BiCMOS Technology. International Journal of Digital Communication and Analog Signals. 2021; 7(2): 1–7p.

Due to constant efforts by the scientist/engineers in the field of SiGe based HBT components; it has possible to design complete Transceiver at W-band frequency range [2, 3].

Amplifier has basic building block of any communication system. Amplifier has generally used for enhanced the input signal level applied at input before transmission and after receiving the signal from antenna. Amplifier has used as variable gain amplifier in the highly changing mobile channel; hence help to recover the transmitted information in the receiver.

SiGe based HBT (Heterojunction Bipolar Transistor) has suitable active component for this kind of application. HBT based cascade configuration has used in each stage for higher gain. This paper present schematic based two-stage cascode amplifier designing. The cascode based two-stage amplifier achieved +18.794±2.0 dB of small signal gain, better than -15dB of input return loss and better than-8.0dB of output return loss in simulation. This amplifier achieved +5.93 dBm of linear output power and +8.14dBm of saturated output power in simulation. This amplifier achieved less than +7% of %THD (Total Harmonic distortion) at 95 GHz. The low value of %THD signifies lower peak currents, less heating and lowers electromagnetic emission [4, 5].

DESIGN TOPOLOGY

The BiCMOS based technology has used for designing purpose, because BiCMOS technology provides better technological parameters as compared to CMOS technological parameters. The parasitic effects have lesser in BiCMOS technology than CMOS technology at W-band frequency. The schematic design of W-band (90 GHz-100 GHz) amplifier has complex work, because device selection, topology selection and component selection have difficult work. The performance of the amplifier depends upon the active device, which has core component of the amplifier [6].

The device modelling and optimization have the biggest challenges at W-band amplifier design. In this frequency range, the active device model becomes highly layout dependent; therefore, universal model establishment has a very difficult task. The maximum achievable gain of transistor has determined by the extrinsic parasitic such as base, collector and emitter resistance, substrate resistance, and different parasitic capacitances of transistors. Careful studies of the foundry models, design manuals and interaction with experienced based fabrication person has very much helpful for designing of W-band amplifier. The most important parameters for amplifier have gain, linearity, output power, DC currents and bandwidth.

Cascode amplifier has a multistage configuration. A HBT (Heterojunction Bipolar Transistor) based cascode amplifier consists of a common emitter stage followed by a common base stage. A cascode amplifier has a high gain, moderately high input impedance, high output impedance, and a high bandwidth compared to traditional common emitter configuration. To increase gain and boost stability, cascode structure has been adopted in the two stages at W-band (90 GHz-100 GHz). The different sizes of transistors have been simulated using the Cadence RF Spectre simulator. The most suitable transistor size has chosen on the basis of DC I-V, small signal parameter and power output [7].

Metal-insulator-metal (MIM) capacitors have used in this design for matching and rf coupling purpose. These capacitors have made of the two metal layers with a dielectric layer (Sio2) in between. When designing an integrated circuit, resistors have important component from matching, stability and biasing point of view, therefore a large resistor area means a large parasitic capacitance exists between the resistor and the substrate. The resistor area should be small as possible. The inductors have not selected for this design, due to low self-resonance frequency and higher parasitic effects. The transmission line width selection has an important criterion at W-band amplifier designing for realize the inductors. The DC and RF pads have used in this design. The octagonal shaped pads have selected for design.

To reduce the parasitic capacitance of pad, the small size pad has selected for design. Two separate power supplies have utilized for design due to trade-off among gain, linearity and reliability point of view. This amplifier has two-stage design with both stages used cascode configuration for sufficient gain and power output. This amplifier used lossy matching technique at the input and lossless matching technique at the output of amplifier. The Input and output matching of the circuit has properly analyzed through software. The effect of bond wire length has also account in this design. The effect of bond wire has significant at W-band (90 GHz-100 GHZ). The collector of circuit has biased by transmission line and base of circuit has biased by 1 Kohm resistor. The aspect ratio of capacitor has also one of important aspect for schematic designing of amplifier at W-band. The aspect ratio adds the amount of parasitic in simulation.

The major objective of this design must include the minimum number of components for achieving good matching with stable operation. Inclusion of more number of components increases the matching loss due to parasitic effect of the component, therefore the gain and power output of the amplifier degraded. The capacitors and bond pads have also behave as lossy in nature at W-band frequency range. The size of bond pad has also critical for designing of the amplifier at W-band frequency [8, 9]. The optimum size of bond pad has chosen for the designing purpose; otherwise, bond pad effects have significant at this frequency range. The parasitic effect of capacitor has significant at this frequency. The loss of transmission line has significant at this frequency. Therefore, selection of passive components has also challenges at this frequency range [10].

RESULTS AND DISCUSSION

The reverse transmission coefficient (S12) of the cascode configuration has higher as compared to common source configuration; therefore, it provides higher stability at W-band frequency range. Therefore, several additional components have not included in design for stability purpose. The stability of amplifier has checked from 10 MHz to 120 GHz and the amplifier has unconditional stable. The value of stability factor (k) $\geq$ 28.377.

Table 1 summarizes the performance of various reported amplifier using various technologies. The proposed W-band amplifier shows comparable performances. Figure 1 shows the schematic of two-stage amplifier. Figure 2 shows simulated small signal gain of proposed amplifier Figure 3 shows simulated input return loss of proposed amplifier. Figure 4 shows simulated output return loss of proposed amplifier. Figure 5 shows simulated reverse transmission (S12) of proposed amplifier. Figure 6 shows simulated linear and saturated output power of proposed amplifier at 95.0 GHz. Figure 7 shows %THD (total harmonic distortion) versus input power at 95.0 GHz for analyzing unintentional interference with other electronic devices. Figure 8 shows in-band stability versus frequency. Figure 9 shows full-band stability versus frequency.

Table 1. Performance comparison of w-band amplifier using various technologies.

Ref.	**Freq. (GHz)**	**Tech**	**Gain**	**Input return loss (db)**	**Output return loss (db)**	**P_{sat} (dBm)**	**Supply voltage (Volt)**	**Total current (mA)**	**Topology**
This work*	90=100	130 nm BiCMOS	18.64	<-15	<-8	8.143	3.3	30	Cascode
2	82-101.5	100 nm GaAs MHEMT	8-10.8	<-10	<-10	N/A	1.5	28	Common source
3	75-100	100 nm GaAs MHEMT	10.1-13	<-5.1	<-5.1	7.6**	1.8	N/A	Common source
4	91-108	90 nm CMOS	17	<-7.0	<-15.0	12	1.5	N/A	Single ended and balanced amplifier

**Schematic simulated N/A- Not Available **P1 db*

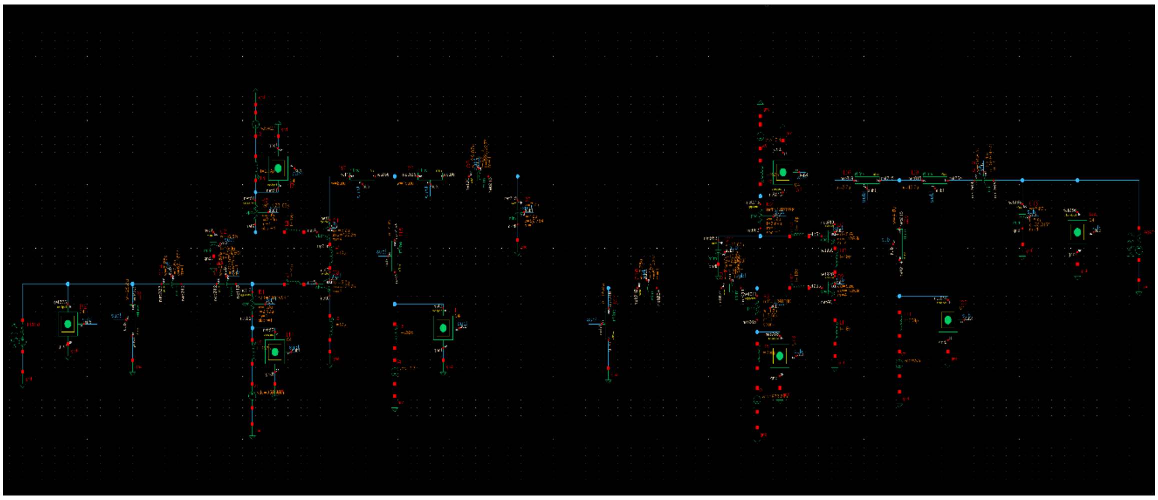

Figure 1. Schematic of two-stage amplifier.

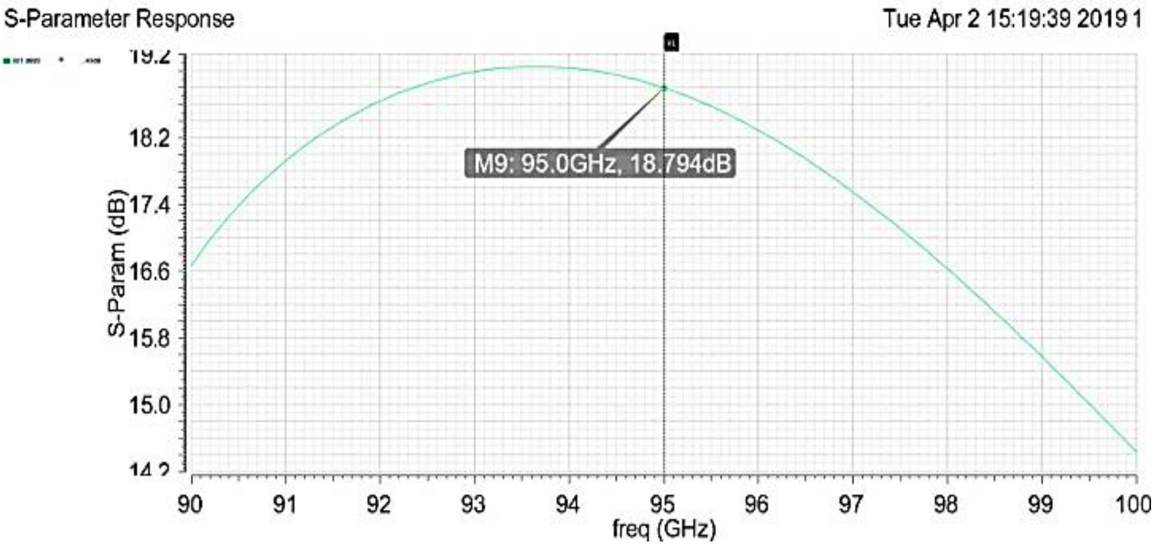

Figure 2. Simulated small signal gain versus frequency.

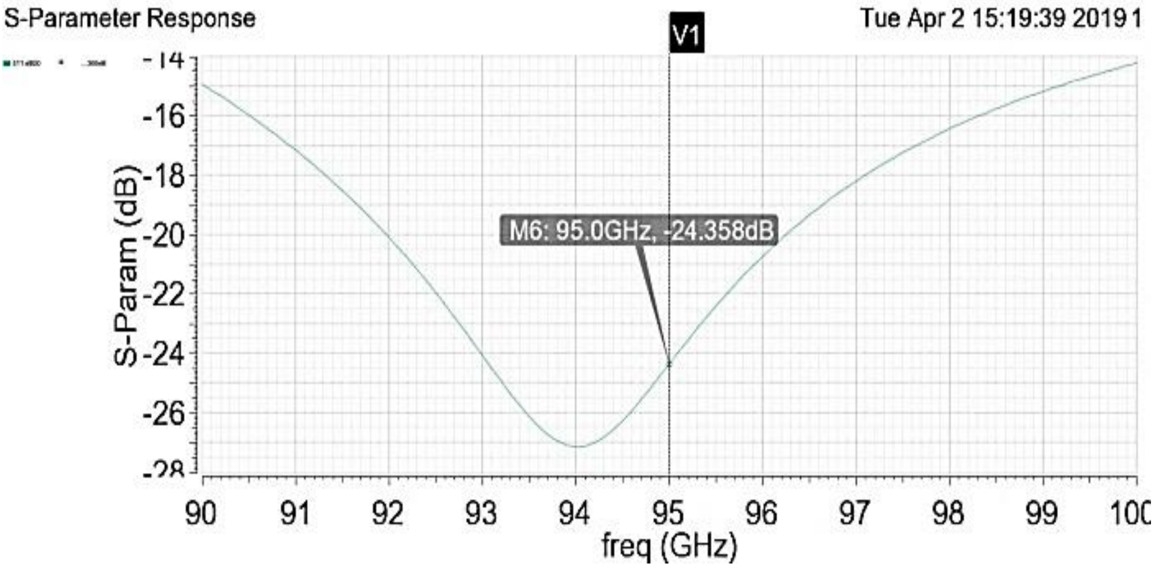

Figure 3. Simulated input return loss versus frequency.

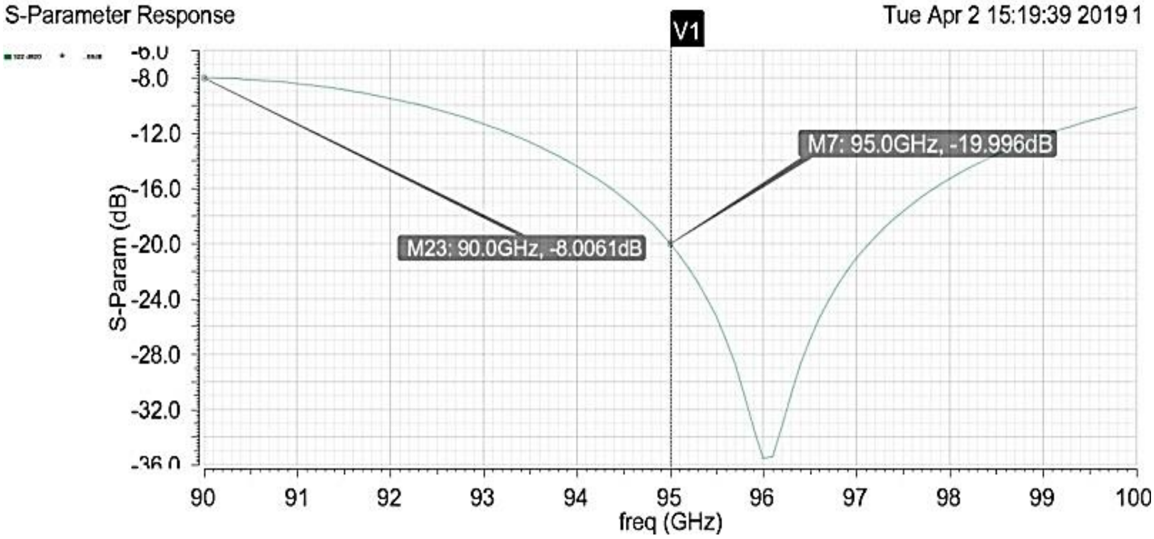

Figure 4. Simulated output return loss versus frequency.

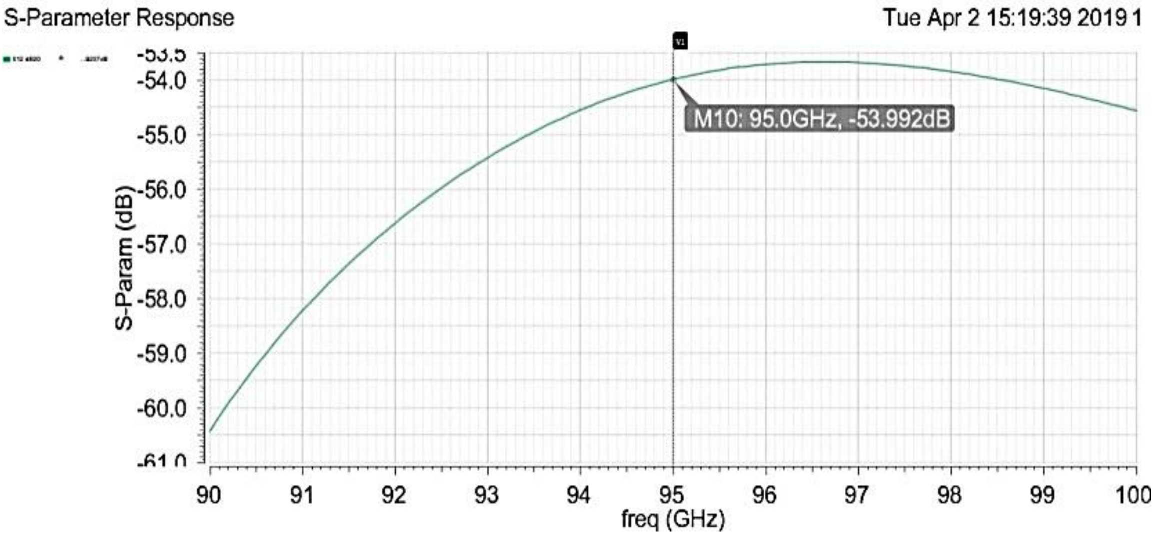

Figure 5. Simulated reverse transmission versus frequency.

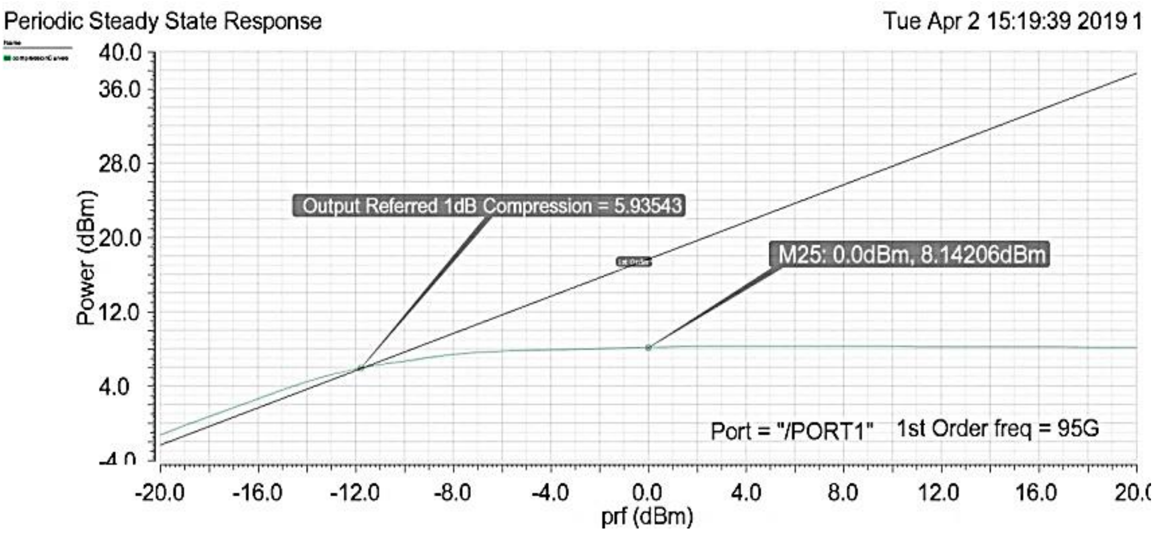

Figure 6. Simulated linear and saturated output power of proposed amplifier at 95.0GHZ.

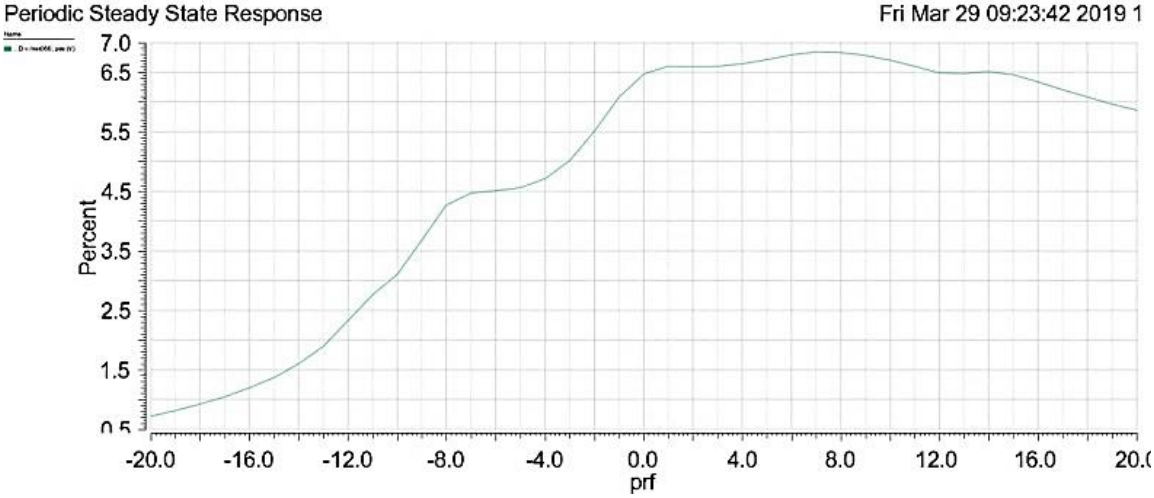

Figure 7. %THD (total harmonic distortion) versus input power at 95.0GHz.

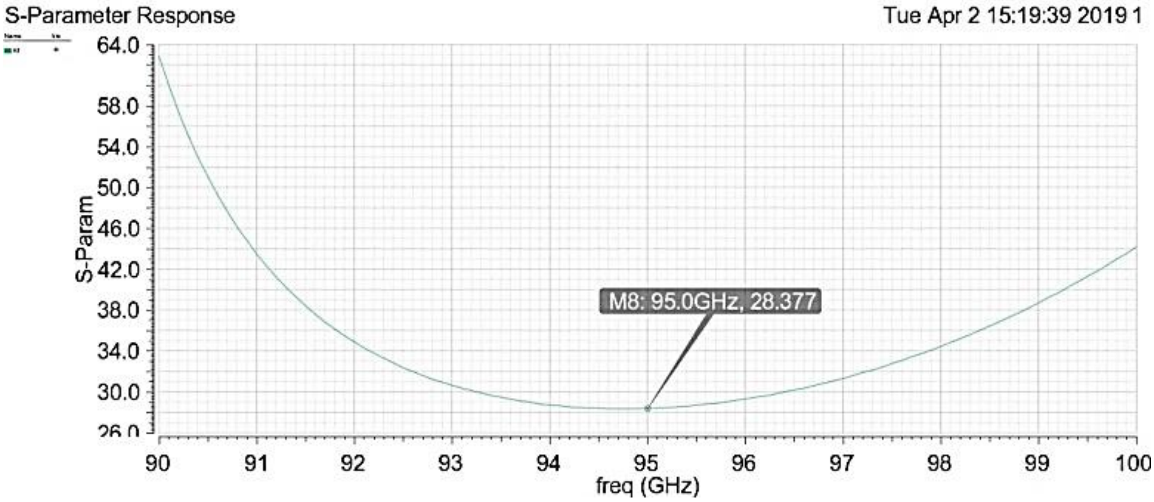

Figure 8. In band stability versus frequency.

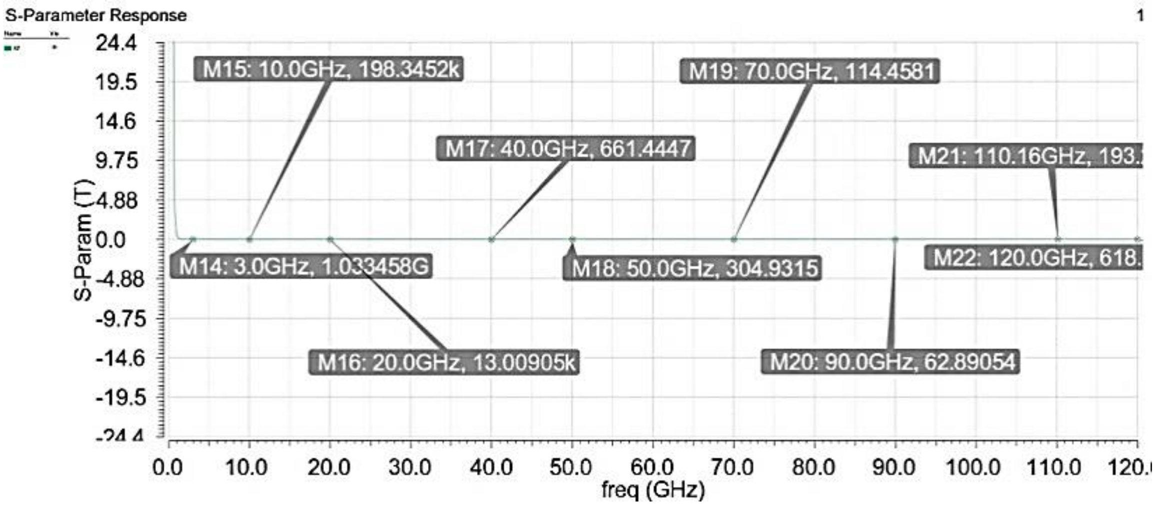

Figure 9. Full band stability versus frequency.

CONCLUSION

In this paper, cascode based high frequency amplifier designing technique have been discuss and two-stage amplifier has been design and simulated at W-band frequency. The two-stage amplifier has design using 130 nm SiGe based BiCMOS technology: which has cost effective, mature and reliable? This paper provides the valuable information that optimal size of active and passive device selection has important aspects for designing of amplifier at W-band.

Acknowledgement

The authors would like to thank CEO, GAETEC (Anant A. Naik) for his kind support, motivation and approval. The authors would like to thank their family members for their kind support and motivation.

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