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Comparative Study of Drain Current of Symmetric and Asymmetric DG-MOSFET with Simulation in Silvaco TCAD Software

Abhishek Saha[1], Vedatrayee Chakraborty[2,*]

Abstract

One of the most attractive and promising devices for the nanoscale devices is the double gate MOSFET. The double gate MOSFET can control the Si channel very efficiently and it chooses a very small width of the Si channel. It controls the Si channel by applying gate contact to either side of the channel. The idea of controlling the S channel in such a way reduces the short channel effects and one can get a higher current as compared with a single gate MOSFET. In this paper, models of both symmetric and asymmetric DG-MOSFET are studied and performance is compared with the performance of single gate strained silicon MOSFET. The model of DG-MOSFET is simulated with Silvaco TCAD device simulator and different characteristic parameters are being studied.

Keywords: Asymmetric DG-MOSFET, device modeling, Silvaco TCAD, strained silicon, symmetric DG-MOSFET

INTRODUCTION

In the year 1965, according to the prediction of Gordon Moore, the number of transistors per chip would quadruple every three years [1, 2]. In order to keep up with this, transistor dimensions have been reduced by half every three years. The sub-micron level was overcome in the 1980s.

Silicon-on-Insulator (SOI) devices came into the picture in the 1990s [2]. They give improved circuit speed and power consumption. Gate electrode has the ability to control the potential distribution and it can also control the flow of current in the channel. If the transistor dimensions are decreased, the distance between source and drain reduces the ability of the gate electrode. This increases the electrostatic effect of the source/drain electrodes on the channel. As a result, short channel effects (SCEs) predominates. To reduce the SCEs, gate-to-channel coupling with respect to source/drain-to-channel coupling is to be increased. High channel doping is required for the planar CMOS. Due to this, the band to band tunneling is increased which in turn increases the leakage current. Conventional bulk MOSFET cannot be scaled down below 20 nm [2]. With the help of double gate MOSFET (DG-MOSFET), these kinds of restrictions can be overcome. The gate-to-channel coupling is doubled with an extra gate which results in a good suppression of SCEs.

A planar double gate MOSFET makes use of a layer-by-layer (conventional planar) manufacturing process to make an efficient and attractive double gate MOSFET. The manufacturing process avoids stricter conditions of lithography requirements.

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The drain to source channel is sandwiched between independently fabricated gate/gate- oxide layers in planar double gate MOSFET.

When gate length becomes comparable to the depletion region then the short channel effects are seen but in DG-MOSFET, both gates control the channel from both sides and have better electrostatics control over the channel. As double gate MOSFET has better control on short channel effects, it is a better attractive alternative of conventional single gate bulk MOSFET [3]. So with double gate MOSFET, one is able to maintain the device performance in terms of low leakage current and higher current density. In recent times, the double gate MOSFET device structure has drawn more attention of the researchers due to the inherent capability of suppressing the short channel effects.

DG-MOSFET STRUCTURE

- In double gate MOSFET, two gates are used.
- They are named as front gate and back gate.
- In double gate MOSFET, as two gates are used, the gate to channel coupling becomes double and it results in good suppression of SCEs (Figure 1).

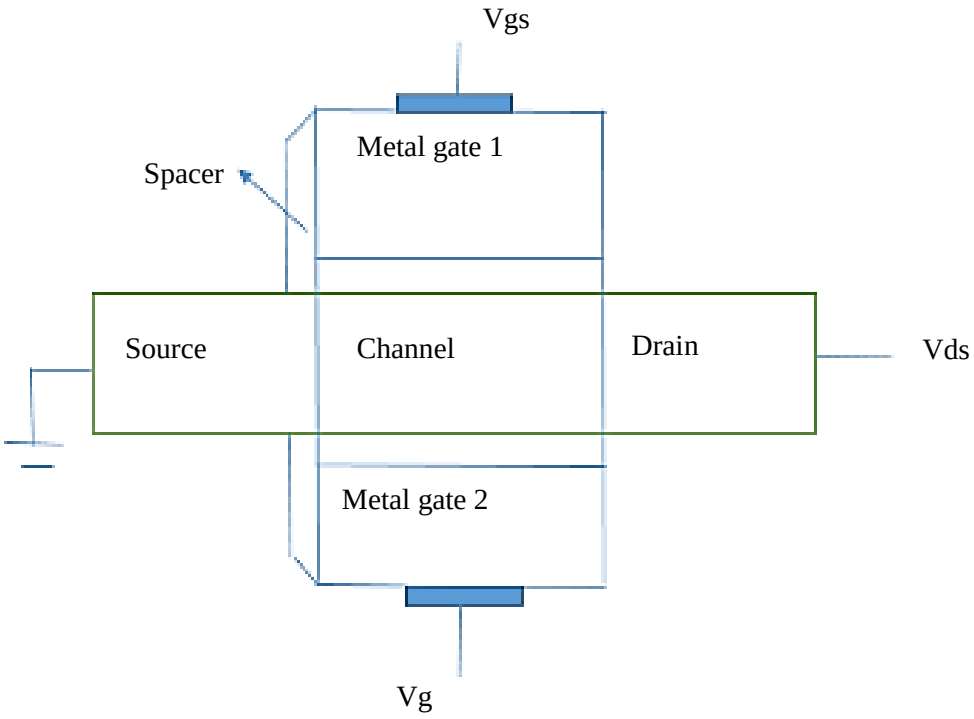

Figure 1. Structure of double gate MOSFET.

Types of DG-MOSFET

According to the way the gate voltages are applied, the double gate MOSFET may be categorized as follows:

i. Symmetric double gate MOSFET: When both gates have the same work function and a single input voltage is applied to both gates, a double gate MOSFET is said to be symmetric.
ii. Asymmetric double gate MOSFET: When a synchronized but different input voltages to both of the identical gates, or the same input voltage to two gates having different work functions is applied then a double gate MOSFET is called an asymmetric double gate MOSFET.

From the prior discussion, one can conclude the presence or absence of symmetry of the electric field inside the channel of the double gate MOSFET. Names of symmetric and asymmetric are given [4–9].

Silvaco TCAD Simulator

Silvaco TCAD products provide semiconductor process and device simulation solutions. Silvaco includes the device simulator ATLAS.

With a group of device simulation products, engineers can have the device technology to simulate the electrical, optical, and thermal behavior of semiconductor devices and this group of device simulation products is called ATLAS. It provides a modular, physics-based, extensible platform to analyze DC, AC, and time-domain responses for all semiconductor-based technologies in 2 and 3 dimensions [6–8].

THEORY TRANSPORT DESCRIPTION

DG-MOSFET model under investigation is simulated with Silvaco TCAD software. Depending on the level of accuracy required, the following simulation model is considered [10].

Drift-diffusion Model

This model is suitable for devices designed with low power density specifications and having long active regions. In this present work, the drift-diffusion model is considered for the simulation.

Drift diffusion approximation: The drift diffusion model is widely used for the simulation of carrier transport in semiconductor and is defined by the basic semiconductor equations. The Current density for electrons is given by:

$$J_n = qn\mu_n E + qD_n \nabla$$

$$J_n = -qn\mu_n \square T_n + qD_n \square \mathrm{n}$$

The current density for the hole is given by

$$J_p = qp\mu_p - qD_p \square_p$$

$$J_p = -qp\mu_p \square \mathrm{T}_p - qD_p \square_p$$

where μ_n and μ_p are the electron and hole mobilities, and T_n and T_p are the electron and hole quasi-fermi potentials respectively.

The three governing equations for carrier transport in semiconductor devices are Poisson's equation and the electron and continuity equations. The Poisson's equation is

$$-\square^2 T = \frac{q}{\varepsilon}(N_D - n + p - N_A) + P_{trap}$$

where ε is the electrical permittivity, q is the elementary electronic charge, n and p are the densities of electron and hole, N_D is the concentration of donor ion, N_A is the concentration of acceptor ion, and ρ_{trap} is the charge density contributed by traps and fixed charge.

Continuity equation for electron is given by:

$$\square J_n = qR + q\frac{\delta n}{\delta t}$$

$$-\square J_p = qR + q\frac{\delta p}{\delta t}$$

where R is the net electron-hole recombination rate.

SIMULATION RESULTS AND DISCUSSION

A model of the DG-MOSFET is considered for the Silvaco simulator. In this work, n channel metal gate symmetric DG-MOSFET is considered. SiO_2 is used as a gate oxide and spacer Si_3N_4 is also used to reduce the fringing field effect. Figure 2 shows the modeling of the symmetric double gate MOSFET. Figure 3 is showing the mesh analysis of the model of symmetric DG-MOSFET. The variation of the doping concentration of the different regions is shown in Figure 4. At the top and bottom of the film which forms the two conduction channels in double gate MOSFET, the electron density is higher. Due to the formation of two channels, it has a good drive current. The conduction band energy and valence band energy are shown in Figure 5. A well is formed in the DG-MOSFET structure. The quantum well is formed in the conduction band. Figure 6 shows the electron quantum potential of the model. The donor concentration and acceptor concentration variation are plotted in Figure 7. Variation of the electron affinity is plotted in Figure 8. To judge the device performance, the threshold voltage is an important parameter. The threshold voltage is actually a source voltage (Vgs) for which a conducting channel is formed due to the accumulation of a sufficient amount of mobile electrons. Figure 9 shows the variation of drain current with the variation of Vgs for two different drain voltages.

In this work, the asymmetric DG-MOSFET is also considered. Drain currents for different Vds are calculated for three different models like asymmetric DG-MOSFET, symmetric DG-MOSFET, and strained silicon single-channel MOSFET. The results are compared and plotted in Figure 10. The drain currents are calculated for different channel lengths and the results are compared with the simulated data. It is plotted in Figure 11. From the figure, it can be concluded that simulated results are almost tallied with the analytical data obtained by the theoretical modeling. The variation of drain current with the variation of the Vgs is obtained for different Vds for both symmetric and asymmetric MOSFET and compared. The comparison is shown in Figure 12. From the comparison, it is clear that the model of asymmetric MOSFET shows a better result (Table 1).

Table 1. Device parameters taken for the design.

S.N.	Parameter	Value (unit)
1.	Gate length	0.030 μm
2.	Gate oxide thickness	0.0015 μm
3.	Silicon film thickness	0.003 μm
4.	Substrate doping p-type	1e18/cc
5.	Source/drain doping n-type	1e20/cc

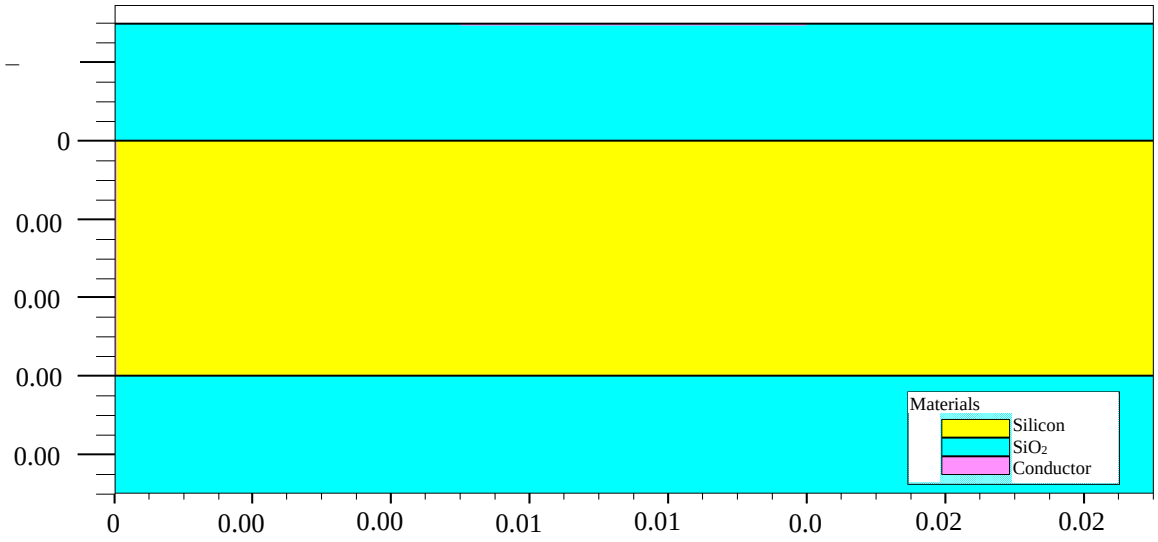

Figure 2. Symmetric double gate MOSFET.

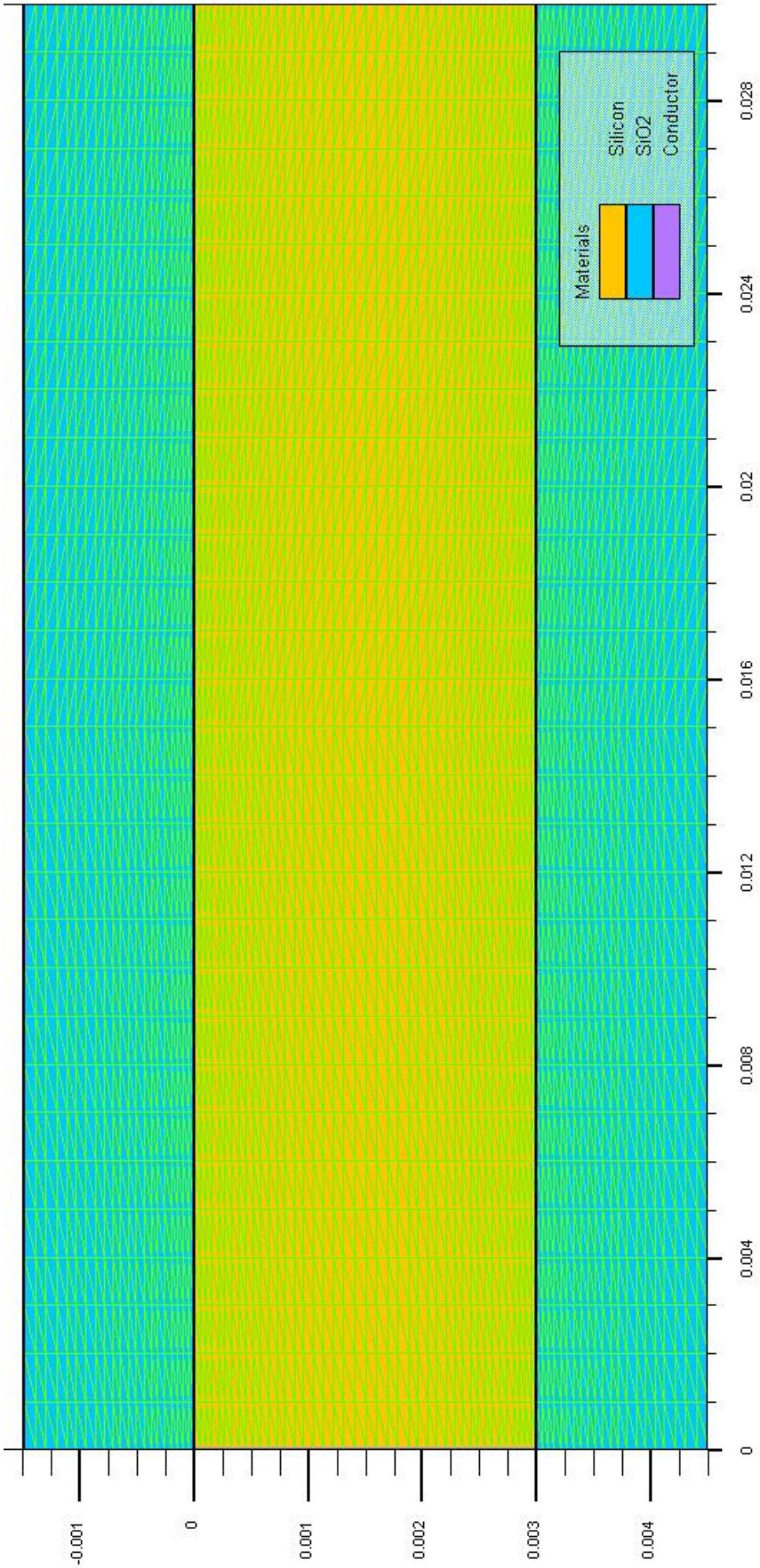

Figure 3. Mesh analysis of the model of symmetric DG-MOSFET.

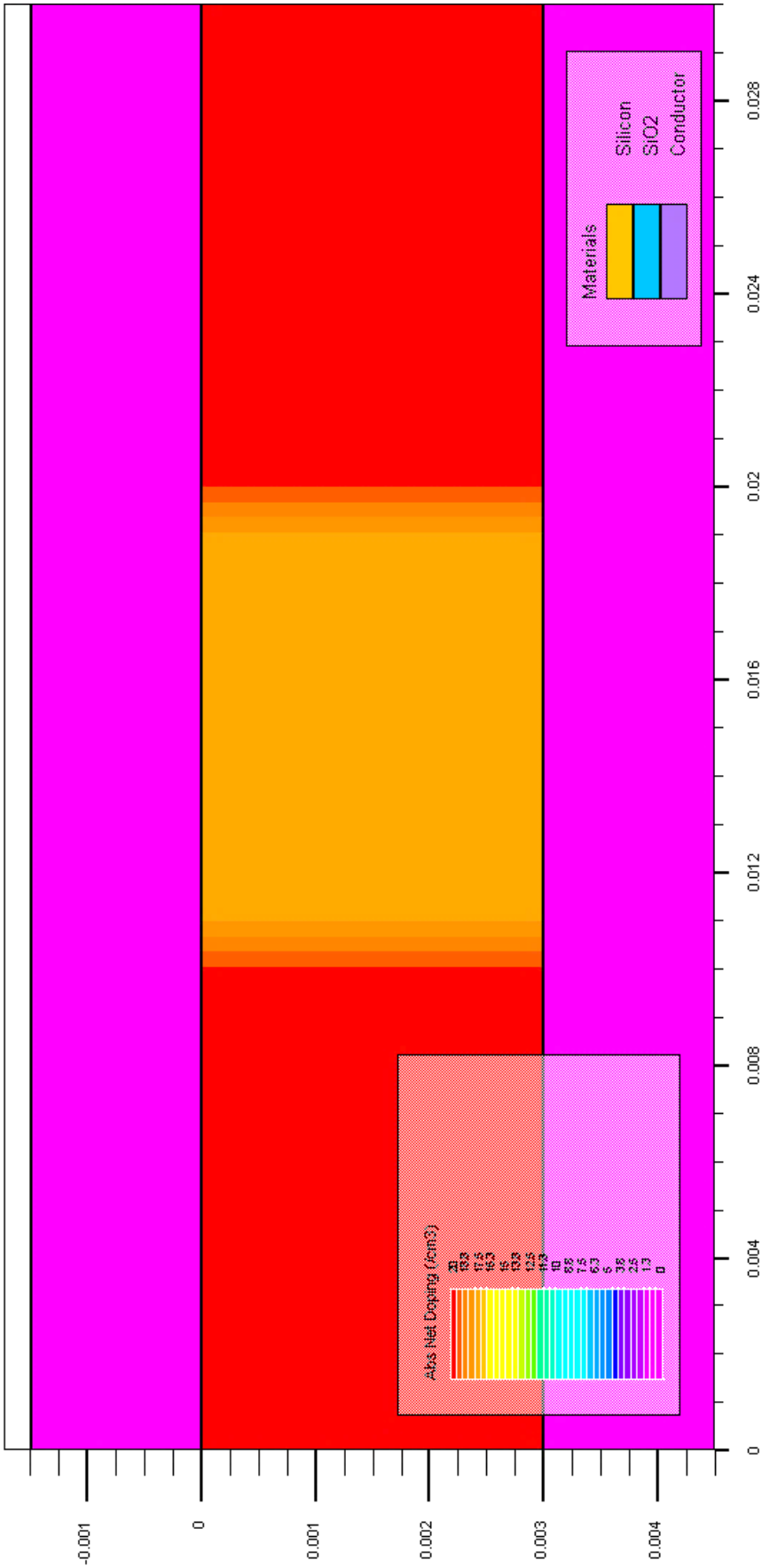

Figure 4. Variation of doping concentration.

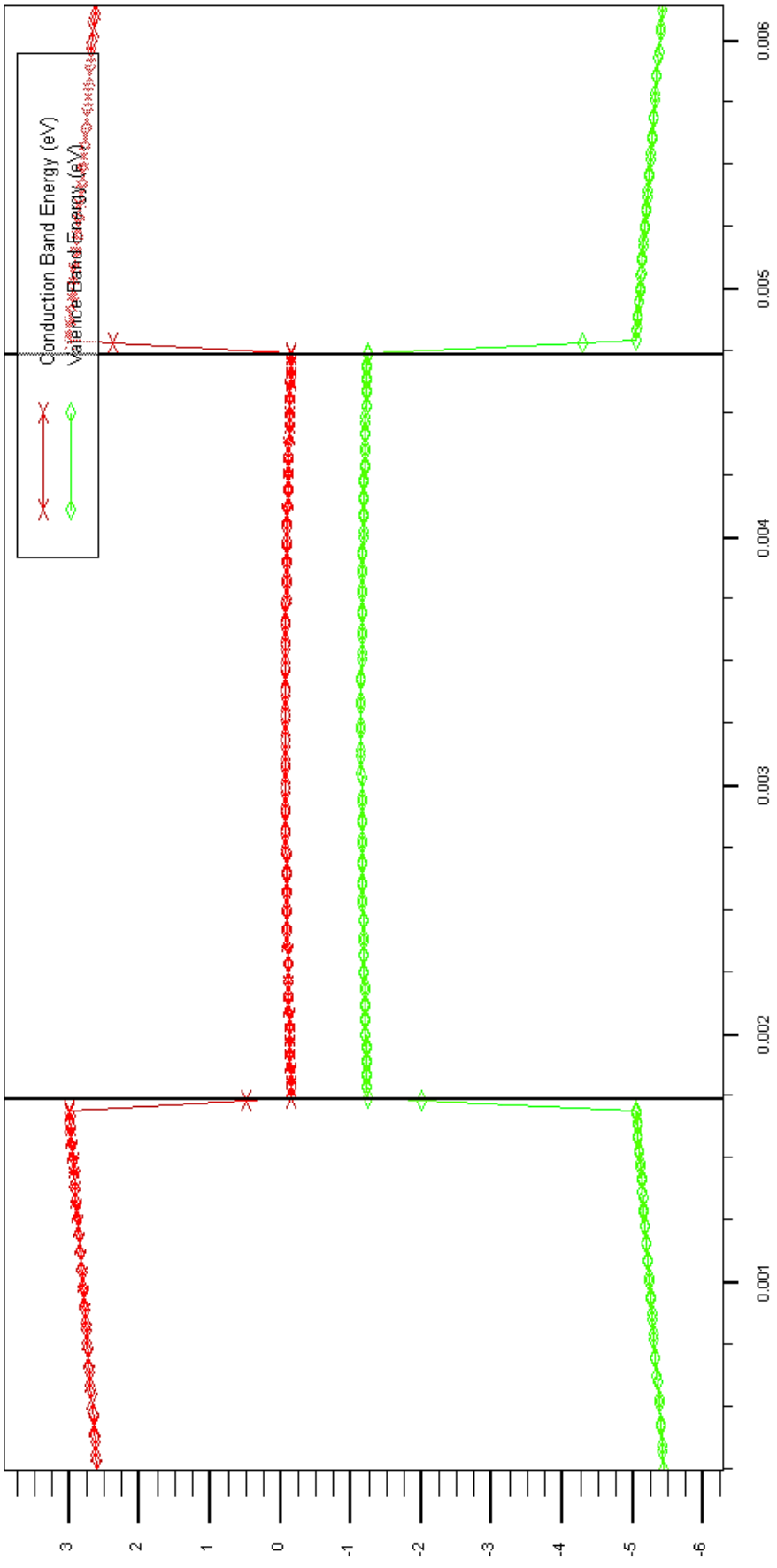

Figure 5. The conduction band energy and valence band energy.

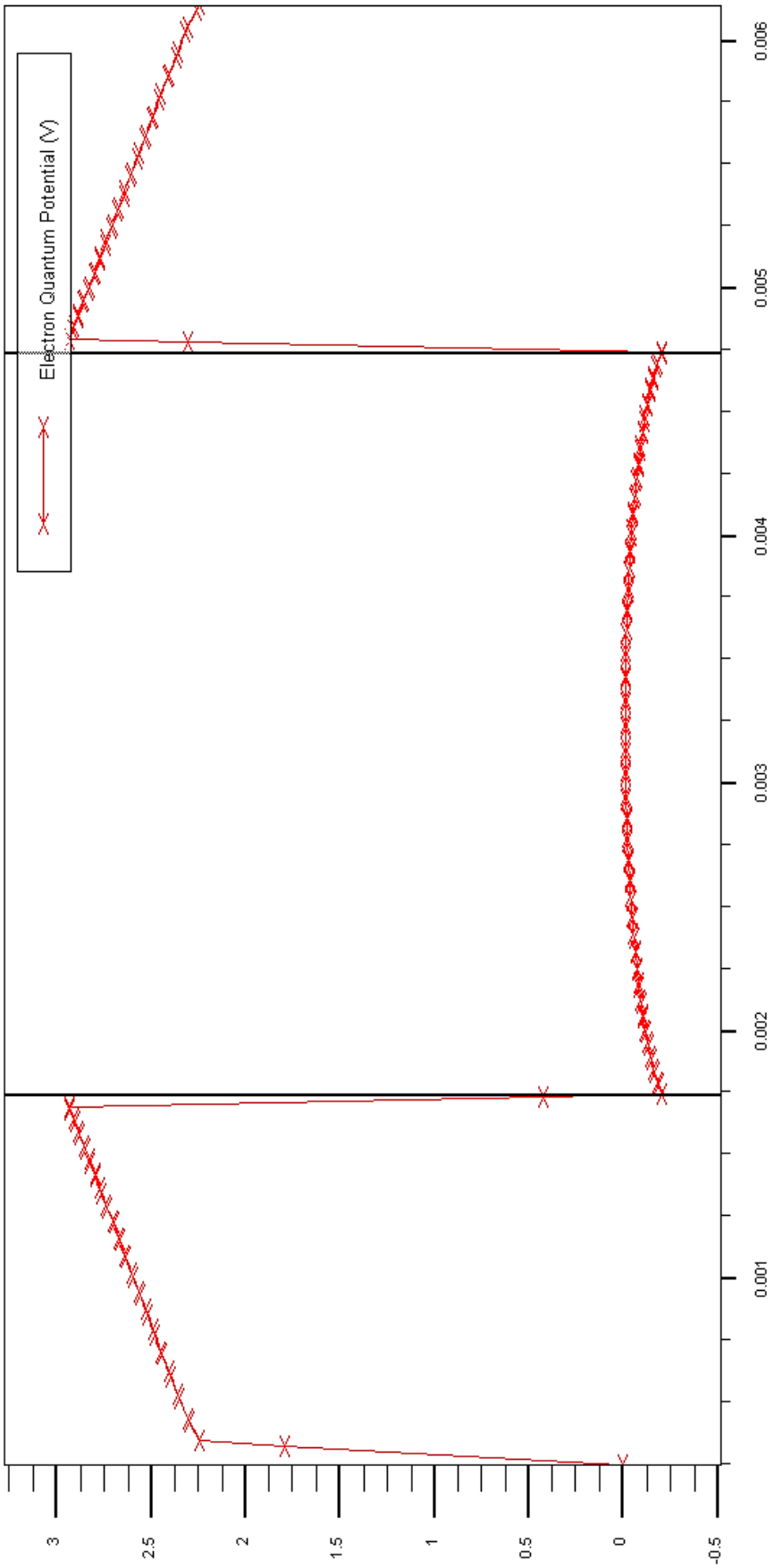

Figure 6. Electron quantum potential of the model.

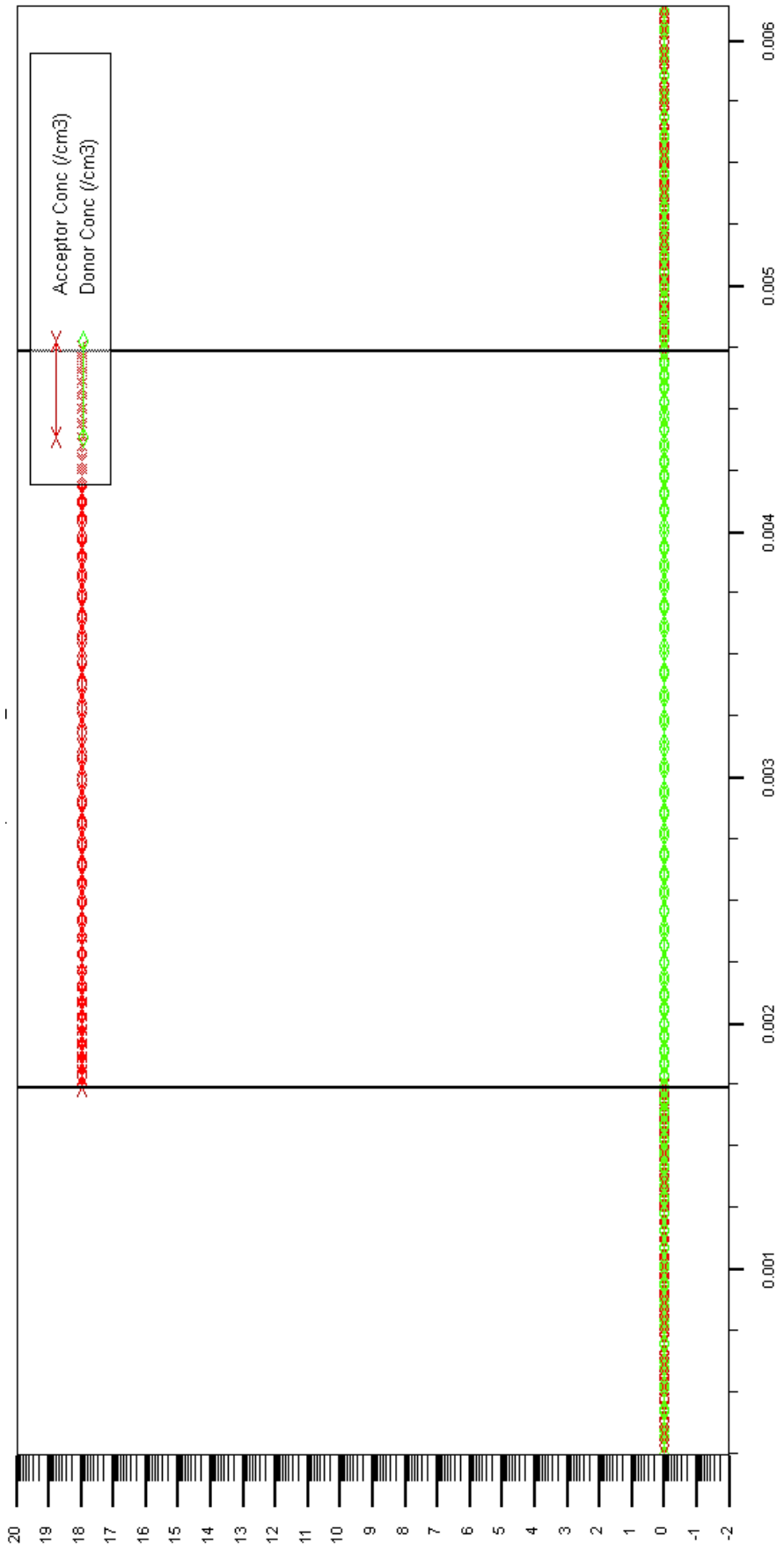

Figure 7. Variation of donor and acceptor concentration.

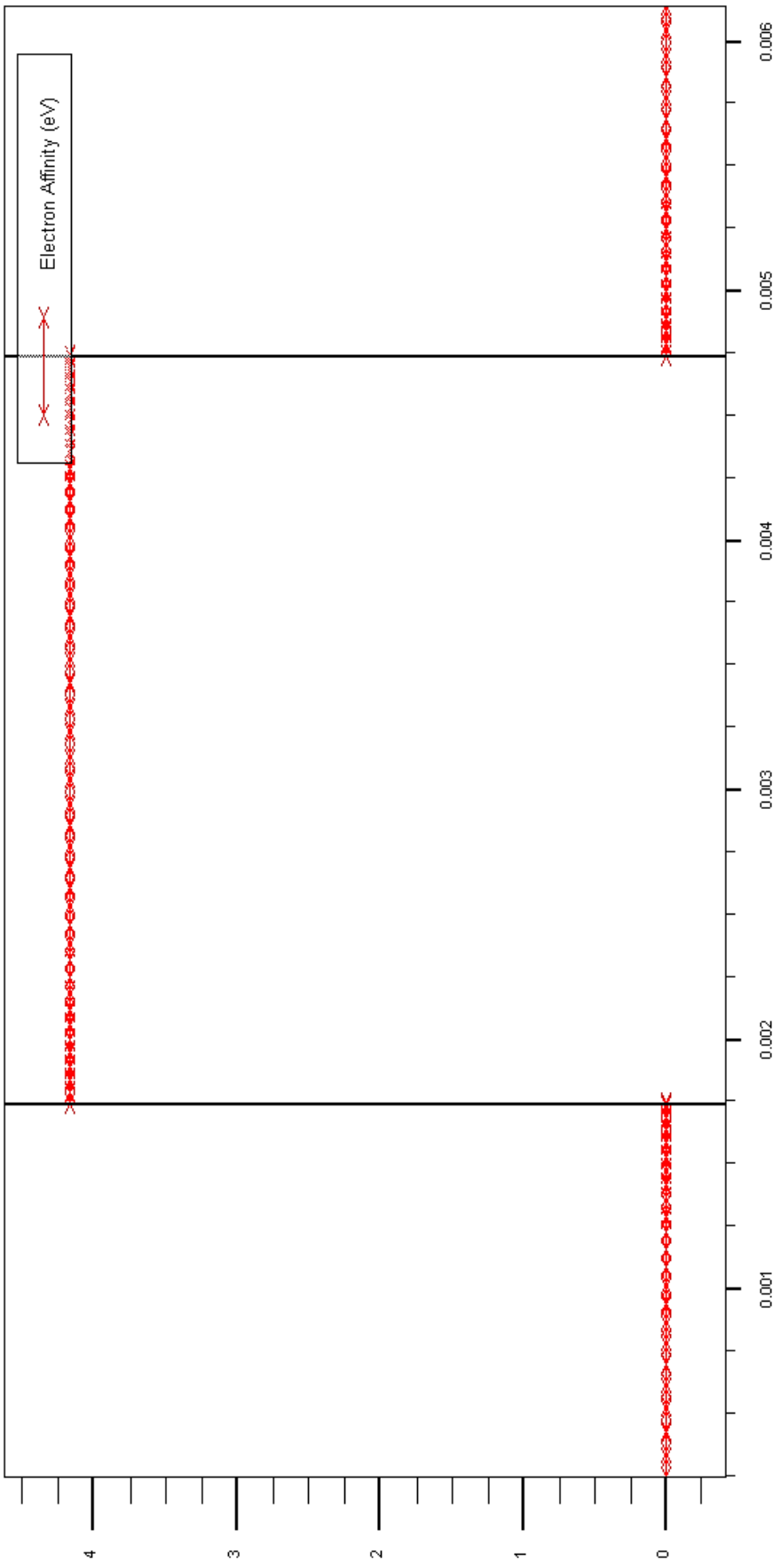

Figure 8. Variation of the electron affinity.

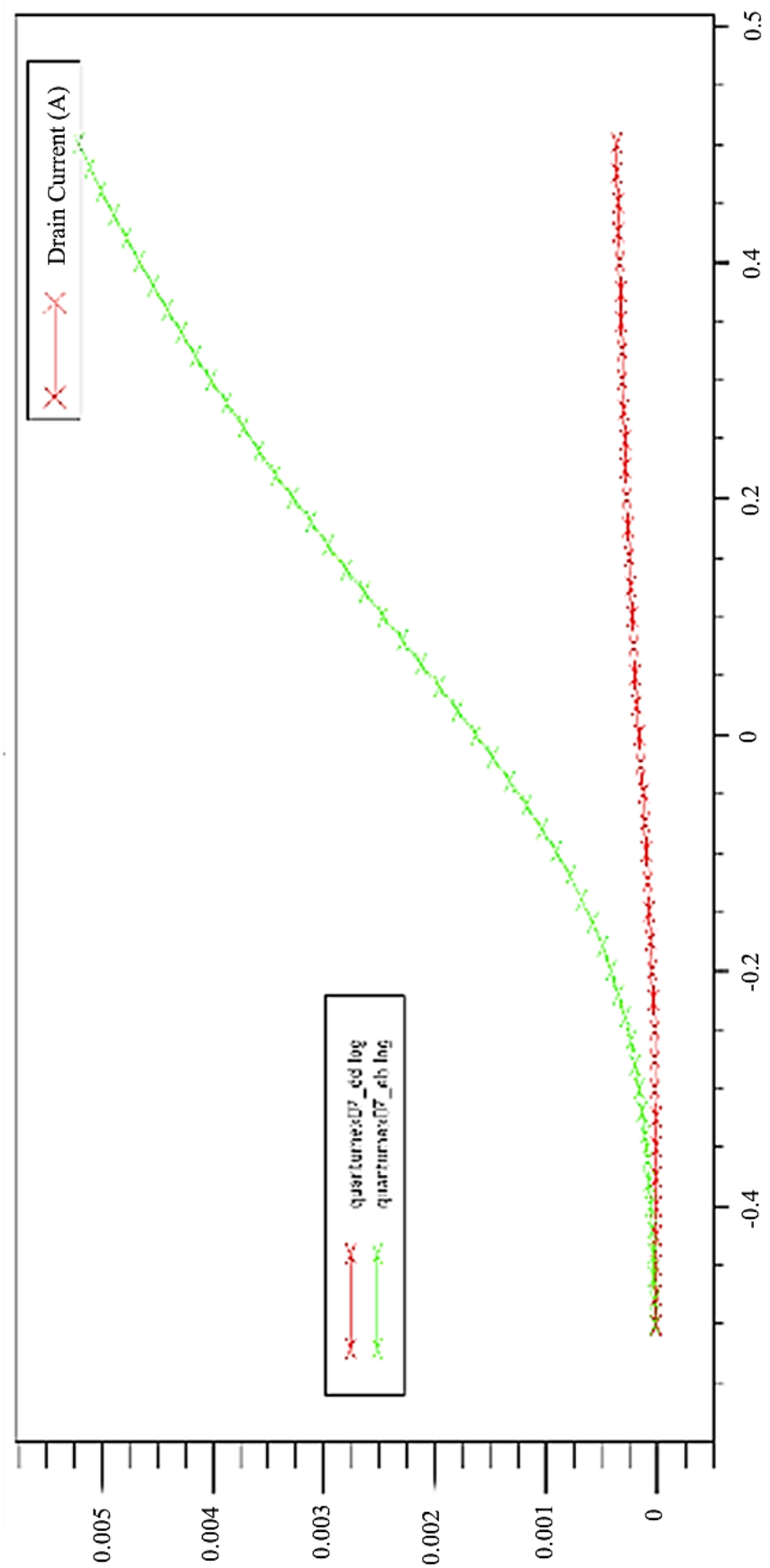

Figure 9. Variation of drain current with the variation of Vgs.

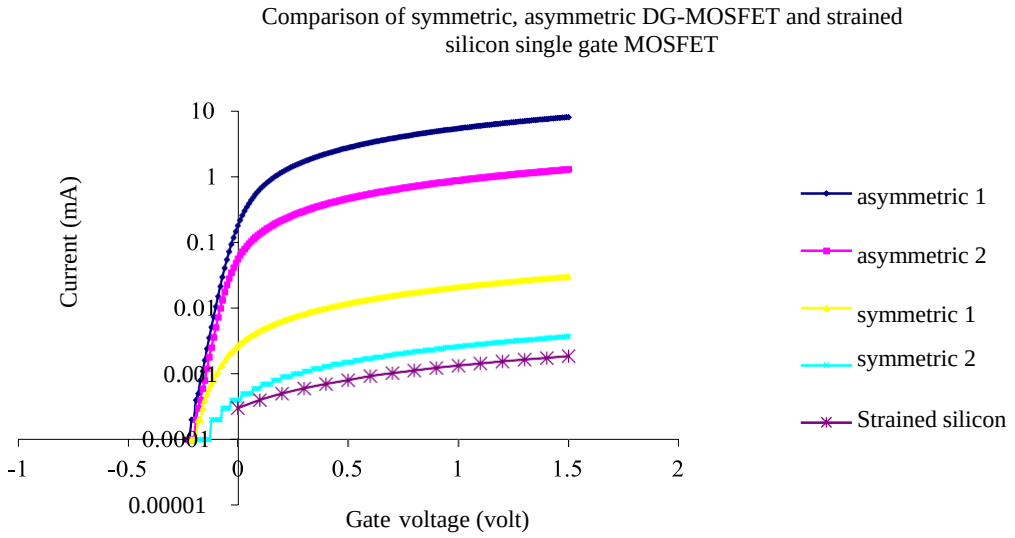

Figure 10. Variation of drain current for different models.

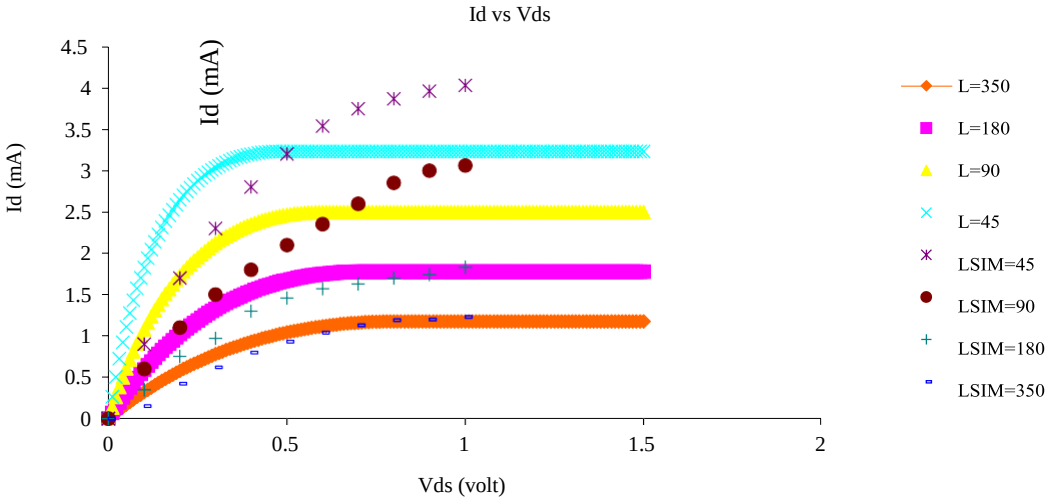

Figure 11. Comparison of drain current variation with simulated data.

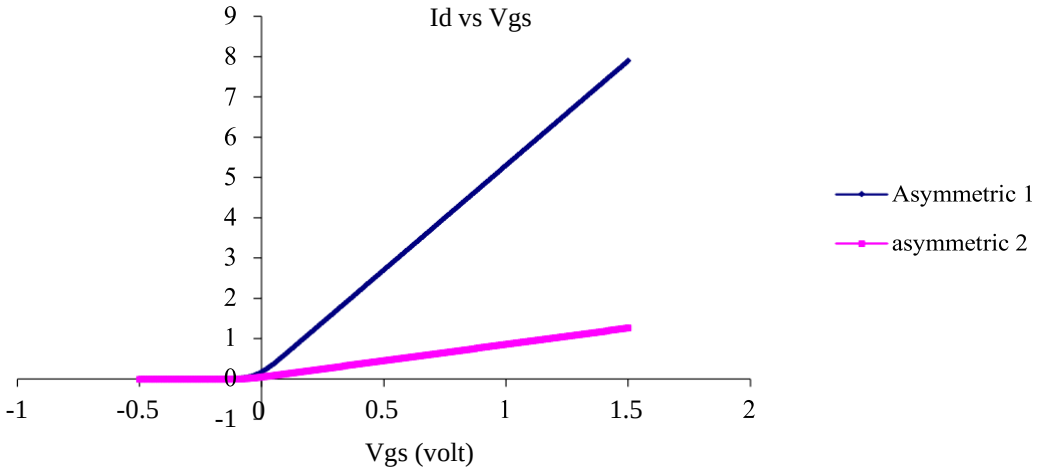

Figure 12. Comparison of drain current of asymmetric and symmetric DG-MOSFET.

CONCLUSION

In this work, a model of DG-MOSFET is studied in both analytical and simulated ways. From this study, some applications can be proposed based on the performance of the DG-MOSFET. The DG-MOSFET can efficiently provide lower threshold voltage (VTH) and higher on/off current ratio through gate coupling effect when conventional MOSFET technology becomes harder and harder to scale down in size. So, it becomes an attractive alternative. In this work, both symmetric and asymmetric DG-MOSFET models were studied. The current-voltage characteristics are compared with the strained silicon single gate MOSFET. From the comparison, it can be concluded that asymmetric DG-MOSFET is showing the better performance.

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