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Power Estimation Approach for Artix 7 FPGA using Machine Learning Technique

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Abstract

This paper presents the power estimation approach using a suitable machine learning technique. Artix7 FPGA has been chosen as the target FPGA (Field Programmable Gate Arrays) platform for understanding the methodology of power estimation. There are various approaches of power estimation for FPGAs that have been given in the literature viz. probabilistic, statistical, and LUT-based, etc. In the past few years, the demand for hand-handled devices like smartphones, tabs, laptops, and wearables has been enhanced drastically. The preferred core of these hand-handled devices is the ASICs. But due to its low performance, it has been replaced by FPGAs because of its increased speed, short turnaround time, and reduced NRE cost. Now, FPGAs have become an integral part of various DSP and telecommunication systems. Commercial tools like Xpower Analyzer, Xpower Estimator, Vivado, and Quartus II are available for estimating the power of the design implementation as per the power budget requirement. But in order to explore the design space early in the design process, the early power estimation models are used that are available in the literature. However, it has been observed that very few power estimation models are available for the estimation of the power of DSP IP cores. However, this paper discussed a supervised machine learning approach namely curve fitting and regression analysis. The approach formulates the power estimation model based on the resource estimation of the given design from the commercial tool. The major contribution of the thesis is to develop a mathematical model for power estimation of MAC IP core using curve fitting and regression, and validation using available commercial tools i.e. XPower Analyzer.

Keywords: ASIC, FPGA, LUT, SRAM, I/O, power

INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are utilized for the execution of digital circuits by the end clients. FPGAs were invented in 1984. They are basically programmable logic devices (PLD) [1, 2]. FPGA is becoming a more attractive and popular technology from a technical point of view. FPGA market consists of three parts. The first is type; it is divided into different types like mid-end FPGA, high-end FPGA, and low-end FPGA. The second is technology; from a technology point of view, it is distributed into flash, EEPROM, SRAM, and the third is application; it is used in military applications, aerospace applications, etc. These devices implement different circuits and DSP blocks because of their resources and high density of gates. As the technology is scaling down rapidly, it enables a large number of devices to be fabricated on a single chip that can be used to implement systems and circuits. For Application-

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Specific Integrated Circuits (ASICs), a single chip is used for a particular circuit or system. This involves high non-recurring (NRE) cost, that can be measured around 1 million US dollars for one application for present silicon technology and will surely increase as the technology scales down. On the other hand, FPGAs facilitate the same chip to be programmed or reprogrammed to design a variety of systems and circuits that have comparably low NRE costs [3]. Therefore, FPGAs have started to gain popularity from ASICs.

One of the most important concerns for FPGAs is high power consumption. A large number of switches and routing tracks are pre-fabricated so as to facilitate flexibility after fabrication. Tracks can consume a significant amount of power during switching as they can be long. Moreover, capacitance can be further added to the tracks by programmable switches that can lead to an increase in dissipation of power by FPGAs [4, 5]. Power consumption can be categorized as, static (spillage) and active (dynamic) power. Static power is mostly due to leakage currents in a transistor. On the other hand, dynamic power happens because of two components namely short circuit current from supply to ground, and charging and discharging of capacitors. Dynamic power constitutes near about 60% of total aggregate power. The spreadsheet-based power estimation is one of the popular methods. However, there is always a need for accurate power estimation methodology at an early stage of the design [6]. Therefore, this paper presents the power modeling methodology of an IP core for different I/O vector lengths using a machine learning approach.

FPGA INTRODUCTION

FPGAs and CPLDs are the two primary decisions in the present high-limit programmable logic device (HCPLD) advertisement [7]. CPLDs execute logic as SOP form while generally, FPGAs contain lookup tables to actualize logic. FPGAs were first presented in 1985 by Xilinx. Early FPGAs contained three primary parts: input/yield logic pads, logical assets, and the steering texture as outlined in the theoretical model in Figure 1(a). Today, merchants also insert memory and special component pieces (which ordinarily target correspondence applications) on their FPGAs as represented in the calculated model in Figure 1(b).

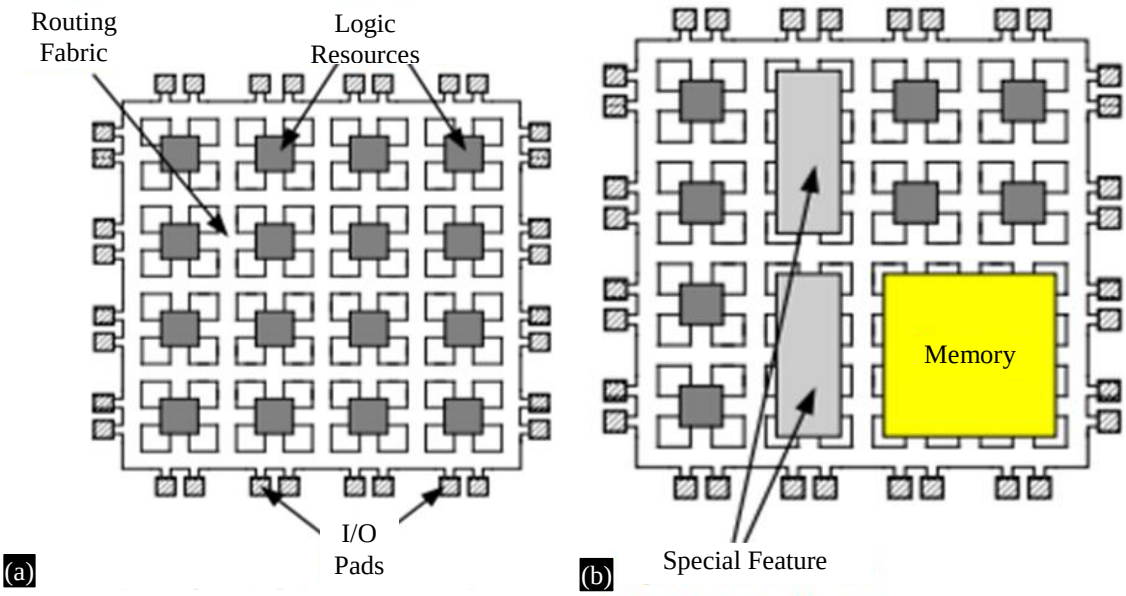

Figure 1. (a) FPGA architecture, (b) Modern FPGA architecture with memory.

FPGAs comprise a two-dimensional cluster of PLBs that are associated with a configurable interconnection texture. The present FPGAs utilize look-up tables (LUTs) as the base component for

executing combinational logic works and contain flip-flops for actualizing successive rationale [8]. A K-input LUT (K-LUT) is a little memory used for the implementation of logic functions. At most, K inputs are used. The majority of FPGAs use 4-input LUT as a base logic element; further, these logic elements are combined to form logic blocks. With such an architectural arrangement, it allows interconnections [9].

POWER DISSIPATION IN FPGAs

The total power dissipation in FPGAs depends on the following components.

Dynamic Power

Recently, many research scholars have studied and considered the breakdown of dynamic power for FPGAs [2]. In [10], breakdown of power was observed in Xilinx Virtex II commercial FPGA, and results were found such that a total of 60% of dynamic power was due to interconnects and 10% was due to IOs. In [11], a similar breakdown was observed. The dominance of FPGA interconnects in dynamic power is also due to FPGA structures. Also, memory elements (SRAM) circuitry and cells occupy a major portion of the area of FPGA's total area. The total area occupied by SRAM cells was around 40–50% of the total area [12].

Static Power

As compared to dynamic power, not much attention was given to static power as dynamic power constitutes around 60% of total power. Leakage is examined in Xilinx Spartan-3 FPGA, a 90 nm FPGA [10]. The study suggested similar results as suggested by [7]. Leakage is dominated by that consumed by interconnects, SRAM and LUT combined, as these constitute 88% of total leakage power.

LITERATURE SURVEY

Nathalie C et al. proposed a power estimation of DSP and multiplier blocks in FPGAs. In this paper, the gate level technique is used to represent the DSP blocks and constant technique, Lookup technique, and PinCap techniques were used for power characterization of DSP blocks [13].

David Elleouet et al. presented a power estimation model based on regression and a curve-fitting approach for embedded memories [14]. Abbas A et al. presents high-performance FHT architecture and develop a functional level power analysis tool for the FHT core. Pipelining and parallelism techniques are used to increase the performance of FHT [15]. Jevtic R developed a power estimation model for embedded multiplier blocks in FPGAs. The methodology is based on high-level switching activity models assuming that all DSP inputs have the same switching activity. Deng's developed the power estimation model for IP cores. The model is based on a regression and curve-fitting approach similar to Abbas' model. But Abbas developed the model for FHT core while Deng developed the model for IP cores. Other works related to power estimation of IP cores were developed by David E et al. [16] and A Amira [17]. Hassan AN presented a power estimation model for DSP cores in FPGA [18].

PROPOSED METHODOLOGY

The Xilinx ISE software has a rich number of IPs available in its library. An IP can be chosen and included in the design. Xilinx XST tool can be utilized to synthesize the IP, and values of different parameters like a number of slices, LUTs, etc. can be noted along with power values like a clock, signal, I/O, and DSP. A supervised machine learning approach like curve fitting and linear regression can be applied to formulate the power model.

The power values from the proposed model can be validated against the power values from commercial tools like Xpower Analyser. The flow diagram of the proposed methodology is shown in Figure 2.

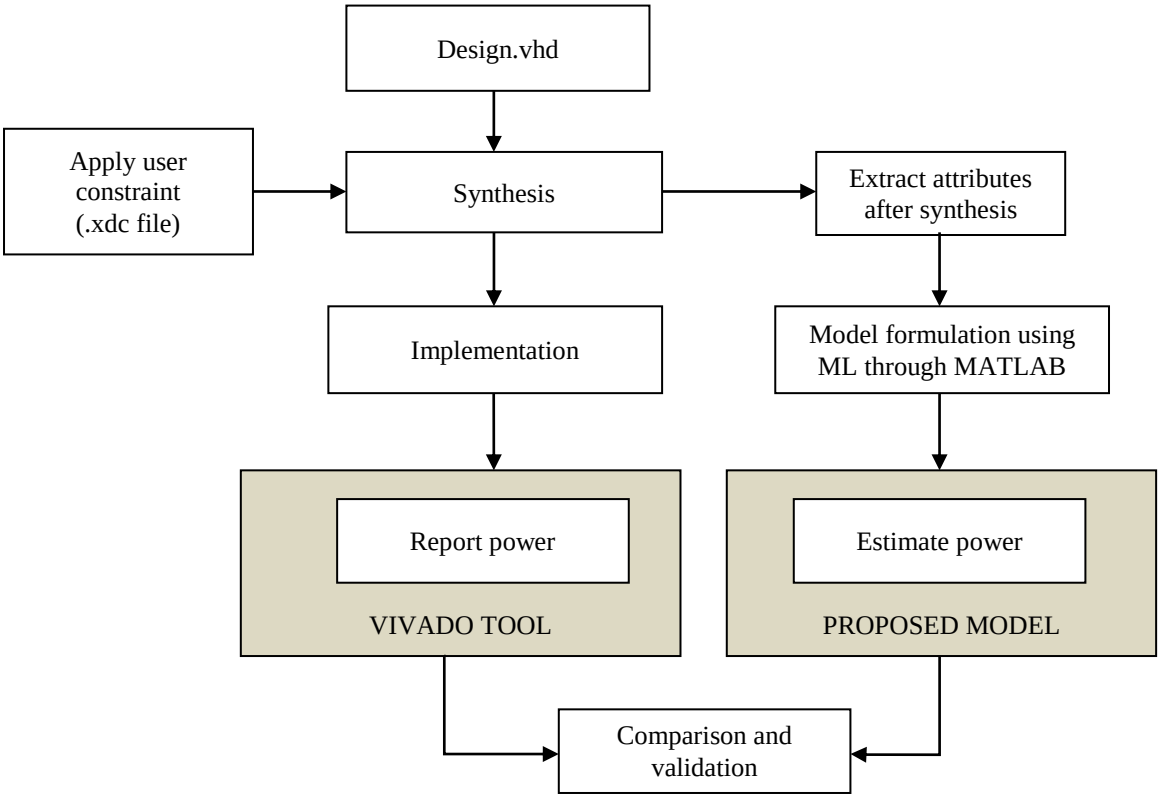

Figure 2. Flow diagram of the proposed methodology.

CONCLUSION

In this work, a mathematical model for power estimation of an IP core for Artix 7 FPGA has been developed. The IP core can be customized for different I/O configurations using the Core Generator tool available in Xilinx ISE 14.7. The modeling can be done using the machine learning technique (curve fitting and linear regression). The result shows that the proposed methodology is one of the best approaches for estimating the power of FPGA-based circuits. This approach can be applied to other complexes for developing power estimation models in the future.

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