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Improvements in Analog Performance of Dual Metal Gate based Silicon-on-Insulator Junctionless Transistor with Pocket Doped Window

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Abstract

This paper elucidates the impact of the pocket doped window on the analog performance of dual metal gate based silicon-on-insulator junctionless transistor (DMG SOIJLT). The analog parameters of the proposed SOIJLT are compared with DMG based conventional SOIJLT. The findings of analog performance comparison reveal that transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), output resistance (r_0), intrinsic gain (A_V), and cut-off frequency (f_T) have improved for DMG PD-SOIJLT as compared to DMG SOIJLT. Improvements were also found in OFF-state leakage current (I_{OFF}) and ON-OFF current ratio (I_{ON}/I_{OFF}) for DMG PD-SOIJLT. The maximum values of g_m, r_0, and f_T improved by 4.46 times, 3.84 times, and 3.85 times respectively, and A_V improved by 21.07 times in ON-state, as compared to DMG SOIJLT. The device simulation and parameter extractions have been carried out using the SILVACO ATLAS-2D device simulator.

Keywords: Analog performance, dual metal gate (DMG), intrinsic gain, junctionless transistor (JLT), pocket doped window, silicon-on-insulator (SOI), output resistance

INTRODUCTION

Today, device scaling has reached a nanoscale regime due to which short channel effects (SCEs) have become a major problem to be tackled down and to make the device efficient for analog and high-frequency applications [1]. Researchers are continuously making efforts to present alternatives to impart changes in the conventional metal oxide semiconductor FET (MOSFET). In the run, silicon-on-insulator (SOI) technology has proven to be effective in mitigating short channel effects, bulk current leakage, and producing enhanced mobility, improved latch-up immunity, reduced junction capacitances [2]. Charge sharing between drain and source region increases as the length of the device is reducing. This increases the leakage current within the transistor.

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The ultra-steep junction formation in the junction transistor poses another major hindrance while dealing with short channel effects. The solution to this problem is a 'junctionless transistor' [3, 4]. It has no source/channel and drain/channel junction. All three regions—drain, channel, and source, are doped with the same type of dopant and same concentration. It works like a gated resistor [5, 6]. The dual material gate (DMG) structure helps to create step potential in the channel region thus helps to mitigate SCEs and boost the transconductance [7]. The two gate materials have distinct metal work functions and the proper arrangement of the two metals and their effects in n-channel and p-channel MOSFETs have

already been studied [8–10]. The effect of DMG structure in full depleted (FD) SOI MOS transistor is that it creates a step function in the potential distribution of channel region. This DMG structure also reduces the hot carrier effect by reducing the peak electrical field in the channel region at the drain end [11]. DMG based FDSOI transistor performance has been studied in [12–14]. DMG structure helps to reduce output conductance and DIBL [12]. Thus, contributing to better analog application.

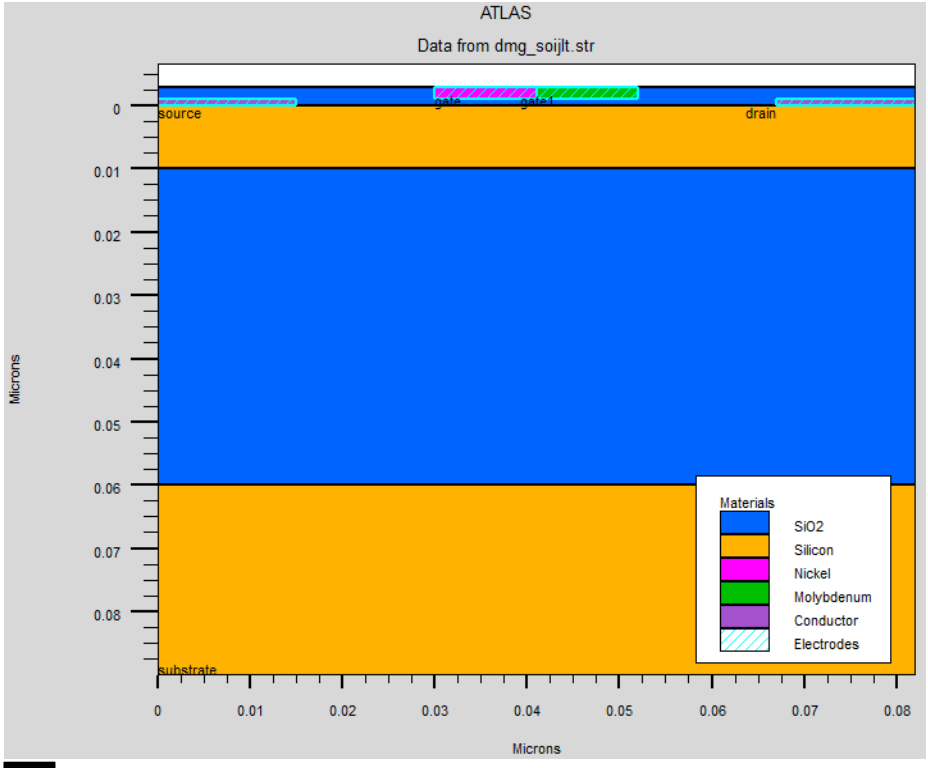
The SOI based junctionless transistor (SOIJLT) suffers from high OFF-state leakage problems. So, researchers have introduced a p-type pocket doped window (PD) inside the buried oxide which greatly enhances the device efficiency [15, 16]. Heavy doping of the pocket drastically reduces the leakage current [16]. The analog performance of DMG SOIJLT is already studied in [12].

This paper is thus intended to propose a new structure for DMG SOIJLT using a p-type pocket doped window and to compare its analog performance with conventional SOIJLT. Various parameters of DMG PD-SOIJLT viz. OFF-state current (I_{OFF}), ON-OFF current ratio (I_{ON}/I_{OFF}), transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), output resistance (r_0), intrinsic gain (A_V), parasitic capacitances, and cut-off frequency (f_T), have been extracted using SILVACO ATLAS-2D device simulator and is compared with that of DMG SOIJLT.

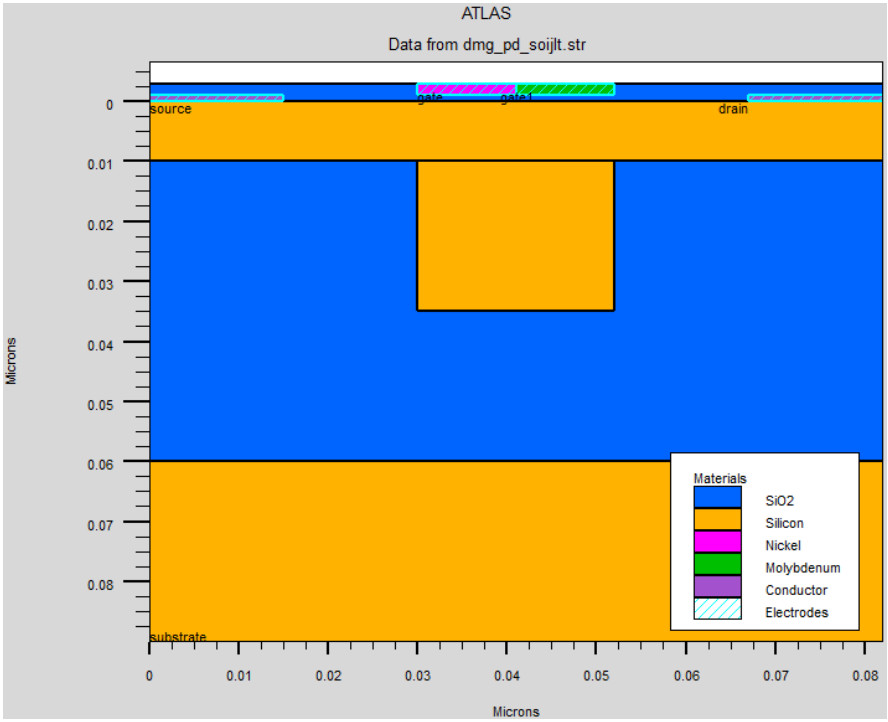
The paper is organized into four sections including the introduction Section I. Henceforth, Section II deals with the device specifications and simulation methodology, Section III deals with results and discussion, and Section IV is the conclusion.

DEVICE SPECIFICATIONS AND SIMULATION METHODOLOGY

The dual metal gate structure is incorporated in pocket doped window-based silicon-on-insulator junctionless transistor termed as DMG PD-SOIJLT and is simulated using SILVACO ATLAS-2D device simulator. The simulated structures of DMG SOIJLT and DMG PD-SOIJLT are shown in Figure 1(a) and 1(b) respectively.



(a)



(b)

Figure 1. Simulated structures of (a) DMG SOIJLT (b) DMG PD-SOIJLT.

Table 1. Various device parameters used in the simulation of DMG PD-SOIJLT.

Parameters	**DMG PD-SOIJLT**	
Channel length, L_C (nm)	22	
Silicon channel thickness, t_{si} (nm)	10	
Buried oxide thickness, t_{BOX} (nm)	50	
Gate oxide thickness, t_{ox} (EOT) (nm)	1	
Channel doping, N_D (cm^{-3})	1×10^{19}	
Gate work function (eV)	L_C (Ni)	L_S (Mo)
	5.01	4.53
Control gate length, L_C (nm)	11	
Screen gate length, L_S (nm)	11	
Pocket thickness, t_{PD} (nm)	25	
Pocket length, L_{PD} (nm)	22	
Pocket doping (p-type) (cm^{-3})	5×10^{19}	
Substrate doping, N_A (p-type) (cm^{-3})	5×10^{18}	

The gate metal near the source side is ‘control gate’ and is assigned Nickel (Ni) metal while gate metal near the drain side is ‘screen gate’ and is assigned Molybdenum (Mo) metal. Nickel and molybdenum have work function values of 5.01 eV and 4.53 eV respectively [17]. The control gate has a high work function and screen gate is set at a low work function and both gate metals have equal lengths 11nm each. The pocket window is doped heavily with p-type dopants of concentration $5 \times 10^{19} cm^{-3}$ [16].

The pocket doped window is 22nm long formed in buried oxide just below the channel region and in vertical alignment with the gate [15]. Various device specifications are listed in Table 1. The DMG SOIJLT has the same structural parameters as that of DMG PD-SOIJLT except it does not have the pocket doped window. Different models such as CVT (constant voltage and temperature mobility model), SRH

(Shockley-Reed-Hall recombination model), BGN (bandgap narrowing model), Auger (Auger recombination model), and Fermi-Dirac (Fermi-Dirac statistics model) have been considered [18].

RESULTS AND DISCUSSION

Figure 2 shows the variation of drain-to-source current (I_{DS}) against gate-to-source voltage (V_{GS}) of both DMG SOIJLT and DMG PD-SOIJLT, on (a) linear and (b) log scale. The OFF-state is assumed at V_{GS} = 0V and ON-state at V_{GS} = V_{DS} = 1V. Due to better depletion being achieved in DMG PD-SOIJLT with a heavily doped p-type pocket window, the OFF-state leakage current (I_{OFF}) has drastically reduced by manifolds. But the ON-state current (I_{ON}) has also reduced because the effective channel thickness has decreased in the case of DMG PD-SOIJLT which in turn limits the maximum rise of current due to less availability of electrons in the channel region as compared to DMG SOIJLT. The I_{ON}/I_{OFF} ratio in the case of DMG PDSOIJLT is obtained greater than 10^6 while that of DMG SOIJLT is less than 10.

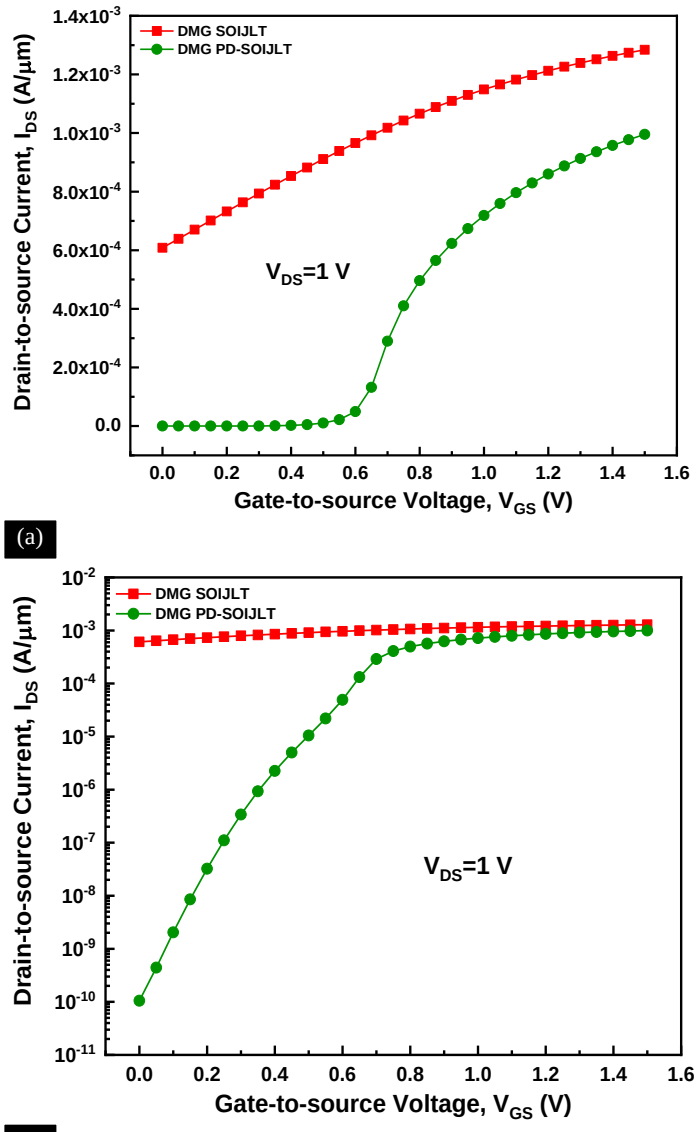


Figure 2. I_{DS}-V_{GS} curve of DMG SOIJLT and DMG PD-SOIJLT on (a) linear and (b) log scale.

Figure 3 shows the variation of drain-to-source current (I_{DS}) against drain-to-source voltage (V_{DS}) of both JLTs. Here also, drain current is obtained less in the case of DMG PD-SOIJLT. This is less

appreciable for the proposed device but still, other analog parameters have greatly improved.

In Figure 4, the plot of transconductance (g_m) against gate-to-source voltage (V_{GS}) is shown. Transconductance defines the device efficiency for conversion of voltage to current. So, a higher value of g_m is always desirable. The transconductance is also increased for DMG PD-SOIJLT; it provides max transconductance of 2.77 mS which is 4.46 times better as compared to that of DMG SOIJLT giving max g_m equal to 0.62 mS.

$$TGF = \frac{g_m}{I_{DS}} \tag{1}$$

Transconductance generation factor (TGF) or power efficiency (given by Eq.1) is also an important analog parameter that specifies the profitable use of the drain current to procure the accepted transconductance value. In the subthreshold region of operation, the ratio g_m/I_{DS} is regarded as maximum. In Figure 4, it is shown that TGF is the maximum for DMG PD-SOIJLT (~ 43.68 V^{-1}) as compared to the maximum TGF (1.007 V^{-1}) of DMG SOIJLT.

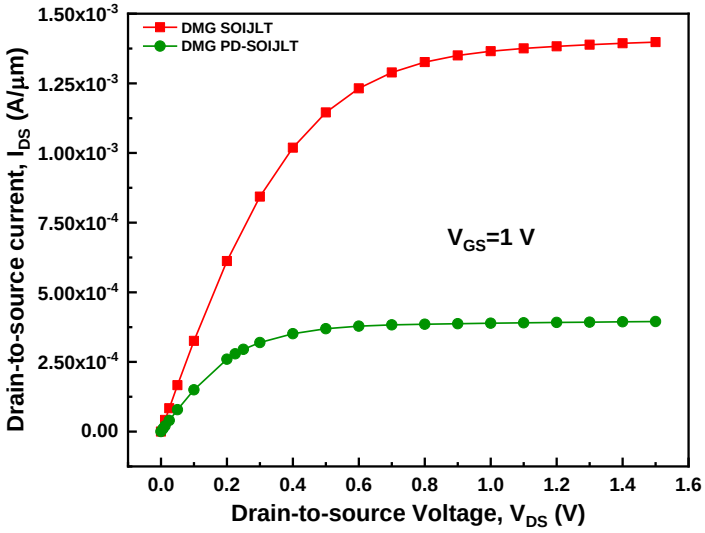


Figure 3. I_{DS}-V_{DS} curve of DMG SOIJLT and DMG PD-SOIJLT.

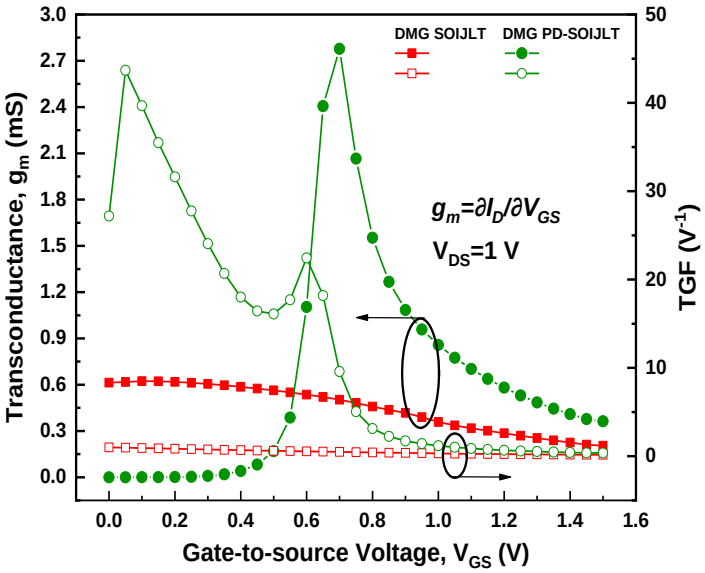


Figure 4. g_m-V_{GS} and TGF-V_{GS} curves of DMG SOIJLT and DMG PD-SOIJLT.

Figure 5 depicts the output-conductance (g_d) and output resistance (r_0) variations against the drain-to-source voltage of both JLTs. The output resistance is determined as a reciprocal of output (drain) conductance. The g_d is decreasing and r_0 is increasing in saturation region as compared to the subthreshold region for both JLTs. DMG PD-SOIJLT is showing lower output conductance (0.011 mS) and higher output resistance (85.78 Kohm) against DMG SOIJLT (0.044 mS and 22.29 Kohm respectively) in the saturation region. This indicates that DMG PD-SOIJLT is less vulnerable to channel length modulation. Hence, for designing analog circuits, particularly analog amplifiers, DMG PD-SOIJLT is more advantageous.

In Figure 6, the plot for gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) against gate voltage is shown. The parasitic capacitances are extracted by performing small-signal ac analysis at V_{DS} = 1V and frequency 100MHz after performing dc analysis. The C_{gd} is decreasing and C_{gs} is increasing for DMG PD-SOIJLT as compared to the DMG SOIJLT. The increase in C_{gs} is due to the additional capacitive coupling arising in DMG PD-SOIJLT due to the vertically formed p-n junction-like structure between gate and source at the pocket window and channel interface. This p-n junction depletion is also responsible for decreased coupling between gate and drain.

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{2}$$

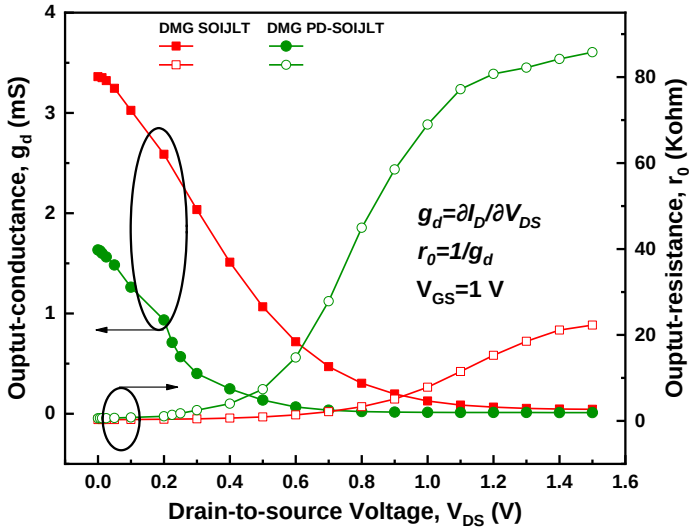


Figure 5. g_d-V_{DS} and r_0-V_{DS} curves of DMG SOIJLT and DMG PD-SOIJLT.

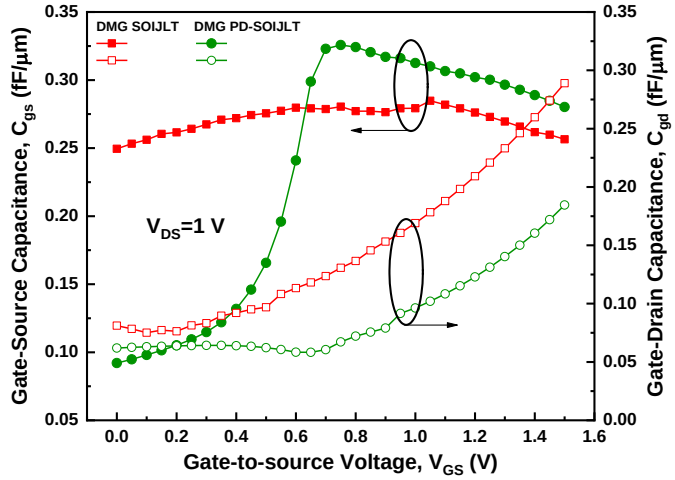


Figure 6. C_{gs}-V_{GS} and C_{gd}-V_{GS} curves of DMG SOIJLT and DMG PD-SOIJLT.

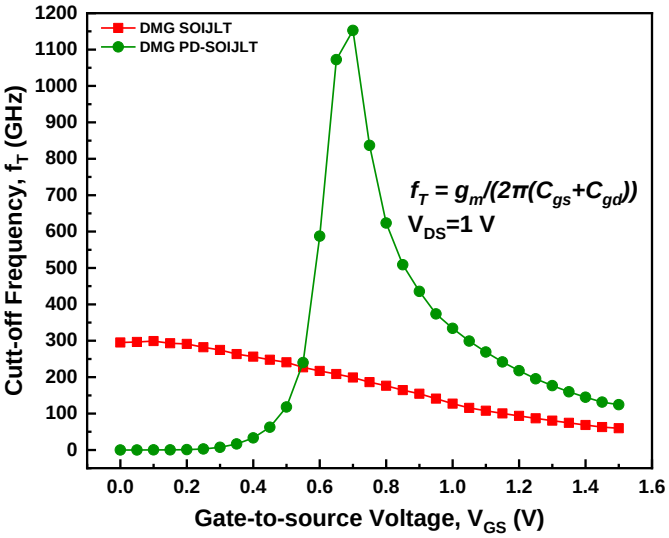


Figure 7. f_T-V_{GS} curve of DMG SOIJLT and DMG PD-SOIJLT.

Figure 7 presents the variation of cut-off frequency (f_T) against gate-to-source voltage (V_{GS}) for both JLTs and is given by Eq. 2. Cut-off (unity gain) frequency is a transition point between the amplification and attenuation capability of the device. Hence, higher f_T is always desirable. Despite the increased C_{gs} in DMG PD-SOIJLT, the increased g_m and decreased C_{gd} compensates for the effect of C_{gs}, and DMG PD-SOIJLT can produce a maximum f_T of 1152.48 GHz which is a 3.85 times improvement over DMG SOIJLT (f_T max =299.28 GHz).

$$A_V = g_m r_0 = \frac{g_m}{g_d} \tag{3}$$

Table 2. Performance comparision between DMG SOIJLT and DMG PD-SOIJLT.

Performance parameters	DMG SOIJLT	DMG PD-SOIJLT
OFF state current, I_{OFF} (A)	6.08439×10^{-4}	1.04889×10^{-10}
ON state current, I_{ON} (A)	1.15×10^{-3}	7.188×10^{-4}
I_{ON}/I_{OFF} ratio	1.89	6.85×10^{6}
Intrinsic gain, A_V at $V_{DS} = V_{GS}$ = 1V	2.808	59.17
g_m max (mS)	0.62	2.77
f_T max (GHz)	299.28	1152.48

The performance of the analog circuit is also evaluated by the intrinsic gain (A_V). It is formulated as the ratio of g_m and g_d (or product of g_m and r_0) and is defined as the maximum gain of a single MOS transistor (refer Eq. 3). From Table 2, it is observed that the dual metal gate structure is successfully able to enhance the intrinsic gain of DMG PD-SOIJLT (~59.17) nearly 21.07 times improved as compared to DMG SOIJLT (~2.808). Thus, the device is able to produce higher gain and higher output resistance simultaneously, which is highly desired for low-power analog amplifiers.

CONCLUSION

In this work, DMG PD-SOIJLT and DMG SOIJLT have been simulated and the impact of pocket doped window has been analyzed on analog performance parameters of DMG SOIJLT. The analog performance of DMG PD-SOIJLT is improved tremendously when compared against DMG SOIJLT. Transconductance (g_m), transconductance generation factor (TGF), output conductance (g_d), output resistance (r_0), intrinsic gain (A_V), and cut-off frequency (f_T) have been improved for DMG PD-SOI JLT as compared to DMG SOIJLT. OFF-state leakage current (I_{OFF}) and ON-OFF current ratio (I_{ON}/I_{OFF}) have also improved for DMG PD-SOIJLT. The ON-state current is less appreciable for the

suggested DMG PD-SOIJLT but still, other analog parameters have improved significantly. The maximum values of g_m, r_0, and f_T are found to be improved by 4.46 times, 3.84 times, and 3.85 times respectively, and A_V is improved by 21.07 times in ON-state, as compared to DMG SOIJLT. Hence the device can be a suitable candidate for low-power analog applications.

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